

TMS44400, TMS44400P, TMS46400, TMS46400P  
1048576-WORD BY 4-BIT  
DYNAMIC RANDOM-ACCESS MEMORIES

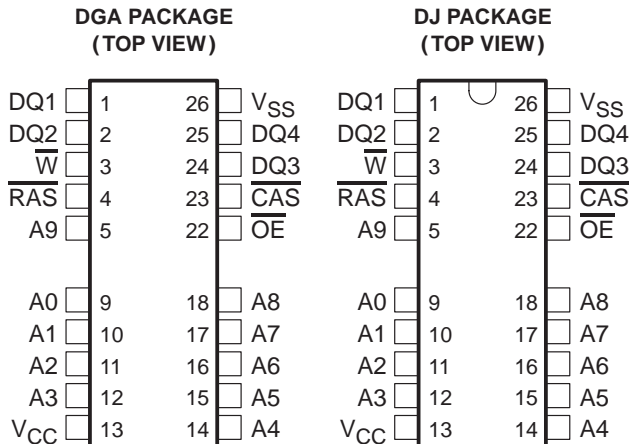
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- Organization . . . 1048576 × 4
- Single 5-V Power Supply for TMS44400/P (±10% Tolerance)
- Single 3.3-V Power Supply for TMS46400/P (±10% Tolerance)
- Low Power Dissipation (TMS46400P only)
  - 200-μA CMOS Standby
  - 200-μA Self Refresh
  - 300-μA Extended-Refresh Battery Backup

● Performance Ranges:

	ACCESS TIME (MAX)	ACCESS TIME (MAX)	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
	(t <sub>RAC</sub> )	(t <sub>CAC</sub> )	(t <sub>AA</sub> )	
'4x400/P-60	60 ns	15 ns	30 ns	110 ns
'4x400/P-70	70 ns	18 ns	35 ns	130 ns
'4x400/P-80	80 ns	20 ns	40 ns	150 ns

- Enhanced Page-Mode Operation for Faster Memory Access
- $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  (CBR) Refresh
- Long Refresh Period
  - 1024-Cycle Refresh in 16 ms
  - 128 ms (MAX) for Low-Power, Self-Refresh Version (TMS4x400P)
- 3-State Unlatched Output
- Texas Instruments EPIC™ CMOS Process



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
DQ1–DQ4	Data In
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V <sub>CC</sub>	5-V or 3.3-V Supply
V <sub>SS</sub>	Ground
$\overline{\text{W}}$	Write Enable

- Operating Free-Air Temperature Range 0°C to 70°C

description

The TMS4x400 series is a set of high-speed, 4194304-bit dynamic random-access memories (DRAMs), organized as 1048576 words of four bits each. The TMS4x400P series is a set of high-speed, low-power, self-refresh with extended-refresh, 4194304-bit DRAMs, organized as 1048576 words of four bits each. Both series employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power.

These devices feature maximum  $\overline{\text{RAS}}$  access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4x400 and TMS4x400P are offered in a 20/26-lead plastic small-outline (TSOP) package (DGA suffix) and a 300-mil 20/26-lead plastic surface-mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44400	5 V	—	1024 in 16 ms
TMS44400P	5 V	Yes	1024 in 128 ms
TMS46400	3.3 V	—	1024 in 16 ms
TMS46400P	3.3 V	Yes	1024 in 128 ms



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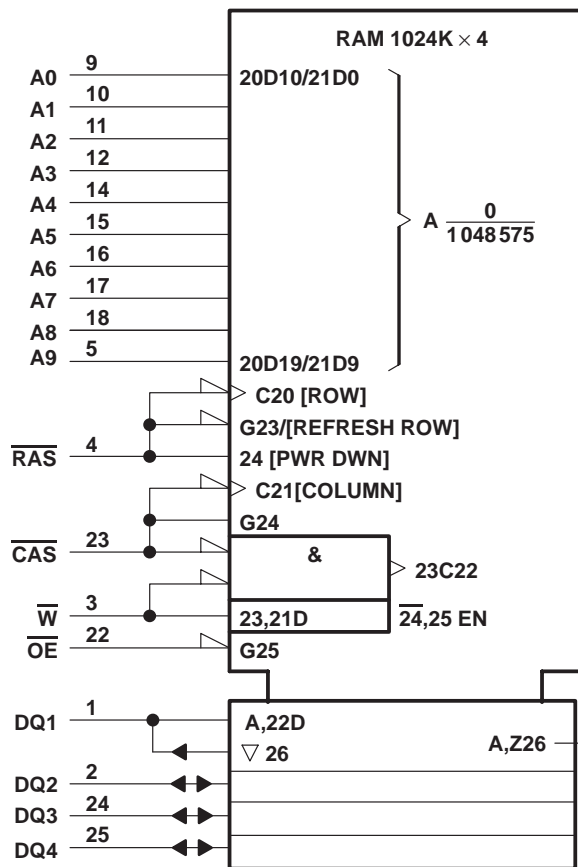
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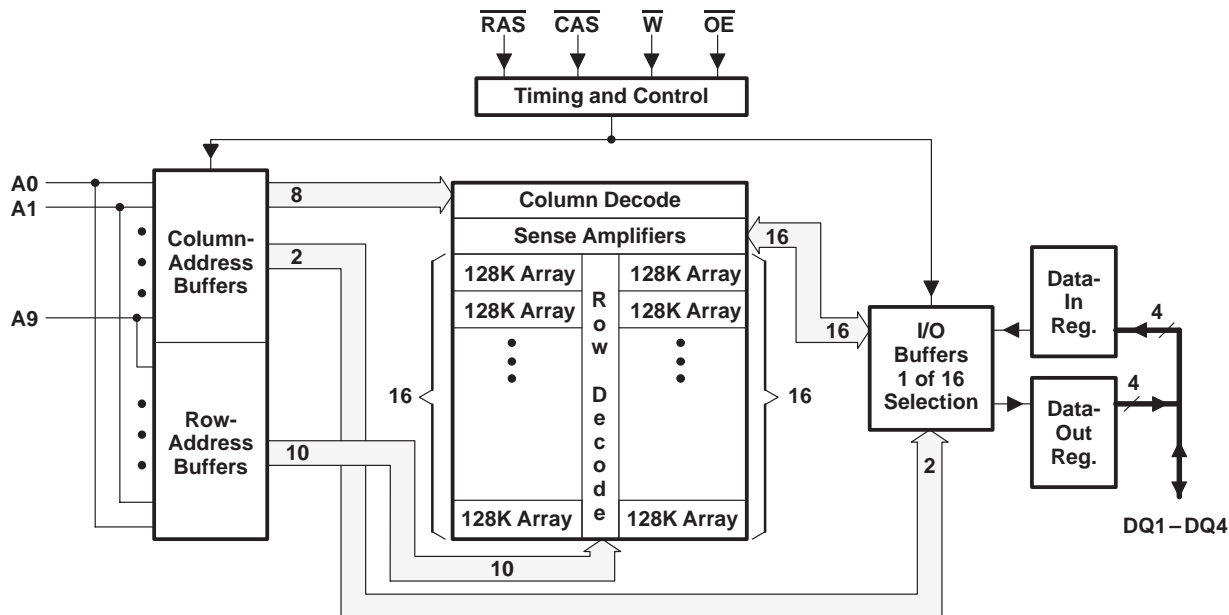
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DJ package.

functional block diagram



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## operation

### enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum  $\overline{RAS}$  low time and the  $\overline{CAS}$  page cycle time used. With minimum  $\overline{CAS}$  page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening  $\overline{RAS}$  cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of  $\overline{RAS}$ . The buffers act as transparent or flow-through latches while  $\overline{CAS}$  is high. The falling edge of  $\overline{CAS}$  latches the column addresses. This feature allows the TMS4x400 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when  $\overline{CAS}$  transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of  $\overline{CAS}$ . In this case, data is obtained after  $t_{CAC}$  maximum (access time from  $\overline{CAS}$  low) if  $t_{AA}$  maximum (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time  $\overline{CAS}$  goes high, access time for the next cycle is determined by the later occurrence of  $t_{CAC}$  (access time from  $\overline{CAS}$  low) or  $t_{CPA}$  (access time from column precharge).

### address (A0–A9)

Twenty address bits are required to decode any one of the 1048576 storage-cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by  $\overline{RAS}$ . The ten column-address bits are set up on A0 through A9 and latched onto the chip by  $\overline{CAS}$ . All addresses must be stable on or before the falling edges of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip enable because it activates the sense amplifiers as well as the row decoder.  $\overline{CAS}$  is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

### write enable ( $\overline{W}$ )

The read or write mode is selected through  $\overline{W}$  input. A logic high on  $\overline{W}$  selects the read mode and a logic low selects the write mode.  $\overline{W}$  can be driven from standard TTL circuits (TMS44400/P) or low voltage TTL circuits (TMS46400/P) without a pullup resistor. The data input is disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$  (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of  $\overline{OE}$ . This permits early-write operation to complete with  $\overline{OE}$  grounded.

### data in/out (DQ1–DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{CAS}$  and  $\overline{OE}$  are brought low. In a read cycle, the output becomes valid after all access times are satisfied. The output remains valid while  $\overline{CAS}$  and  $\overline{OE}$  are low.  $\overline{CAS}$  or  $\overline{OE}$  going high returns the output to a high-impedance state. This is accomplished by bringing  $\overline{OE}$  high prior to applying data, satisfying the  $\overline{OE}$  to data delay hold time ( $t_{OED}$ ).

### output enable ( $\overline{OE}$ )

$\overline{OE}$  controls the impedance of the output buffers. When  $\overline{OE}$  is high, the buffers remain in the high-impedance state. Bringing  $\overline{OE}$  low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both  $\overline{RAS}$  and  $\overline{CAS}$  to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either  $\overline{OE}$  or  $\overline{CAS}$  is brought high.

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#### refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x400P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a  $\overline{\text{RAS}}$ -only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  after a read operation and cycling  $\overline{\text{RAS}}$  after a specified precharge period, similar to a  $\overline{\text{RAS}}$ -only refresh cycle. The external address is ignored during the hidden-refresh cycle.

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is utilized by bringing  $\overline{\text{CAS}}$  low earlier than  $\overline{\text{RAS}}$  (see parameter  $t_{\text{CSR}}$ ) and holding it low after  $\overline{\text{RAS}}$  falls (see parameter  $t_{\text{CHR}}$ ). For successive CBR refresh cycles,  $\overline{\text{CAS}}$  can remain low while cycling  $\overline{\text{RAS}}$ . The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300- $\mu\text{A}$  (TMS46400P) or 500- $\mu\text{A}$  (TMS44400P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125  $\mu\text{s}$  while holding  $\overline{\text{RAS}}$  low for less than 1  $\mu\text{s}$ . To minimize current consumption, all input levels need to be at CMOS levels ( $V_{\text{IL}} \leq 0.2 \text{ V}$ ,  $V_{\text{IH}} \geq V_{\text{CC}} - 0.2 \text{ V}$ ).

#### self refresh

The self-refresh mode is entered by dropping  $\overline{\text{CAS}}$  low prior to  $\overline{\text{RAS}}$  going low.  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  are both held low for a minimum of 100  $\mu\text{s}$ . The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are brought high to satisfy  $t_{\text{CHS}}$ . Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation, to ensure that the DRAM is fully refreshed.

#### power up

To achieve proper device operation, an initial pause of 200  $\mu\text{s}$  followed by a minimum of eight initialization cycles is required after full  $V_{\text{CC}}$  level is achieved. These eight initialization cycles must include at least one refresh ( $\overline{\text{RAS}}$ -only or CBR) cycle.

#### test mode

The test mode is initiated with a CBR refresh cycle while simultaneously holding  $\overline{\text{W}}$  low (WCBR). The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a CBR refresh cycle with  $\overline{\text{W}}$  held high or a  $\overline{\text{RAS}}$ -only refresh (ROR) cycle is performed.

The TMS4x400/P is configured as a 512K  $\times$  8 bit device in test mode, where each DQ pin has a separate 2-bit parallel read- and write-data bus. During a read cycle, the two internal bits are compared for each DQ pin separately. If the two bits agree, the DQ pin goes high; if not, the DQ pin goes low. The two bits are written to reflect the state of their respective DQ pins during a parallel-write operation. Each DQ pin is independent of the others, and any data pattern desired can be written on each DQ pin. Test time is reduced by a factor of 4 for this series.

test mode (continued)

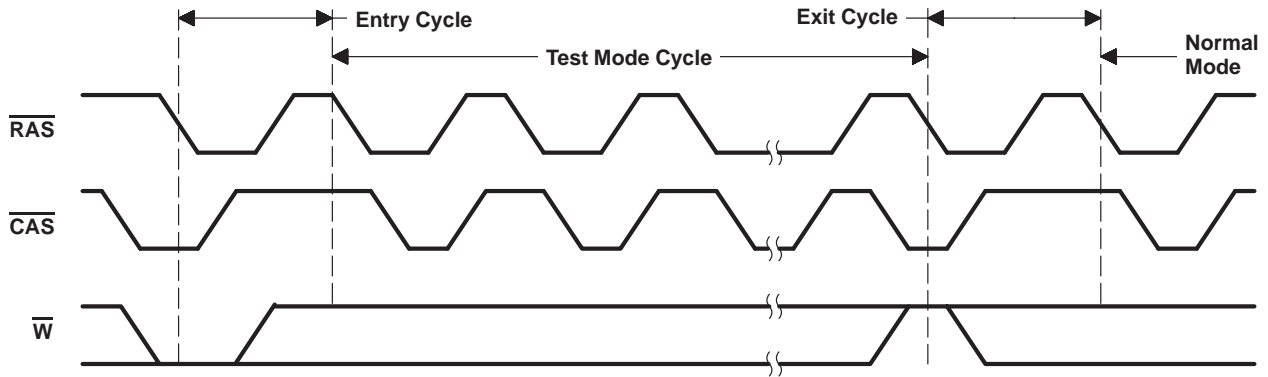


Figure 1. Test-Mode Cycle Timing†

† The states of  $\overline{W}$ , data in, and address are defined by the type of cycle used during test mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ :	TMS44400, TMS44400P .....	- 1.0 V to 7.0 V
	TMS46400, TMS46400P .....	- 0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	TMS44400, TMS44400P .....	- 1.0 V to 7.0 V
	TMS46400, TMS46400P .....	- 0.5 V to 4.6 V
Short-circuit output current .....		50 mA
Power dissipation .....		1 W
Operating free-air temperature range, $T_A$ .....		0°C to 70°C
Storage temperature range, $T_{stg}$ .....		- 55°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

recommended operating conditions

		TMS44400/P			TMS46400/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
$V_{IH}$	High-level input voltage	2.4		6.5	2		$V_{CC} + 0.3$	V
$V_{IL}$	Low-level input voltage (see Note 2)	- 1		0.8	- 0.3		0.8	V
$T_A$	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'44400-60 '44400P-60		'44400-70 '44400P-70		'44400-80 '44400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA		2.4		2.4		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		0.4		V
I <sub>I</sub>	Input current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V, All others = 0 V to V <sub>CC</sub>		± 10		± 10		µA
I <sub>O</sub>	Output current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> , CAS high		± 10		± 10		µA
I <sub>CC1</sub>	Read- or write-cycle current (see Note 3)	V <sub>CC</sub> = 5.5 V, Minimum cycle		105		90		80 mA
I <sub>CC2</sub>	Standby current	After one memory cycle, RAS and CAS high, V <sub>IH</sub> = 2.4 V (TTL)		2		2		2 mA
		After one memory cycle, RAS and CAS high, V <sub>IH</sub> = V <sub>CC</sub> - 0.2 V (CMOS)	'44400	1		1		1 mA
		'44400P	500		500		500 µA	
I <sub>CC3</sub>	Average refresh current (RAS only or CBR) (see Note 4)	V <sub>CC</sub> = 5.5 V, Minimum cycle, RAS cycling, CAS high (RAS only); RAS low after CAS low (CBR)		105		90		80 mA
I <sub>CC4</sub>	Average page current (see Notes 3 and 5)	V <sub>CC</sub> = 5.5 V, t <sub>PC</sub> = MIN, RAS low, CAS cycling		90		80		70 mA
I <sub>CC6</sub> <sup>†</sup>	Self-refresh current (see Note 3)	CAS ≤ 0.2 V, RAS < 0.2 V, t <sub>RAS</sub> and t <sub>CAS</sub> > 1000 ms		500		500		500 µA
I <sub>CC7</sub>	Standby current, outputs enabled (see Note 3)	RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> , Data out = enabled		5		5		5 mA
I <sub>CC10</sub> <sup>†</sup>	Battery-backup current (with CBR)	t <sub>RC</sub> = 125 µs, t <sub>RAS</sub> ≤ 1 ms, V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ 6.5 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V, W and OE = V <sub>IH</sub> , Address and data stable		500		500		500 µA

<sup>†</sup> For TMS44400P only

- NOTES: 3. I<sub>CC</sub> MAX is specified with no load connected.  
 4. Measured with a maximum of one address change while RAS = V<sub>IL</sub>  
 5. Measured with a maximum of one address change while CAS = V<sub>IH</sub>

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'46400-60 '46400P-60		'46400-70 '46400P-70		'46400-80 '46400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -2 mA (LVTTTL)		2.4		2.4		V
		I <sub>OH</sub> = -100 μA (LVCMOS)		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2 mA (LVTTTL)		0.4		0.4		V
		I <sub>OL</sub> = 100 μA (LVCMOS)		0.2		0.2		
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 3.9 V, V <sub>CC</sub> = 3.6 V, All others = 0 V to V <sub>CC</sub>		± 10		± 10		μA
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0 V to V <sub>CC</sub> , V <sub>CC</sub> = 3.6 V, <u>CAS</u> high		± 10		± 10		μA
I <sub>CC1</sub>	Read- or write-cycle current (see Note 3)	Minimum cycle, V <sub>CC</sub> = 3.6 V		70		60		50 mA
I <sub>CC2</sub>	Standby current	After one memory cycle, <u>RAS</u> and <u>CAS</u> high, V <sub>IH</sub> = 2 V (LVTTTL)		2		2		2 mA
		After one memory cycle, <u>RAS</u> and <u>CAS</u> high, V <sub>IH</sub> = V <sub>CC</sub> - 0.2 V (LVCMOS)	'46400	300		300		300 μA
			'46400P	200		200		200 μA
I <sub>CC3</sub>	Average refresh current ( <u>RAS</u> only or CBR) (see Note 4)	Minimum cycle, V <sub>CC</sub> = 3.6 V, <u>RAS</u> cycling, <u>CAS</u> high ( <u>RAS</u> only); <u>RAS</u> low after <u>CAS</u> low (CBR)		70		60		50 mA
I <sub>CC4</sub>	Average page current (see Notes 3 and 5)	t <sub>PC</sub> = MIN, V <sub>CC</sub> = 3.6 V, <u>RAS</u> low, <u>CAS</u> cycling		60		50		40 mA
I <sub>CC6</sub> <sup>†</sup>	Self-refresh current (see Note 3)	<u>CAS</u> ≤ 0.2 V, <u>RAS</u> < 0.2 V, t <sub>RAS</sub> and t <sub>CAS</sub> > 1000 ms		200		200		200 μA
I <sub>CC7</sub>	Standby current, outputs enabled (see Note 3)	<u>RAS</u> = V <sub>IH</sub> , <u>CAS</u> = V <sub>IL</sub> , Data out = enabled		5		5		5 mA
I <sub>CC10</sub> <sup>†</sup>	Battery-backup current (with CBR)	t <sub>RC</sub> = 125 μs, t <sub>RAS</sub> ≤ 1 ms, V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ 3.9 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V, <u>W</u> and <u>OE</u> = V <sub>IH</sub> , Address and data stable		300		300		300 μA

<sup>†</sup> For TMS46400P only

- NOTES: 3. I<sub>CC</sub> MAX is specified with no load connected.  
 4. Measured with a maximum of one address change while RAS = V<sub>IL</sub>  
 5. Measured with a maximum of one address change while CAS = V<sub>IH</sub>

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capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1$  MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
$C_o$	Output capacitance		7	pF

NOTE 6:  $V_{CC} = 5\text{ V} \pm .5\text{ V}$  for the TMS44400 devices,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  for the TMS46400 devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{AA}$	30		35		40	
$t_{CAC}$	15		18		20		ns
$t_{CPA}$	35		40		45		ns
$t_{RAC}$	60		70		80		ns
$t_{OEA}$	15		18		20		ns
$t_{CLZ}$	0		0		0		ns
$t_{OFF}$	0	15	0	18	0	20	ns
$t_{OEZ}$	0	15	0	18	0	20	ns

NOTE 7:  $t_{OFF}$  is specified when the output is no longer driven.

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### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x6400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Cycle time, random read or write (see Note 8)	110		130		150		ns
t <sub>RWC</sub>	Cycle time, read-write	155		181		205		ns
t <sub>PC</sub>	Cycle time, page-mode read or write (see Note 9)	40		45		50		ns
t <sub>PRWC</sub>	Cycle time, page-mode read-write	85		96		105		ns
t <sub>RASP</sub>	Pulse duration, $\overline{\text{RAS}}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub>	Pulse duration, $\overline{\text{RAS}}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t <sub>RASS</sub>	Pulse duration, $\overline{\text{RAS}}$ low, self refresh	100		100		100		μs
t <sub>CAS</sub>	Pulse duration, $\overline{\text{CAS}}$ low (see Note 11)	10	10 000	18	10 000	20	10 000	ns
t <sub>CP</sub>	Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t <sub>RP</sub>	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>RPS</sub>	Precharge time after self refresh using $\overline{\text{RAS}}$	110		130		150		ns
t <sub>WP</sub>	Pulse duration, write	10		10		10		ns
t <sub>ASC</sub>	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub>	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub>	Setup time, data (see Note 12)	0		0		0		ns
t <sub>RCS</sub>	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	15		18		20		ns
t <sub>RWL</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>WCS</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low (early-write operation only)	0		0		0		ns
t <sub>WSR</sub>	Setup time, $\overline{\text{W}}$ high ( $\overline{\text{CBR}}$ refresh only)	10		10		10		ns
t <sub>WTS</sub>	Setup time, $\overline{\text{W}}$ low (test mode only)	10		10		10		ns
t <sub>CAH</sub>	Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DHR</sub>	Hold time, data after $\overline{\text{RAS}}$ low (see Note 13)	50		55		60		ns
t <sub>DH</sub>	Hold time, data (see Note 12)	10		15		15		ns
t <sub>AR</sub>	Hold time, column address after $\overline{\text{RAS}}$ low (see Note 13)	50		55		60		ns
t <sub>RAH</sub>	Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 14)	0		0		0		ns
t <sub>RRH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 14)	0		0		0		ns
t <sub>WCH</sub>	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low (early-write operation only)	10		15		15		ns
t <sub>WCR</sub>	Hold time, $\overline{\text{W}}$ low after $\overline{\text{RAS}}$ low (see Note 13)	50		55		60		ns
t <sub>WHR</sub>	Hold time, $\overline{\text{W}}$ high ( $\overline{\text{CBR}}$ refresh only)	10		10		10		ns
t <sub>WTH</sub>	Hold time, $\overline{\text{W}}$ low (test mode only)	10		10		10		ns
t <sub>CHS</sub>	Hold time, $\overline{\text{CAS}}$ low after $\overline{\text{RAS}}$ high (self refresh)	- 50		- 50		- 50		ns
t <sub>OEH</sub>	Hold time, $\overline{\text{OE}}$ command	15		18		20		ns
t <sub>OED</sub>	Hold time, $\overline{\text{OE}}$ to data delay	15		18		20		ns

NOTES: 8. All cycle times assume  $t_T = 5$  ns.

9. To ensure  $t_{PC}$  min,  $t_{ASC}$  should be  $\geq t_{CP}$ .

10. In a read-write cycle,  $t_{RWD}$  and  $t_{RWL}$  must be observed.

11. In a read-write cycle,  $t_{CWD}$  and  $t_{CWL}$  must be observed.

12. Referenced to the later of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  in write operations

13. The minimum value is measured when  $t_{RCD}$  is set to  $t_{RCD}$  min as a reference.

14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.

TMS44400, TMS44400P, TMS46400, TMS46400P  
 1048576-WORD BY 4-BIT  
 DYNAMIC RANDOM-ACCESS MEMORIES

SMHS562C – MAY 1995 – REVISED NOVEMBER 1996

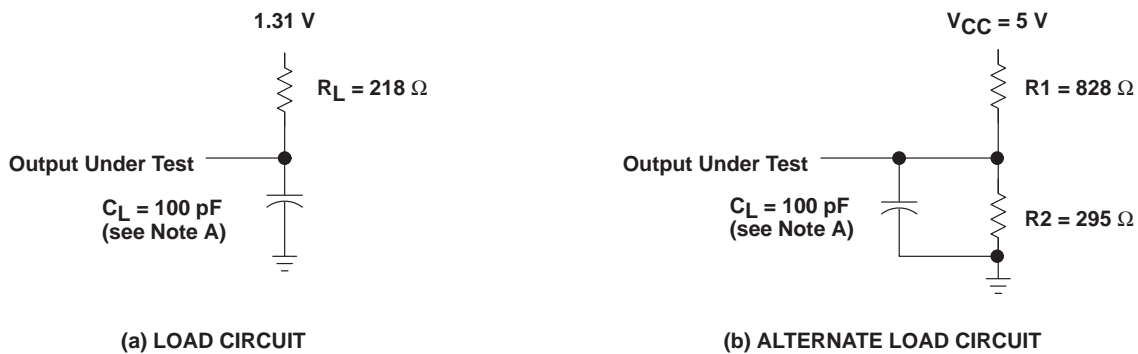
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>ROH</sub>	Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$	10		10		10		ns
t <sub>AWD</sub>	Delay time, column address to $\overline{\text{W}}$ low (read-write operation only)	55		63		70		ns
t <sub>CHR</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t <sub>CRP</sub>	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>CSH</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t <sub>CSR</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t <sub>CWD</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (read-write operation only)	40		46		50		ns
t <sub>RAD</sub>	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 15)	15	30	15	35	15	40	ns
t <sub>RAL</sub>	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t <sub>CAL</sub>	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t <sub>RCD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 15)	20	45	20	52	20	60	ns
t <sub>RPC</sub>	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>RSH</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>RWD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (read-write operation only)	85		98		110		ns
t <sub>TAA</sub>	Access time from address (test mode)	35		40		45		ns
t <sub>TCPA</sub>	Access time from column precharge (test mode)	40		45		50		ns
t <sub>TRAC</sub>	Access time from $\overline{\text{RAS}}$ (test mode)	65		75		85		ns
t <sub>REF</sub>	Refresh time interval	'4x400				16		ms
		'4x400P				128		ms
t <sub>T</sub>	Transition time	2	30	2	30	2	30	ns

NOTE 15: The maximum value is specified only to ensure access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: C<sub>L</sub> includes probe and fixture capacitance.

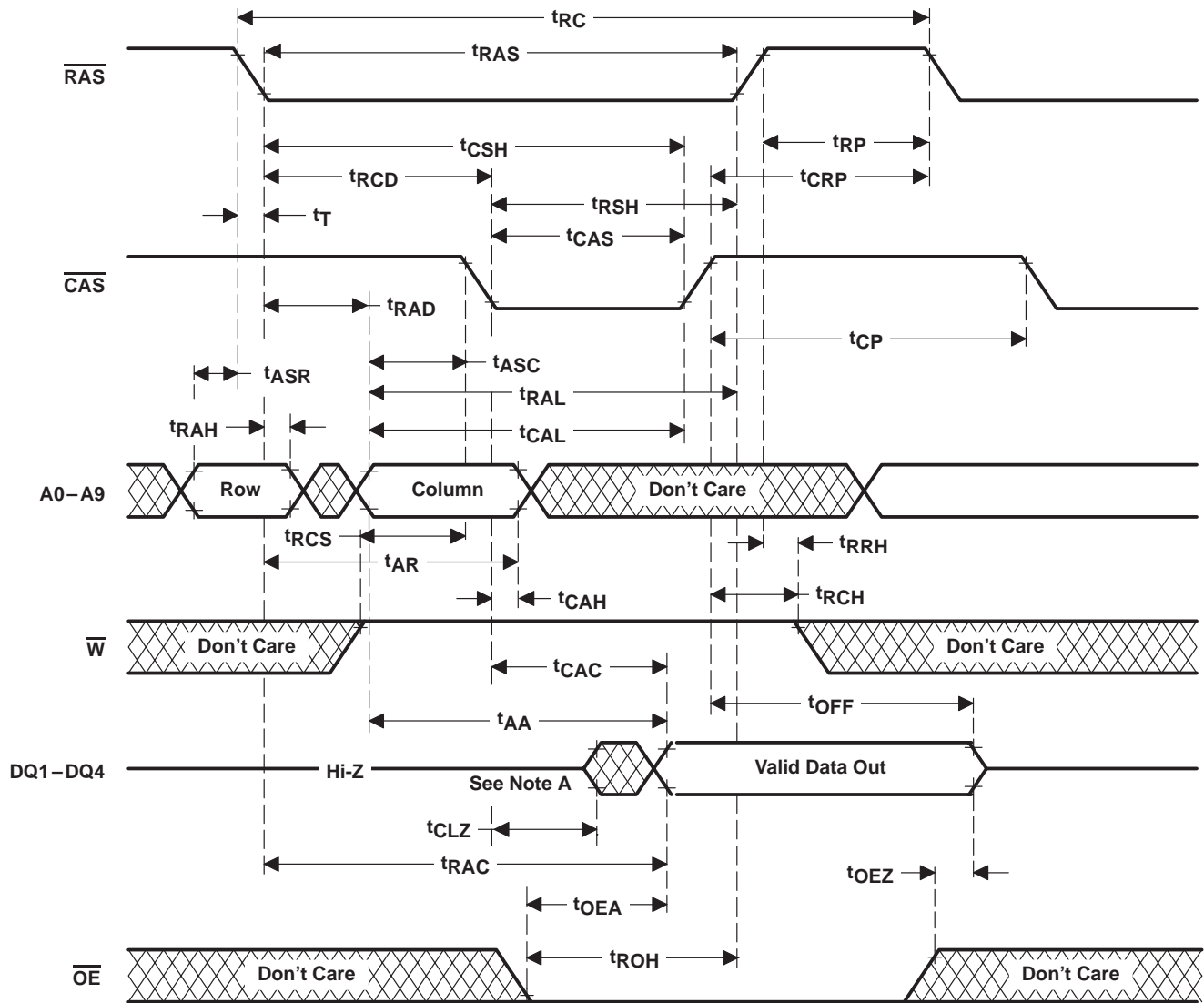
Figure 2. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and fixture capacitance.

Figure 3. Low-Voltage Load Circuits for Timing Parameters



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 4. Read-Cycle Timing

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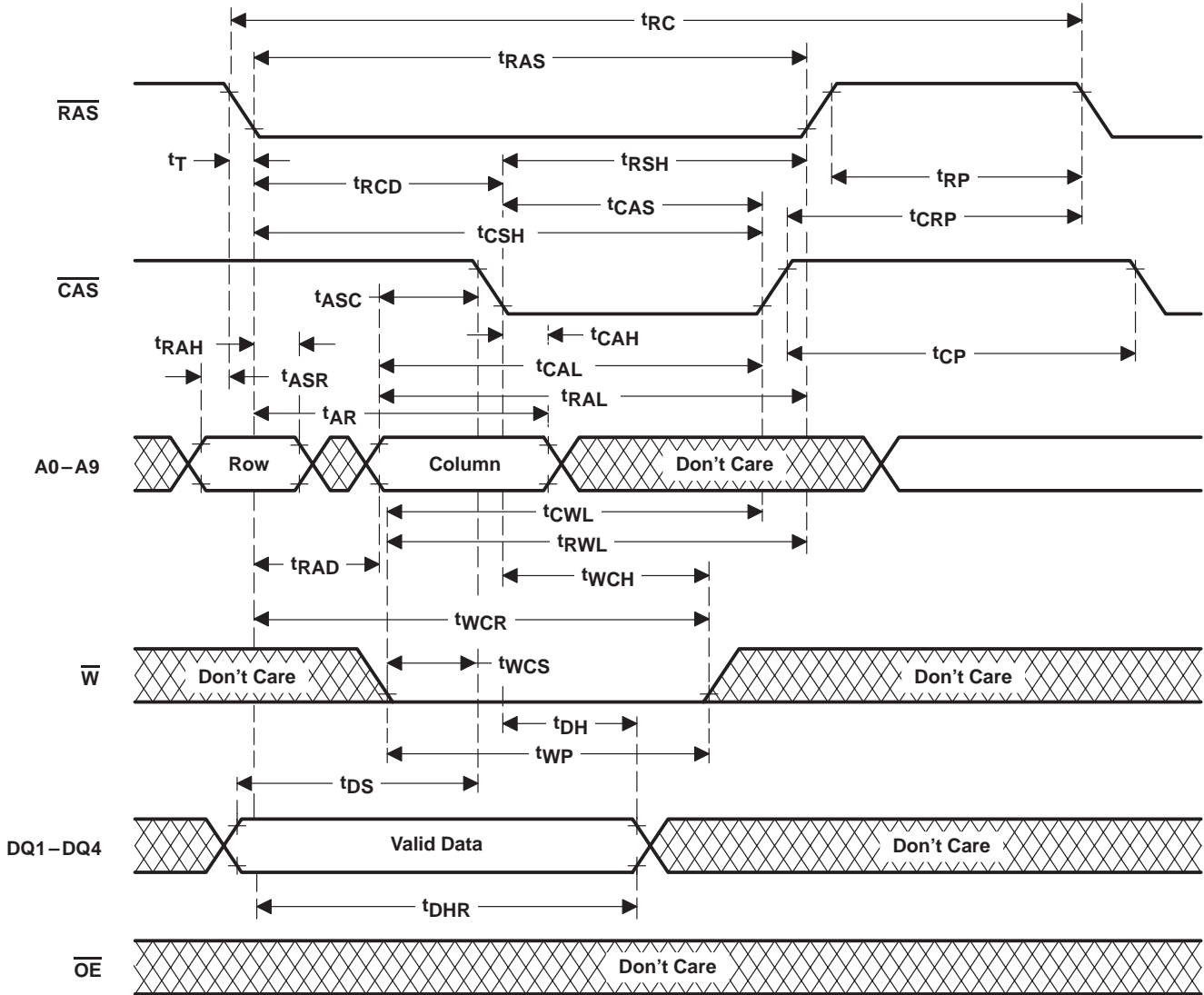


Figure 5. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

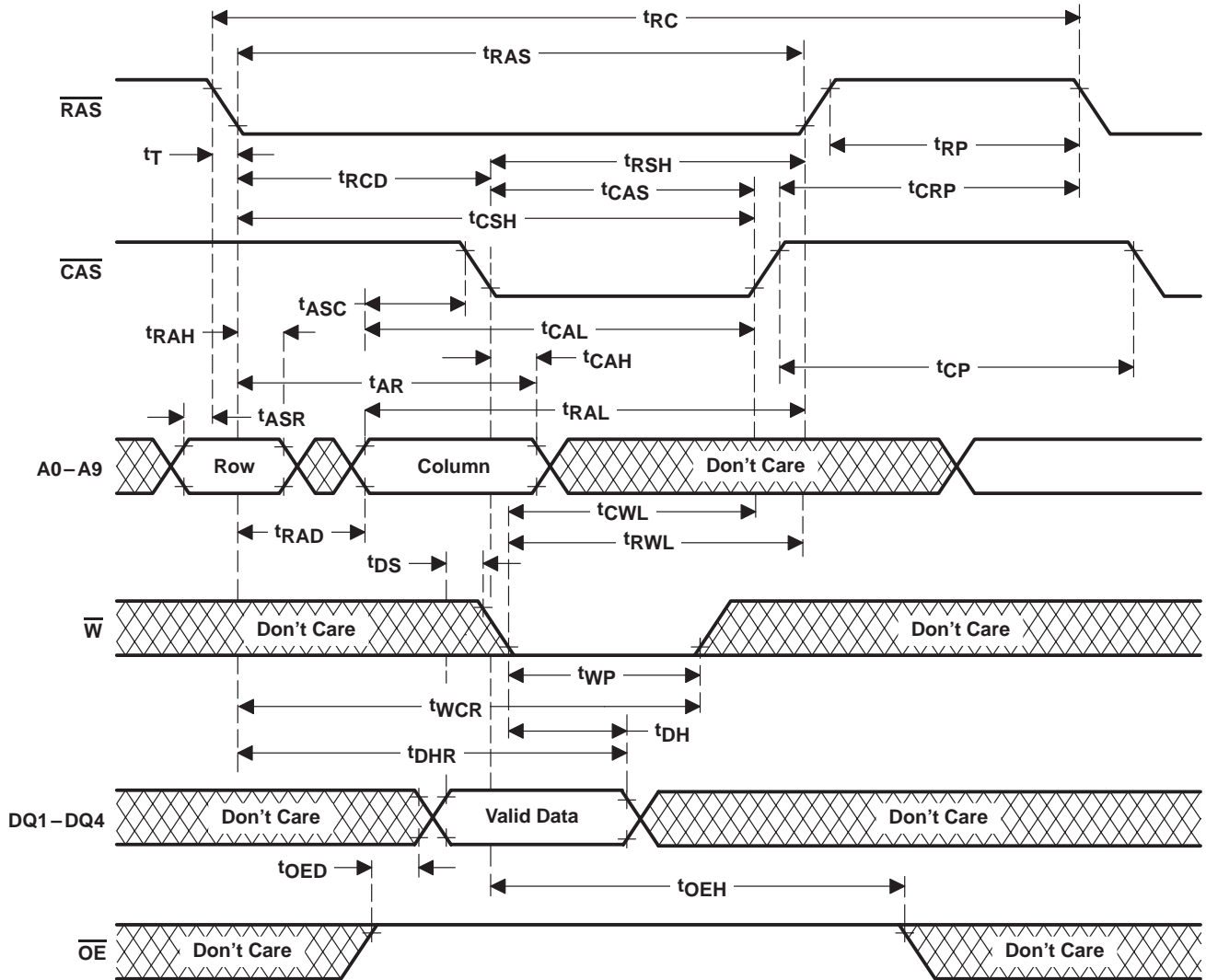
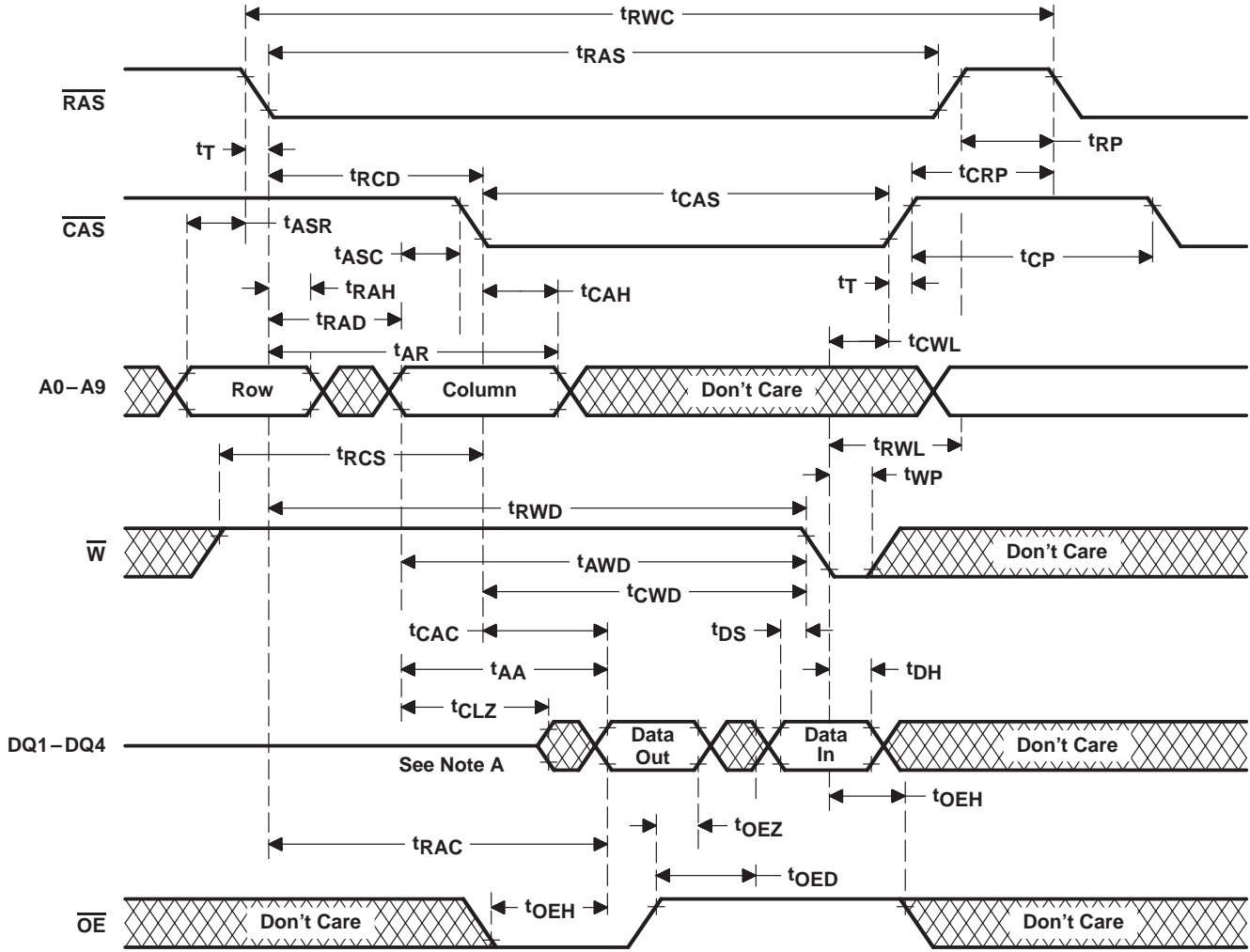


Figure 6. Write-Cycle Timing

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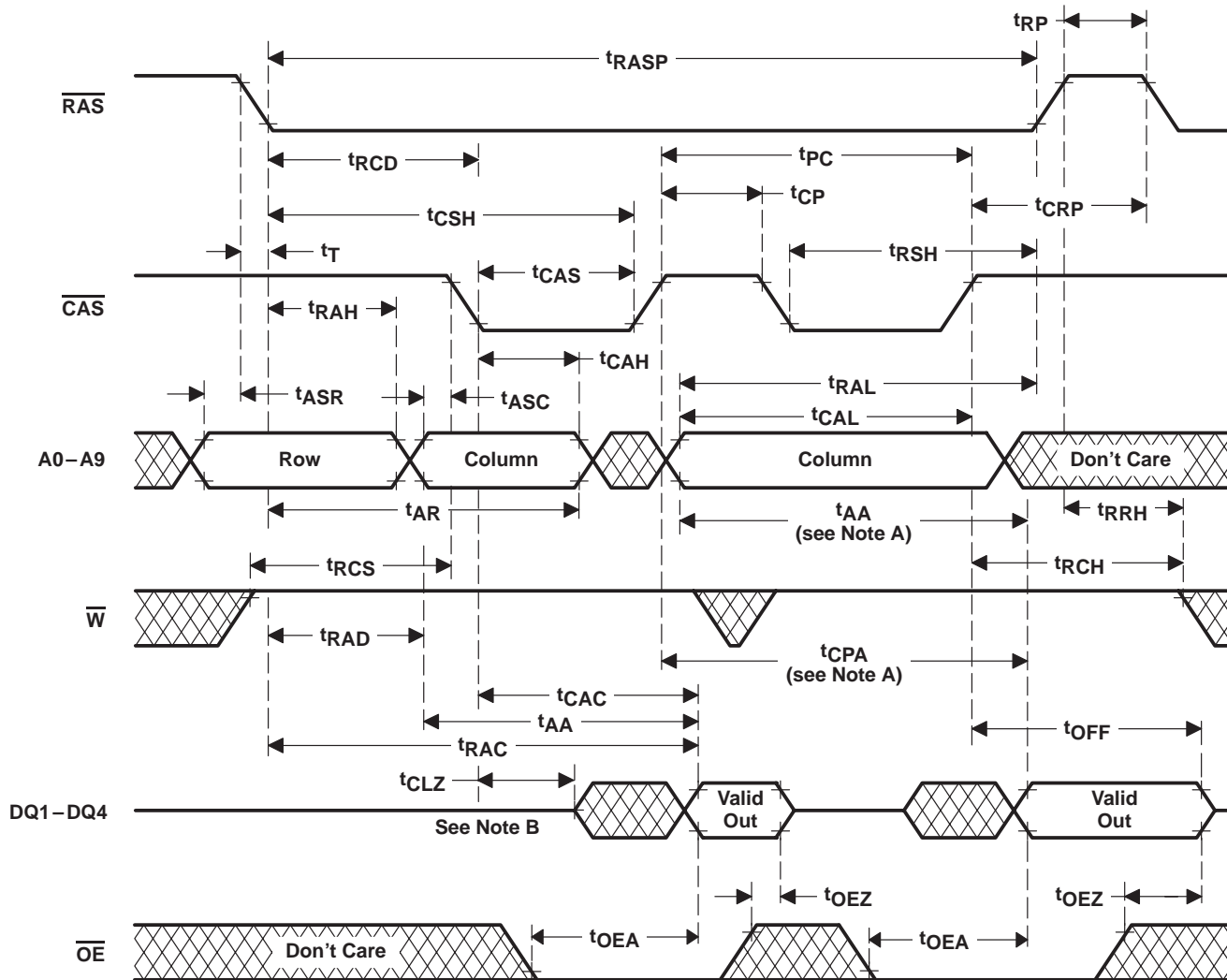
ADVANCE INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



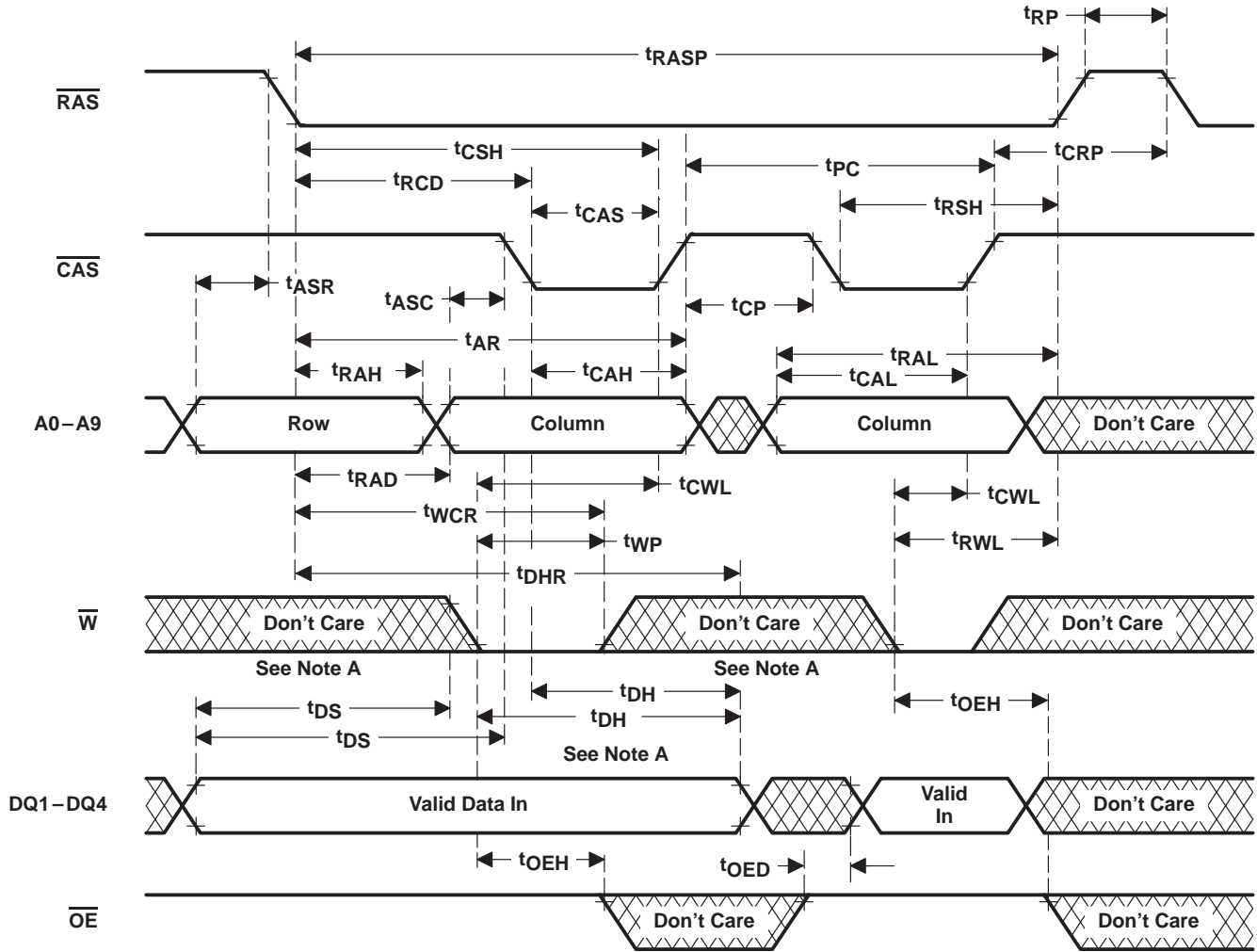
- NOTES: A. Access time is  $t_{\text{CPA}}$  or  $t_{\text{AA}}$  dependent.  
 B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 8. Enhanced-Page-Mode Read-Cycle Timing

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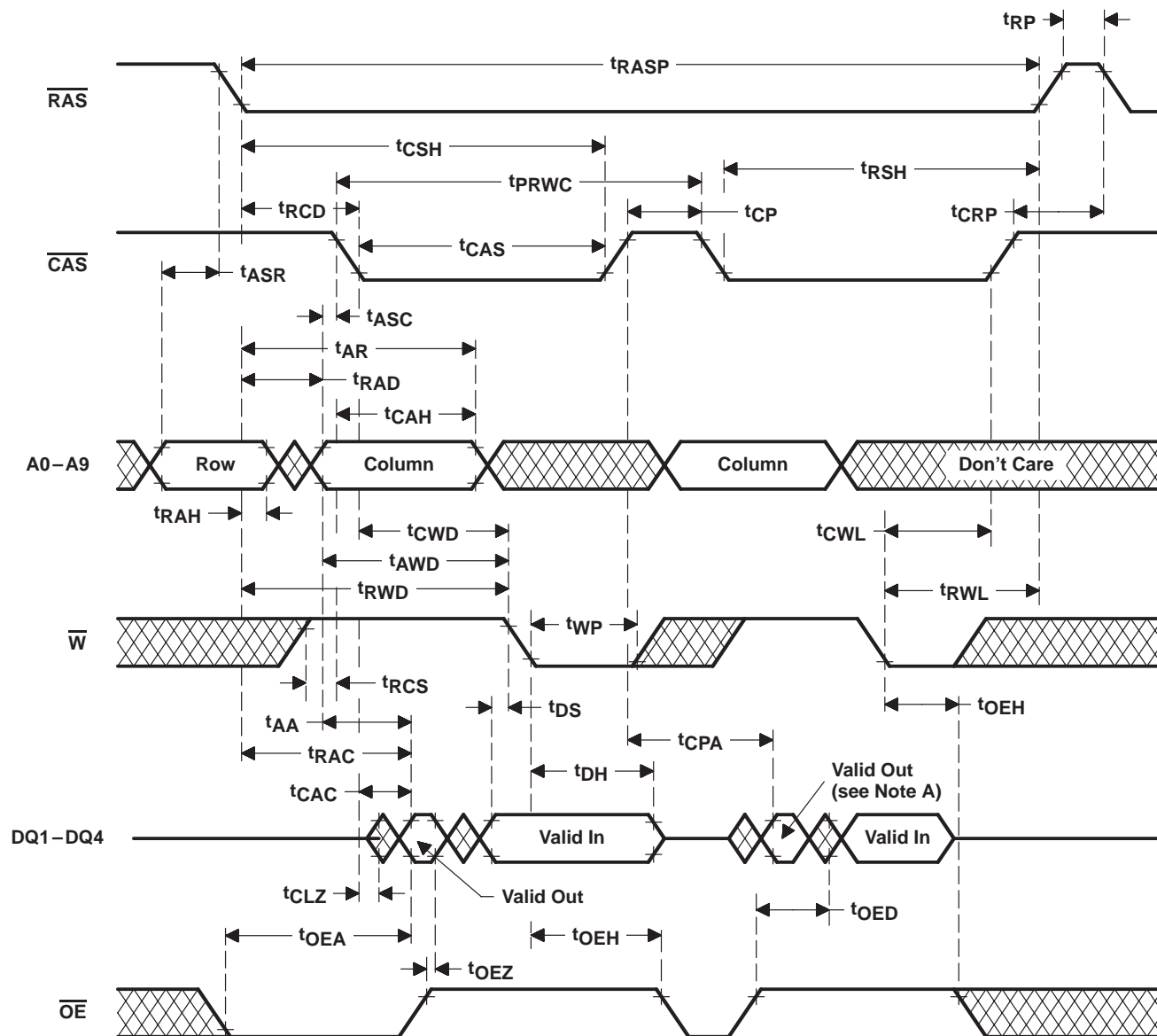


- NOTES: A. Referenced to  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$ , whichever occurs last  
 B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Write-Cycle Timing



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
- B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 10. Enhanced-Page-Mode Read-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

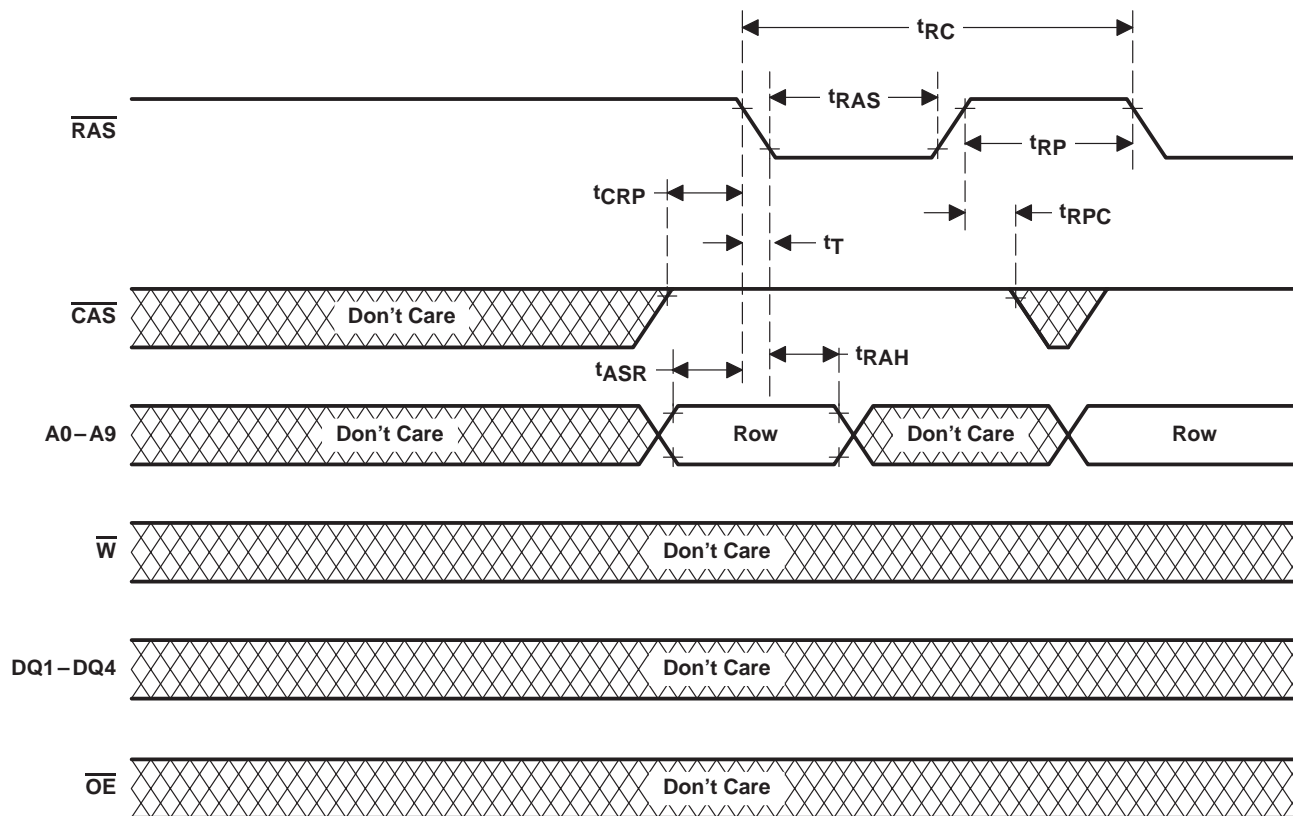


Figure 11. RAS-Only Refresh-Cycle Timing

ADVANCE INFORMATION

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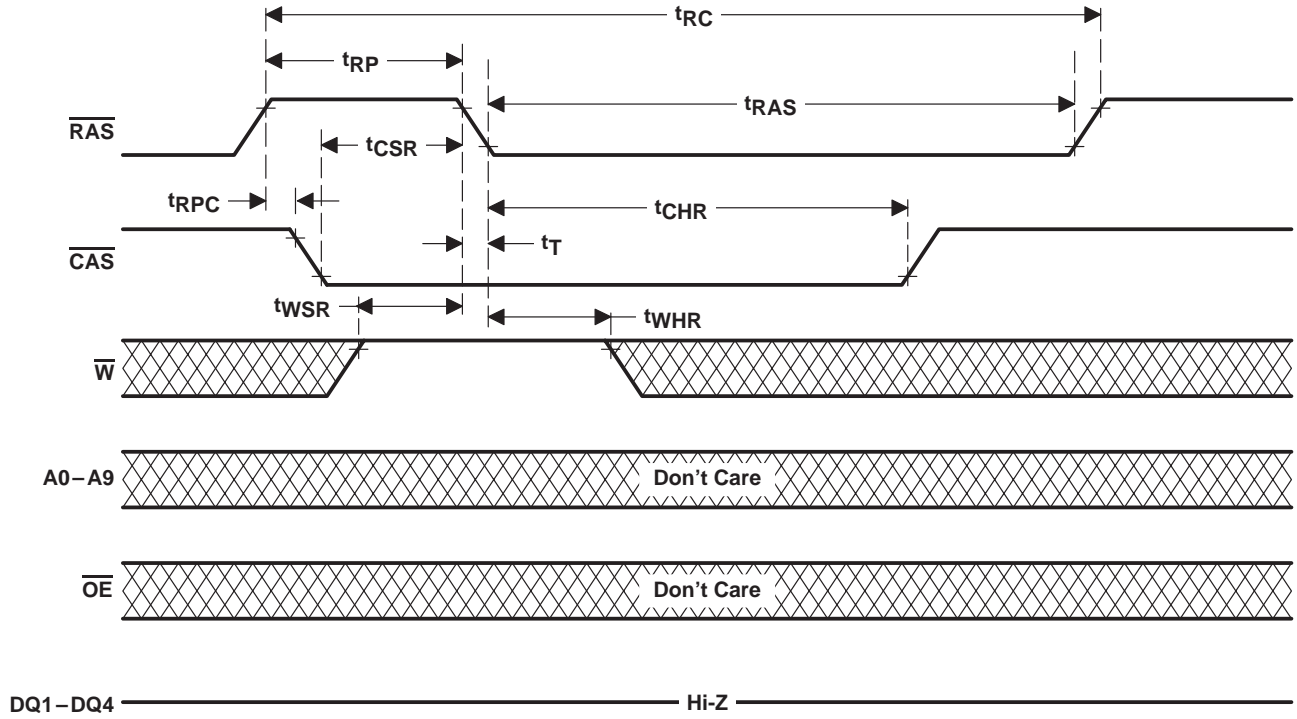


Figure 12. Automatic-CBR-Refresh-Cycle Timing

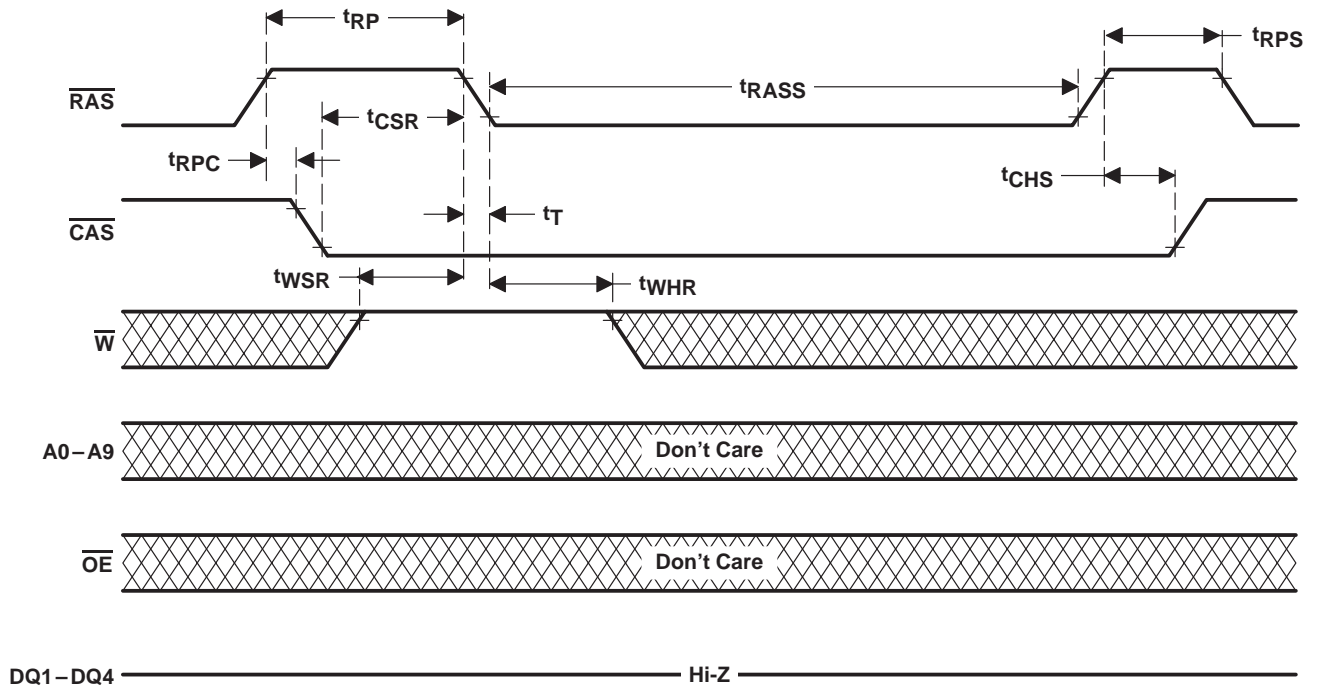


Figure 13. Self-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

ADVANCE INFORMATION

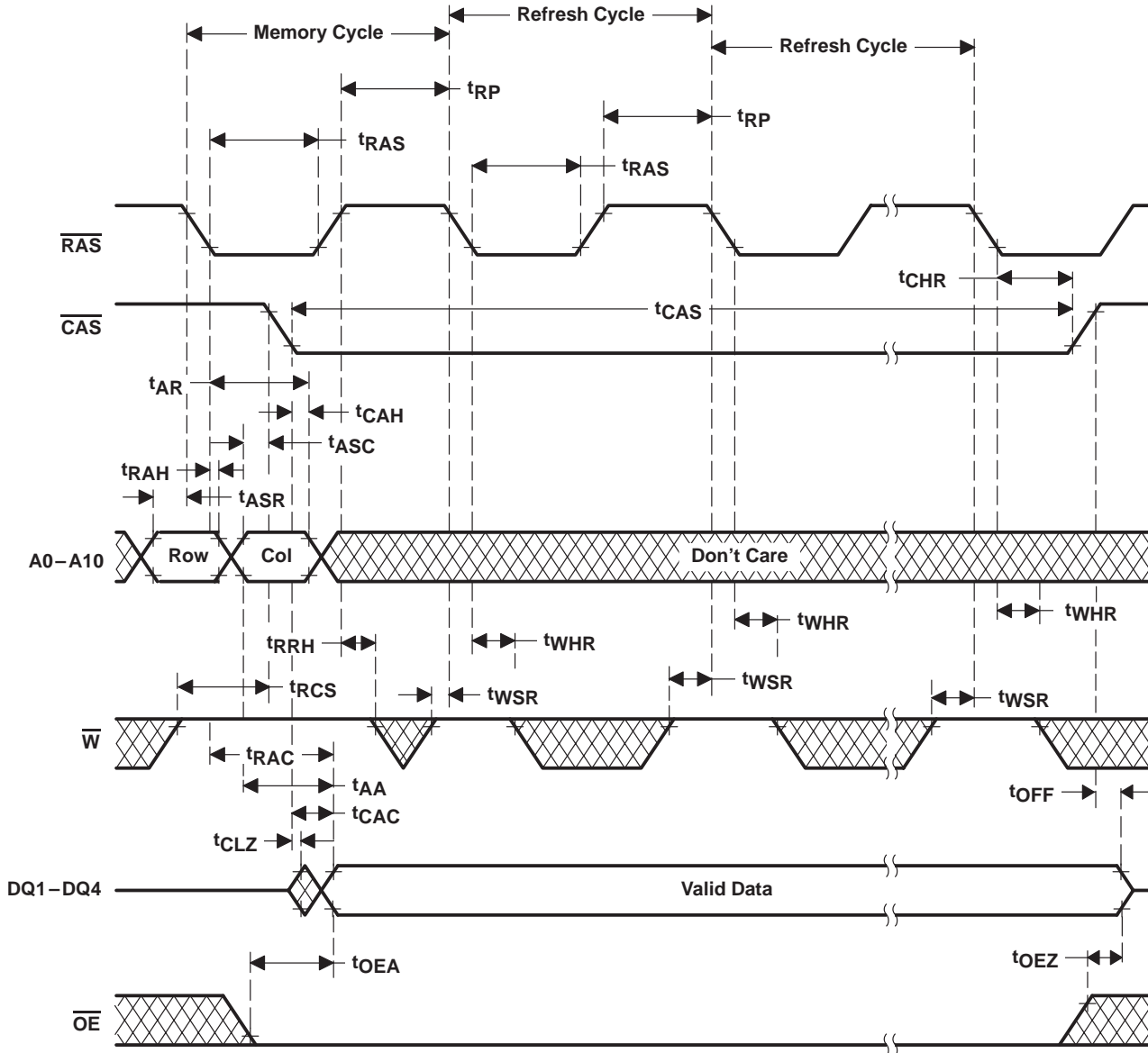


Figure 14. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

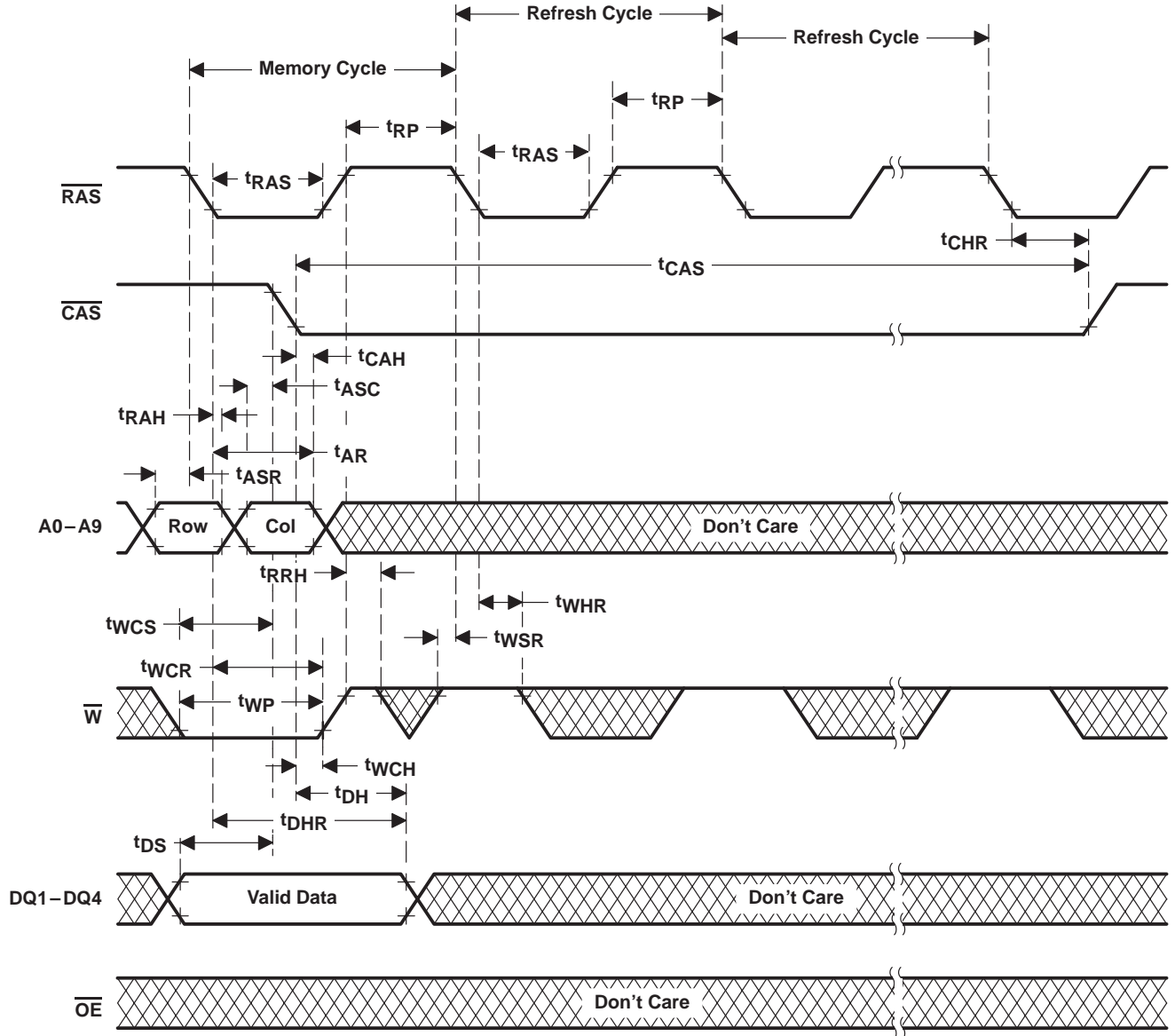


Figure 15. Hidden-Refresh-Cycle (Write) Timing

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PARAMETER MEASUREMENT INFORMATION

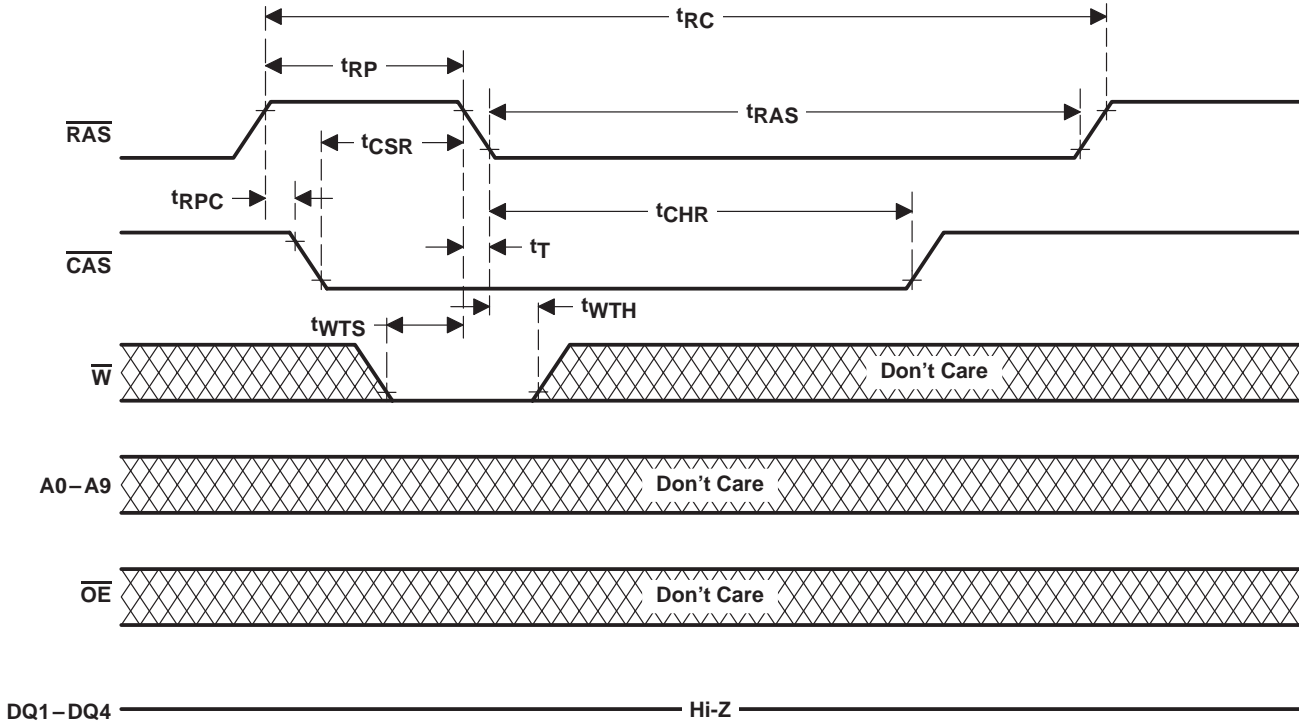
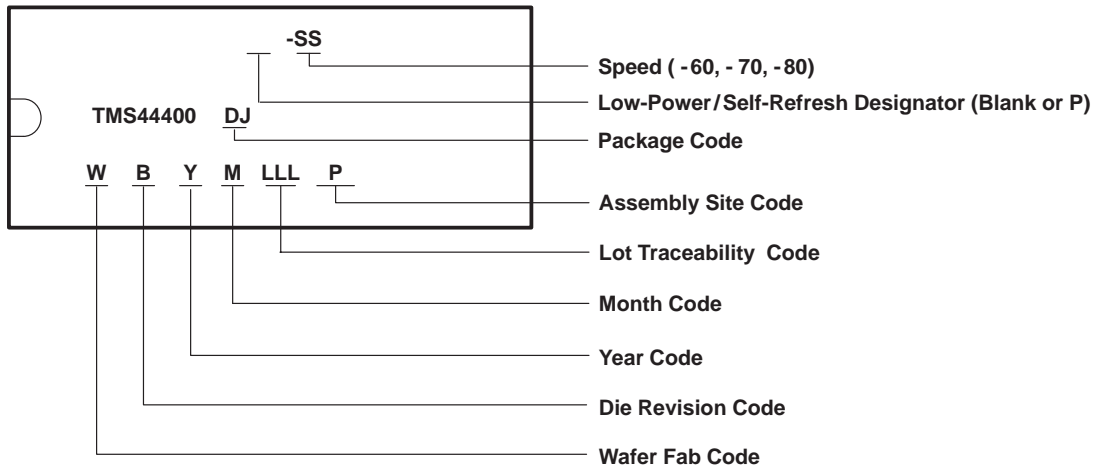


Figure 16. Test-Mode Entry-Cycle Timing

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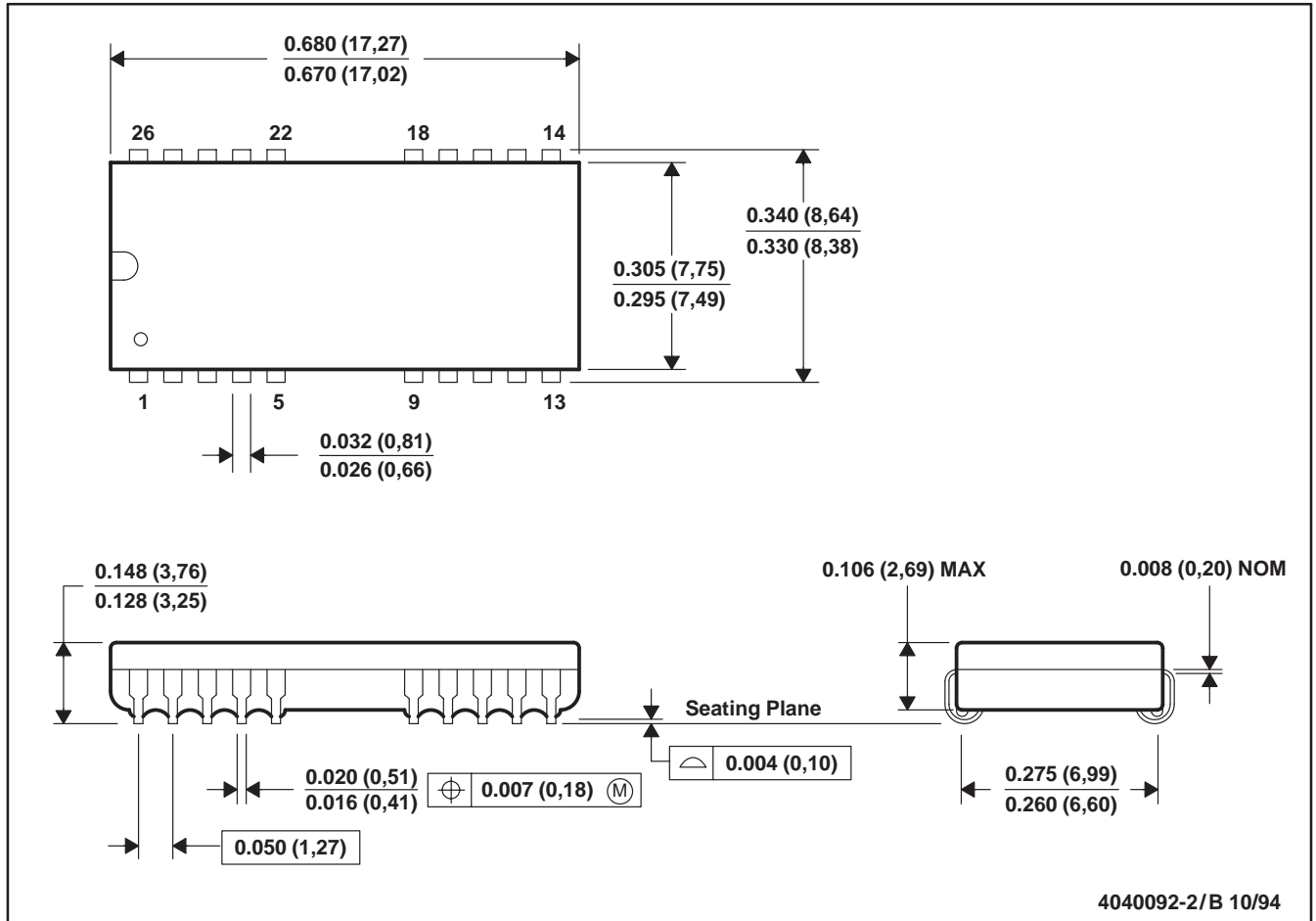
device symbolization (TMS44400 illustrated)



PARAMETER MEASUREMENT INFORMATION

DJ (R-PDSO-J20/26)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

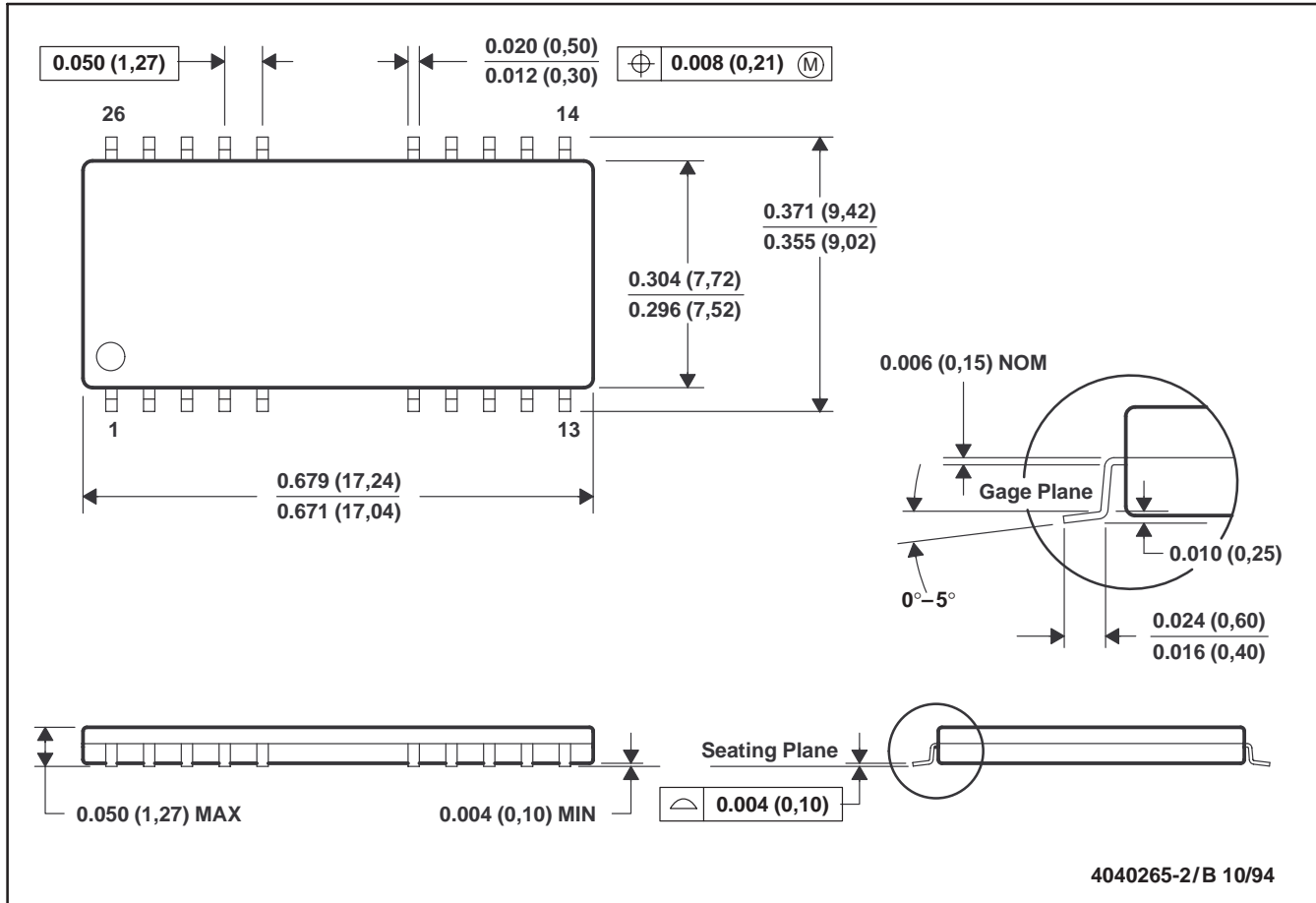
ADVANCE INFORMATION

MECHANICAL DATA

DGA (R-PDSO-G20/26)

PLASTIC SMALL-OUTLINE PACKAGE

ADVANCE INFORMATION



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.



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