TC1920

32-Bit Single-Chip Microcontroller

Draft

32bit

Microcontrollers

Infineon technologies

Never stop thinking.

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Page	**Subjects (major changes since last revision)**

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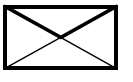

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1 Introduction

The TC1920 offers a 32bit TriCore based microcontroller/DSP, which is mainly designed for automotive telematics applications. Due to its high integration, this microcontroller/DSP offers high system performance at minimised cost. Typical telematics functions processed by RISC-, DSP- and speech- (CODEC) modules are now combined in one component. The combination of dedicated automotive peripherals (CAN, J1850) and standard peripherals (ADC, SSC/SPI, ASC and IIC), makes this microcontroller/DSP the engine tailored for a wide variety of telematics applications such as navigation, emergency call, speech interface or communication interface.

1.1 TC1920 Features:

- TriCore V1.3:
  - 100MHz internal clock
  - 32-bit super-scalar TriCore main CPU
  - 4-GByte unified memory space support
  - Fast context-switching
  - Dual 16 x 16 Multiply-accumulate (MAC) unit
  - 64-bit Local Memory Bus (LMB)
  - 32-bit Flexible Peripheral Interface (FPI)
  - 32-bit wide external bus unit (EBU)
- 32-bit Peripheral Control Processor (PCP2) with DMA-support
- 164kB on-chip SRAM
- Product Specific Peripherals:
  - 14-bit double CODEC with flexible sample rates and FIFO support
- Automotive Peripherals:
  - Two independent CAN-nodes (TwinCAN) with gateway support
  - J1850 (SDLM)
- Standard Peripherals:
  - 6-channel, 8-/10-/12-bit ADC
  - 3x asynchr. serial interface (ASC) with IrDa-support
  - 1 SPI-compatible synchr. serial interface @10Mbit (SSC)
  - 2-channel IIC
  - 6x 32 bit timer
  - ≥ 16 I/O- and interrupt pins (GPIO)
- General Peripherals:
  - Real time clock (RTC)
  - Watchdog timer(WDT)
- PLL with 3.1 MHz to 37.5 MHz input
- Debug Support:
  - Debug Interface (OCDS level 2) with Trace Port
- Power saving features

- Dual voltage supply (1.8V core, 3.3V I/O)
- 40°C to +85°C temperature range
- LBGA-256 package
- Supported RTOS: VxWorks

1.2 Block Diagram

The figure below shows the block diagram of the TC1920 device.

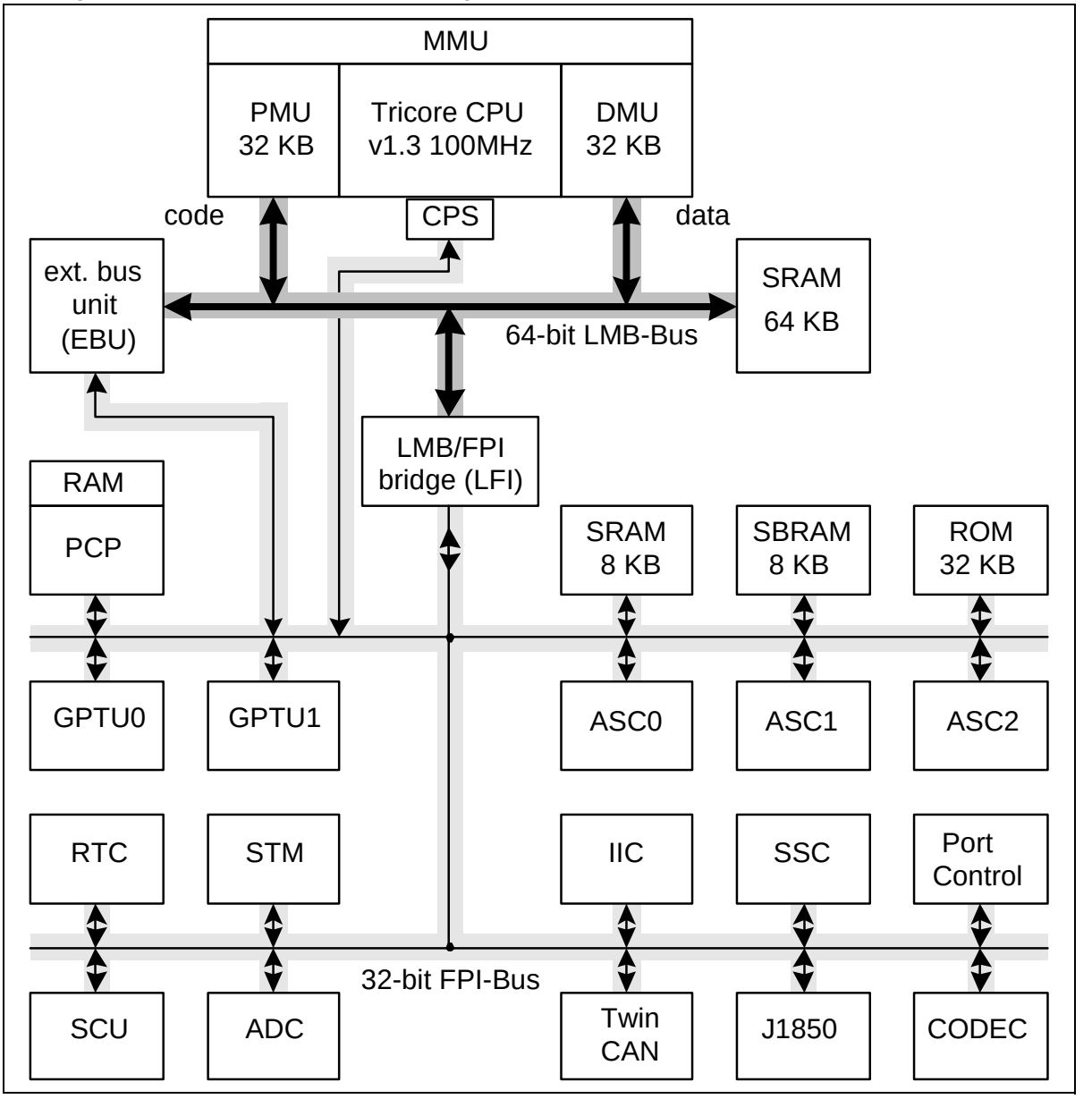

Figure 1-1 TC1920 Device Block Diagram

1.3 Target applications:

- On-board and off-board navigation
- Emergency call systems
- Car speech interface
- Car communication interface
- Gateways: automotive - infotainment
- Occupant Sensing
- Drowsiness detection
- Rear- & side-mirror replacement
- Pre-crash sensing

1.4 Logical Symbol

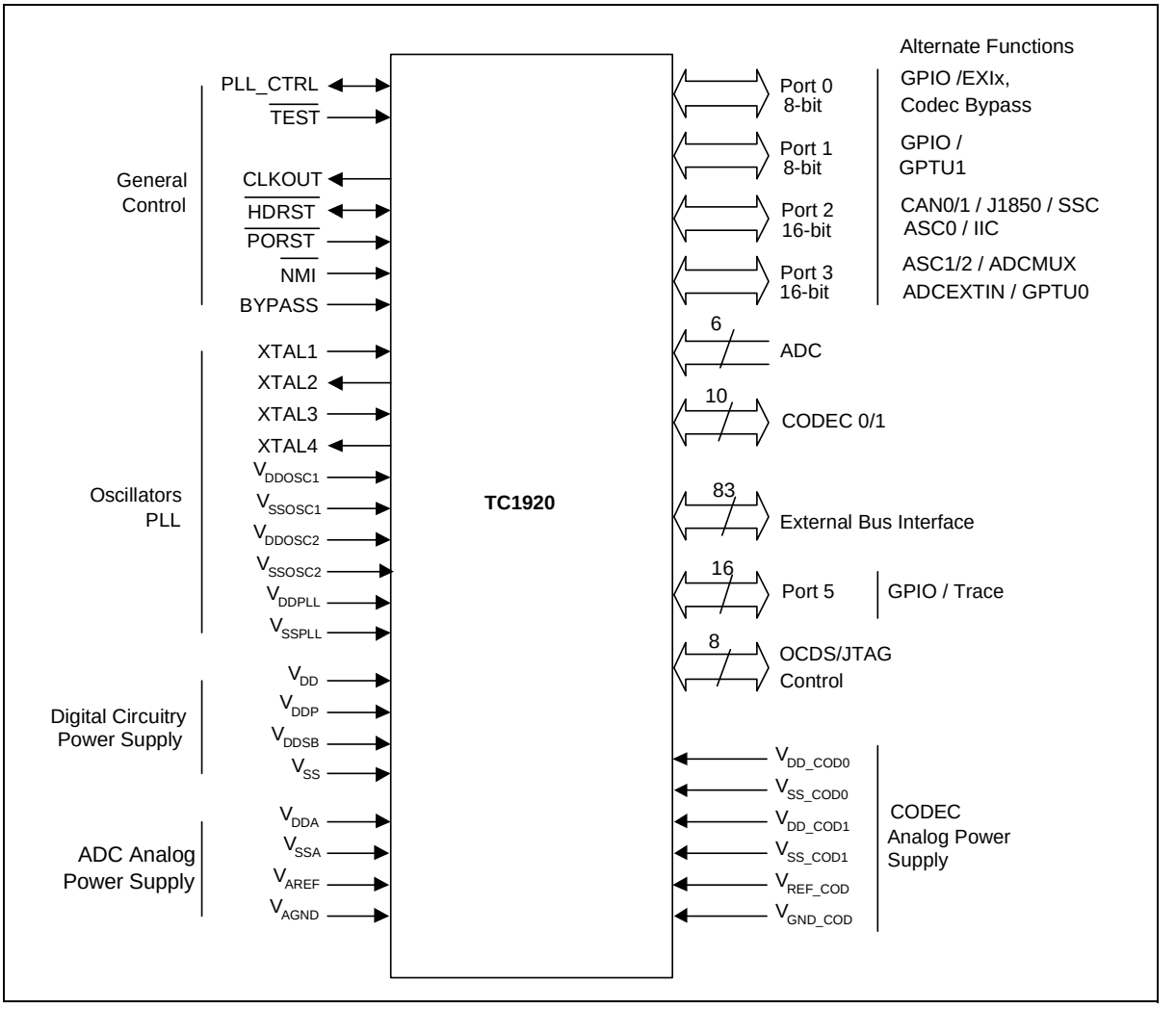

Figure 1-2 Logical Symbol of the TC1920 Device

2 System Architecture and Control

2.1 32-Bit TriCore CPU

- 32-bit architecture with 4-GByte unified data, program and input/output address space
- Fast automatic context-switch
- Dual 16 x 16 Multiply-accumulate (MAC) unit
- Saturating integer arithmetic
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

Instruction Set with High Efficiency:

- 16/32-bit instructions for reduced code size
- Little endian byte ordering with support for big and little endian byte ordering at bus interface
- Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double word integers and IEEE-754 single precision floating-point data types
- Bit, 8-bit byte, 16-bit half word, 32-bit word and 64-bit double word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

2.2 On-chip Memory

2.2.1 Code Memories

PMU Scratch-Pad SRAM (CSRAM):

The CSRAM is a 32-KByte static RAM which can be configured in 2 modes. It can be used as Code Scratchpad RAM (CSRAM) and as Instruction Cache (ICACHE).

Address range of PMU Scratch-Pad SRAM:

- $D400\ 0000_H$ - $D400\ 7FFF_H$

Local Memory Bus Code Memory (LMBRAM):

Address range of the 64 KByte Local Memory Bus Code Memory:

- $C000\ 0000_H$ - $C000\ FFFF_H$ (in segment 12 for cached operation)
- $E800\ 0000_H$ - $E800\ FFFF_H$ (in segment 14 for non-cached operation)

Boot ROM (BROM):

The TC1920 contains 32 KByte of Boot ROM memory, which can be used for device operating mode initialization routines, bootstrap loader support or test functions.

The address range of the Boot ROM is:

- DFFF 8000_H – DFFF $FFFF_H$

2.2.2 Data Memories

DMU Scratch-Pad SRAM (DSRAM):

The DSRAM is a 32-KByte static RAM which can be configured in 3 modes. It can be used as Data Scratchpad RAM (DSRAM) and as Data Cache (DCACHE).

Address range of DMU Scratch-Pad SRAM:

- D000 0000_H - D000 $7FFF_H$

FPI-Bus Data Memory (FPIDRAM):

The 16 KByte FPI-Bus Data Memory (FPIDRAM) is located on the FPI-Bus. It contains two parts: FPIDRAM0 and FPIDRAM1. One half of it (FPIDRAM1) can be used for standby power operation.

Address range of FPI Data Memory:

- BFFF 8000_H - BFFF $BFFF_H$ (in segment 9 for cached operation)
- 9FFF 8000_H - 9FFF $BFFF_H$ (in segment 11 for non-cached operation)

2.2.3 PCP Memories

PCP Code Memory (PCODE):

The address range of the 16 KByte PCP Code Memory (PCODE) is:

- F002 0000_H - F002 $3FFF_H$

PCP Data Memory (PRAM):

The address range of the 4 KByte PCP Data Memory (PRAM) is:

- F001 0000_H - F001 $0FFF_H$

2.3 System Control Unit (SCU)

The System Control Unit of the TC1920 basically handles all system control tasks. All these system functions are tightly coupled and therefore they are handled physically by one unit, the SCU. The system tasks of the SCU are:

- Clock Generation and Control (system clock and RTC clock, clock distribution)
- Reset control
- Power Management control and wake-up
- Watchdog timer
- Trace port control
- Device identification
- Standby SRAM control
- External interrupt capability (8 sources)

2.4 System timer (STM)

The System Timer is designed for global system timing applications requiring both high precision and long range. It is used by the CPU for software operating system issues.

Features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock, f_{STM} (normally identical with the system clock).
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

2.5 External Bus Interface (EBU_LMB)

EBU_LMB is connected to the Local Memory Bus (LMB) of the TC1.3 and also to the FPI Bus. EBU_LMB is always a slave on the LMB and always a master on the FPI. The LMB is a 64-bit implementation of the FPI bus with slight modifications. Most of the signals and transfer types are identical to FPI Bus.

Any LMB masters thus can access external memories or devices through EBU_LMB. Currently the maximum length of the bursts are according to the size of program and data cache lines, i.e. 8 x32-bit words. EBU_LMB also supports shorter bursts of 4 and 2 of 32-bit words. Single transfers (non-burst) are supported for 8-bit, 16-bit and 32-bit wide access.

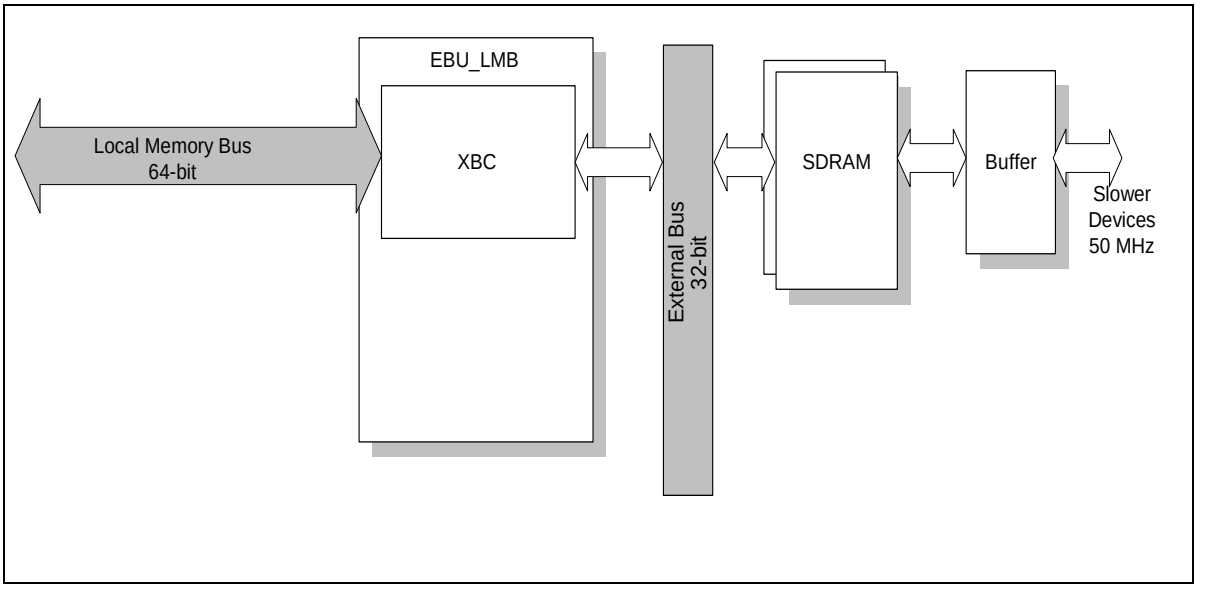

Figure 2-1 EBU_LMB block diagram

Features:

- Local Memory Bus (LMB 64-bit) support
- External bus frequency up to 100 MHz
- Internal LMB frequency up to 100 MHz
- External bus frequency : LMB frequency = 1:1 or 1:2 or 1:4
- Highly programmable access parameters
- Intel- and Motorola-style peripherals/devices support
- PC 100 SDRAM support (burst access, multibanking, precharge, refresh)
- 16- and 32-bit SDRAM data bus and support of 64, 128 and 256MBit devices
- Burst flash support (e.g. Intel 28F800F3/160F3, AMD 29BL162)
- Multiplexed access (address & data on the same bus) when PC100 is not used
- Data Buffering : Code Prefetch Buffer, Read/Write Buffer.
- External master arbitration compatible to C166 and other Tricore devices
- 8 programmable address regions (1 dedicated for emulator)
- Little- and Big-endian support
- CSglb signal, dedicated pin, bit programmable to combine one or more $\overline{CS}$ lines, for buffer control
- $\overline{LOCK}$ signal reflecting a read-modify-write action
- Signal for controlling data flow of slow-memory buffer
- Slave unit for external (off-chip) master to access devices on FPI bus
- Data Mover Engine (see EBU_LMB specification for more details)

2.6 Interrupt System

- Flexible interrupt prioritizing scheme with 256 interrupt priority levels
- Fast interrupt response
- Service requests are serviced by the CPU or by the PCP (two independent interrupt buses, that can be selected by each interrupt source)

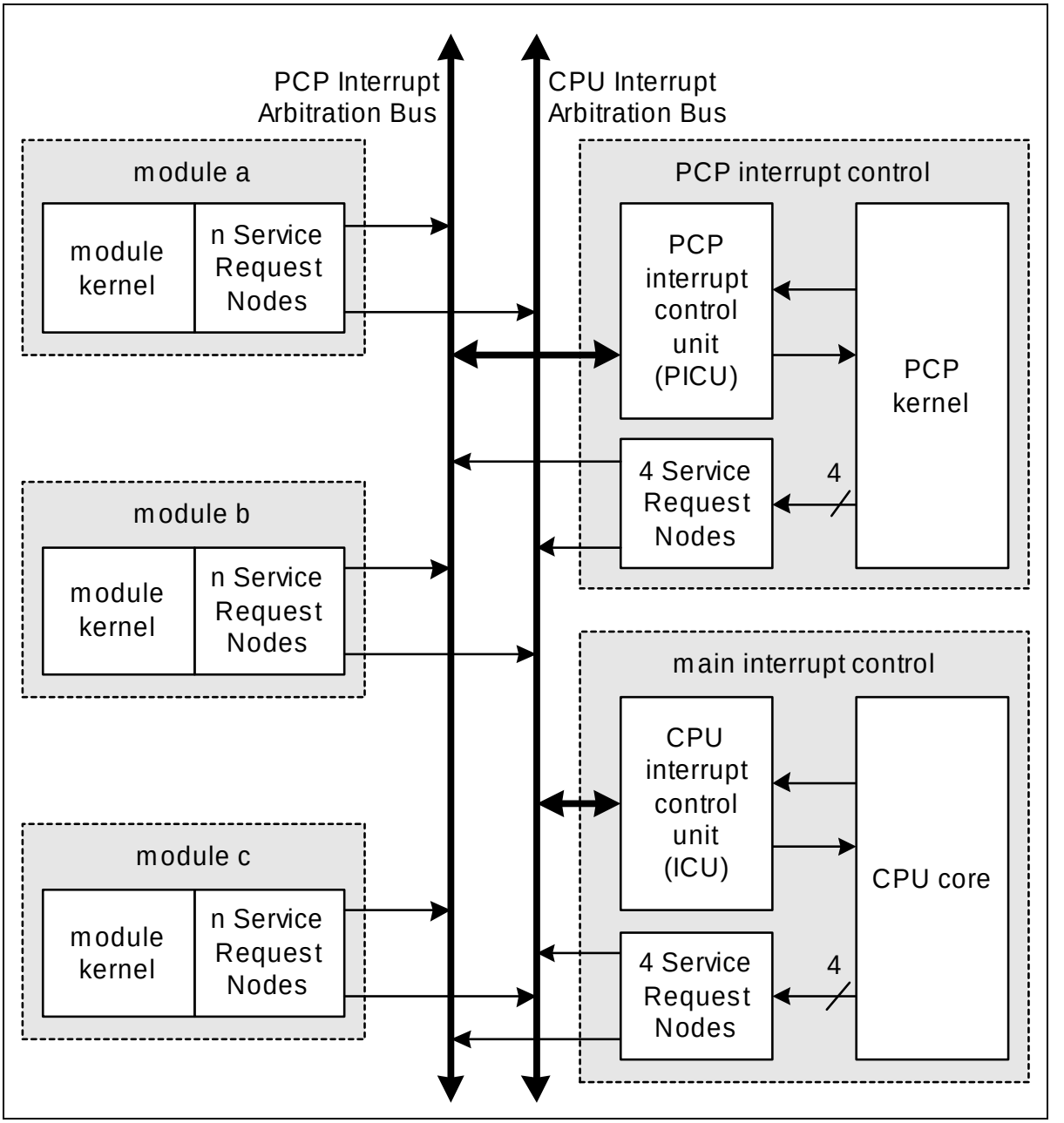

Figure 2-2 Block Diagram Interrupt System

2.7 Peripheral Control Processor (PCP)

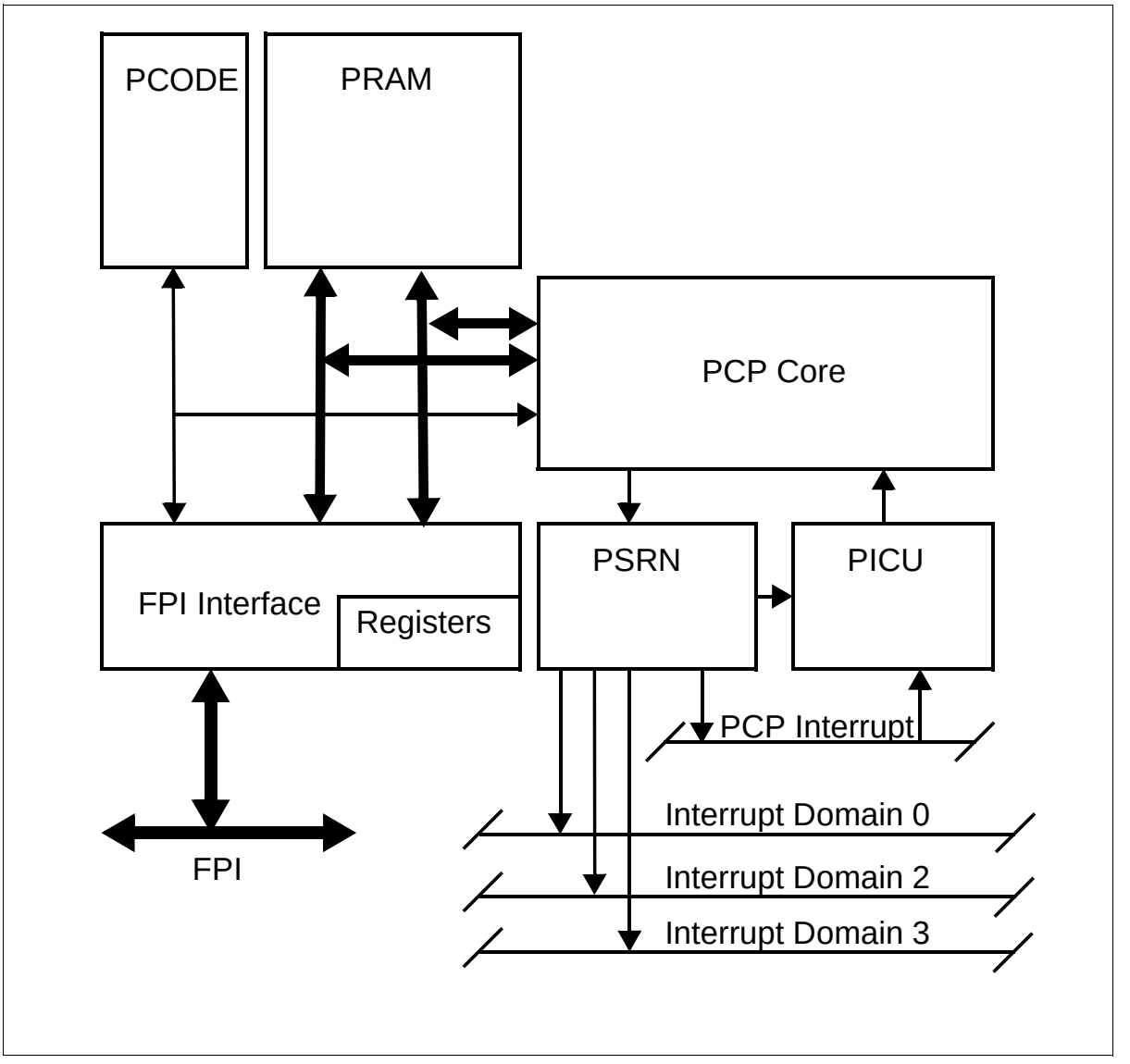

Figure 2-3 PCP block diagram

The PCP is designed to work in partnership with a host CPU and performs many of the tasks that would conventionally be performed by CPU interrupt service routines or a DMA controller. The PCP off-loads the host CPU from most of the time critical interrupts, easing the implementation of systems based on operating systems.

In principle the PCP may be considered to be a conventional processor which only executes code in response to interrupt service requests (i.e. has no processing which is not at interrupt level). It has an architecture which efficiently supports DMA type of bus transactions to / from arbitrary devices and memory addresses and also some reasonable computational capabilities. Whenever the PCP responds to a PCP interrupt

request (which has a specific interrupt priority level) it will use a register set ("context") specific to that individual interrupt level and will also generally execute code which is also specific to that interrupt level. For this reason the term "Channel" will be used throughout the remainder of this document to refer to all PCP resources associated with a particular PCP interrupt level.

The architecture is flexible enough to allow the implementation of a subset of the commands/instructions as a simple DMA controller.

The PCP has a Harvard architecture (i.e. separate code and data memory spaces). Any FPI bus master (including the PCP itself) can access both PCP code (PCODE) and data (PRAM) memory via the FPI bus.

2.8 FPI-Bus

The FPI-Bus is based on the OMI-PI-Bus proposal, but includes many modifications to reduce complexity of the necessary control logic. The changes go beyond a point were some degree of compatibility would have been maintained.

FPI-Bus Features:

The FPI-Bus is designed with requirements of high-performance systems in mind. The features are:

- Core independent
- Multi-master capability (8 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 480 MBytes/s (@ 60 MHz bus clock)
- Address and data bus scalable (32 bit address bus, 32 bit data bus)
- 8-/16- and 32 bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Burst transfer capability
- EMI and power consumption minimized

FPI-Bus does **not** provide:

- Cache coherency support
- Broadcasts
- Dynamic bus sizing
- Unaligned data accesses
- Split transaction support for agents with long response time

2.9 LMB-Bus

The local bus is a synchronous, pipelined, split bus with variable block size transfer support. All signals relate to the positive clock edge.

The protocol supports 8,16,32 & 64 bits single beat transactions and variable length 64 bits block transfers. The bus is currently designed to support 3 master/slaves and 4 slaves but it is expandable (no protocol limitations except capacitance limitations).

An effort was made to comply with the FPI bus protocol as much as possible. This was done in order to simplify the FPI to Local Bus bridge and to enable future transformation of FPI compliant agents to the Local bus. The differences that still exist enable enhanced bus utilization.

Key Features:

The LMB provides the following features:

- Optimized for high speed and high performance
- 32 bit address, 64 bit data busses
- Central simple per cycle arbitration
- Slave controlled wait state insertion
- Address pipelining (max depth - 2)
- Split transactions
- Variable block length - 2, 4 or 8 beats of 64 bit data

2.10 On-Chip Debug System (OCDS)

The TC1920 architecture is supporting OCDS level 1 and 2.

OCDS level 3 is not required.

Level	Run Time Control	System access via		Basic PC trace
		JTAG	Trace bus	
1	Y	Y	N	N
2	Y	Y	Y	Y

Table 2-1 Core-related and System Control Modules

Module	Address Range	I/O Lines	Interrupt Nodes
TriCore CPU Slave Registers (CPS)	F7E0 FF00$_H$ - F7E0 FFFF$_H$	-	CPU_SRC0..3 CPU_SRCSB
Memory Management[1] Unit (MMU)	F7E1 8000$_H$ - F7E1 80FF$_H$	-	-
Segment Protection Registers[1]	F7E1 C000$_H$ - F7E1 C0FF$_H$	-	-
Core Debug[1] (Core OCDS)	F7E1 FD00$_H$ - F7E1 FDFF$_H$	-	-
TriCore CPU[1] SFR, GPR	F7E1 FE00$_H$ - F7E1 FFFF$_H$	-	-
Program Memory Unit[2] (PMU)	F87F FD00$_H$ - F87F FDFF$_H$	-	-
Data Memory Unit[2] (DMU)	F87F FC00$_H$ - F87F FCFF$_H$	-	-
Peripheral Control Processor (PCP)	F000 3F00$_H$ - F000 3FFF$_H$	-	PCP_SRC0..3
External Bus Unit (EBU)	F800 0000$_H$ - F800 03FF$_H$	AD[31:0], A[23:0], 27 control lines	-
System Control Unit (SCU)	F000 0000$_H$ - F000 00FF$_H$	4 XTAL, $\overline{\text{PORST}}$, $\overline{\text{HRST}}$, 8 EXIN, $\overline{\text{NMI}}$, 4 test, CLKOUT, BYPASS	EXI_SRC0..7 NMI[3]

Table 2-1 Core-related and System Control Modules (cont'd)

Module	Address Range	I/O Lines	Interrupt Nodes
FPI Bus Control Unit (BCU)	F000 0200_H - F000 $02FF_H$	-	BCU_SRC
LMB Bus Control Unit (LCU)	F87F $FE00_H$ - F87F $FEFF_H$	-	LCU_SRC
LMB to FPI Bus Bridge (LFI)	F87F $FF00_H$ - F87F $FFFF_H$	-	-
Port Control (Ports 0, 1, 2, 3, 5)	F000 2800_H - F000 $2CFF_H$	P0 (7), P1(7), P2(15), P3(15), P5(15)	-
Debug Support (JTAG, OCDS)	F000 0400_H - F000 $04FF_H$	$\overline{\text{TRST}}$, TCK, TDI, TDO, TMS, OCDSE, BRKIN, BRKOUT, 16 trace outputs	-

1) This address range is also accessed via the CPS by the FPI bus.

2) This address range is accessed via the LMB.

3) The NMI is directly connected to the core (no SRC) and always acts on the highest priority. It is used as highest priority interrupt for the NMI input, the watchdog, the PLL and for wake-up via the RTC or via the EXIx inputs.

3 On-Chip Peripheral Units

The TC1920 offers several on-chip peripheral units such as serial controllers, timer units, AD converter and Codec interface. Within the TC1920 all these peripheral units are connected to the TriCore CPU/system via the FPI (Flexible Peripheral Interconnect) Bus. Several IO lines on the TC1920 ports are reserved for these peripheral units to communicate with the external world.

Peripheral Units of the TC1920:

- Three Asynchronous/Synchronous Serial Channels with baudrate generator, parity, framing and overrun error detection, IrDA mode, FIFO mode (only for ASC2)
- One High Speed Synchronous Serial Channels with programmable data length and shift direction
- TwinCAN Module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
- Serial Data Link Module compliant to SAE Class B J1850 specification
- IIC module with connection to 2 external busses
- 2 multi-functional General Purpose Timer Units with three 32-bit timer/counter
- One Analog-to-Digital Converter Units with 8-bit, 10-bit, or 12-bit resolution and 6 analog inputs
- Dual channel Codec interface
- GPIO blocks

Table 3-1 Peripheral Modules

Module	Address Range	I/O Lines	Interrupt Nodes
Asynchronous Serial Channel 0 (ASC0)	$F000\ 0A00_H$ - $F000\ 0AFF_H$	RDX0, TDX0	ASC0_TSRC ASC0_RSRC ASC0_ESRC ASC0_TBSRC
Asynchronous Serial Channel 1 (ASC1)	$F000\ 0B00_H$ - $F000\ 0BFF_H$	RDX1, TDX1	ASC1_TSRC ASC1_RSRC ASC1_ESRC ASC1_TBSRC
Asynchronous Serial Channel 2 (ASC2)	$F000\ 0C00_H$ - $F000\ 0CFF_H$	RDX2, TDX2	ASC2_TSRC ASC2_RSRC ASC2_ESRC ASC2_TBSRC
Synchronous Serial Channel (SSC)	$F000\ 0800_H$ - $F000\ 08FF_H$	SCLK, MRST, MTSR	SSC_TSRC SSC_RSRC SSC_ESRC

Table 3-1 Peripheral Modules (cont'd)

Module	Address Range	I/O Lines	Interrupt Nodes
Inter-IC Bus (IIC)	$F000\ 0500_H$ - $F000\ 05FF_H$	SCL[1:0], SDA[1:0]	IIC_XP0SRC IIC_XP1SRC IIC_XP2SRC
Real Time Clock (RTC)	$F000\ 0100_H$ - $F000\ 01FF_H$	-	RTC_SRC
System Timer Unit (STM)	$F000\ 0300_H$ - $F000\ 03FF_H$	-	-
General Purpose Timer 0 (GPTU0)	$F000\ 0700_H$ - $F000\ 07FF_H$	GPTU0[7:0]	GPTU0_SRC0..7
General Purpose Timer 1 (GPTU1)	$F000\ 0600_H$ - $F000\ 06FF_H$	GPTU1[7:0]	GPTU1_SRC0..7
CAN (TwinCAN)	$F010\ 0000_H$ - $F010\ 0BFF_H$	RXDCAN[1:0], TXDCAN[1:0]	CAN_SRC0..7
SDLM (J1850)	$F000\ 2600_H$ - $F000\ 26FF_H$	RXJ1850, TXJ1850	SDLM_SRC0..1
Speech Interface (Codec)	$F000\ 2400_H$ - $F000\ 24FF_H$	2*2 analog IN, 2*2 analog OUT, CEXT, CODEC_DIS	CODEC_SRC0..5
Analog to Digital Converter (ADC)	$F000\ 2200_H$ - $F000\ 23FF_H$	AIN[5:0] = P4, ADEMUX[2:0], ADEXTIN	ADC_SRC0..3

3.1 Asynchronous/Synchronous Serial Interfaces (ASC 0/1/2)

Overview:

The Asynchronous/Synchronous Serial Interface ASC provides serial communication between the TriCore and other microcontrollers, microprocessors or external peripherals. The implementation is held parametrizable in order to allow the usage of parallel busses of different width and with different protocols.

Features:

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 3.75 MBaud to 0.888 Baud (@ 60 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 7.5 MBaud to 764.4 Baud (@ 60 MHz module clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - on a transmitter buffer empty condition
  - on a transmit last bit of a frame condition
  - on a receiver buffer full condition
  - on an error condition (frame, parity, overrun error)
- Support for IrDA
- Automatic Baudrate Detection
- 8 Byte FIFO (ASC2 only)

3.2 High-Speed Synchronous Serial Interfaces (SSC)

Overview:

The High Speed Synchronous Serial Interface SSC provides serial communication between microcontrollers, microprocessors or external peripherals. The SSC supports full-duplex and half-duplex synchronous communication up to 30 MBaud (@ 60 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits : 2 to 16 bit
  - Programmable shift direction : LSB or MSB shift first
  - Programmable clock polarity : idle low or high state for the shift clock
  - Programmable clock/data phase : data shift with leading or trailing edge of SCLK
- Baudrate generation from 30 MBaud to 457.76 Baud (@ 60 MHz module clock)

Interrupt generation
  - on a transmitter empty condition
  - on a receiver full condition
  - on an error condition (receive, phase, baudrate, transmit error)
- Three pin interface

3.3 Inter-IC Interface (IIC)

IIC supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA).

The on-chip IIC Bus module connects the platform buses to other external controllers and/or peripherals via the two-line serial IIC interface. The IIC Bus module provides communication at data rates of up to 400 Kbit/s and features 7-bit addressing as well as 10-bit addressing. This module is fully compatible to the IIC bus protocol.

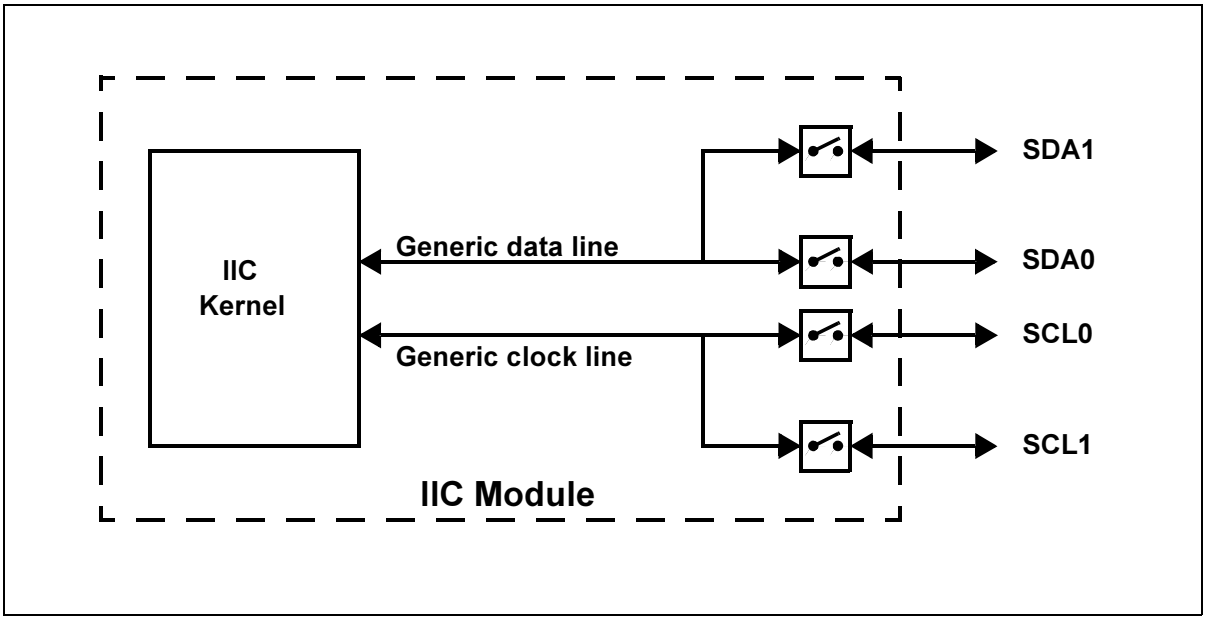

Figure 3-1 IIC Bus Line Connections

The module can operate in three different modes:

Master mode, where the IIC controls the bus transactions and provides the clock signal.

Slave mode, where an external master controls the bus transactions and provides the clock signal.

Multimaster mode, where several masters can be connected to the bus, i.e. the IIC can be master or slave.

The on-chip IIC bus module allows efficient communication via the common IIC bus. The module unloads the CPU of low level tasks like:

- (De)Serialization of bus data.
- Generation of start and stop conditions.
- Monitoring the bus lines in slave mode.
- Evaluation of the device address in slave mode.
- Bus access arbitration in multimaster mode.

IIC Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored.
- Selectable baud rate generation.
- Support of standard 100 KBaud and extended 400 KBaud data rates.
- Operation in 7-bit addressing mode or 10-bit addressing mode.
- Flexible control via interrupt service routines or by polling.
- Dynamic access to up to 4 physical IIC busses.

3.4 CAN Interface (TwinCAN)

Figure 3-2 shows a global view of the functional blocks of the TwinCAN module.

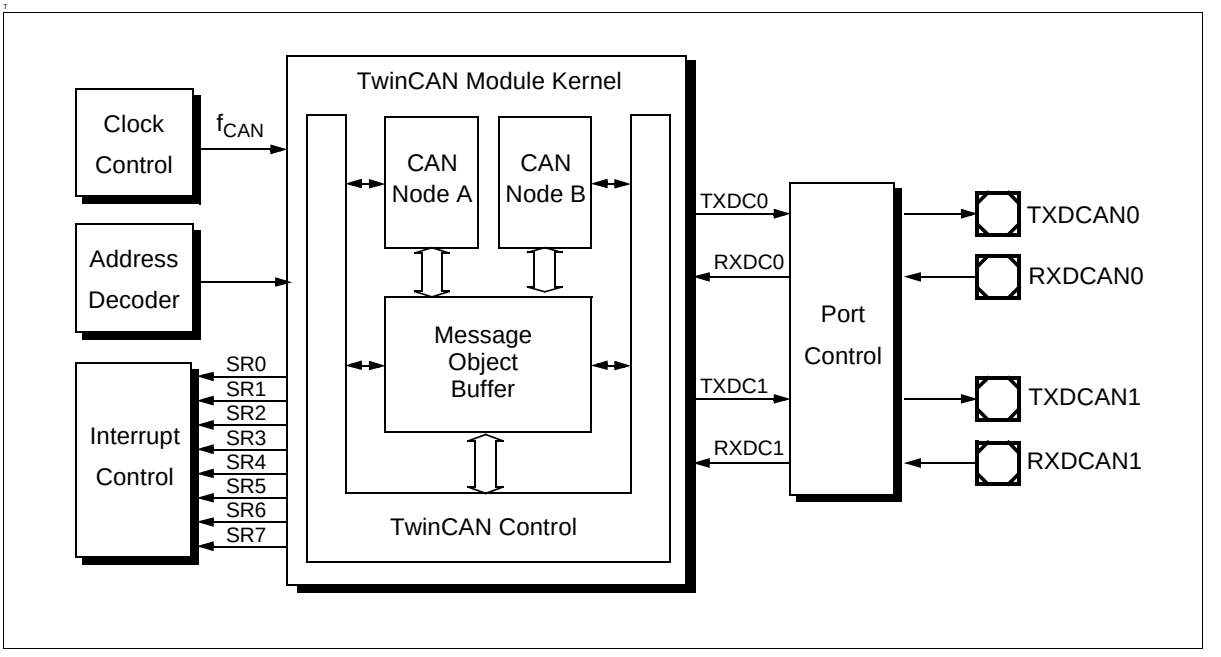

Figure 3-2 General Block Diagram of the TwinCAN Interfaces

TwinCAN Features:

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Full-CAN functionality: 32 message objects can be individually
  - assigned to one of the two CAN nodes,
  - configured as transmit or receive object,
  - participate in a 2,4,8,16 or 32 message buffer with FIFO algorithm,
  - setup to handle frames with 11 bit or 29 bit identifiers,
  - provided with programmable acceptance mask register for filtering,
  - monitored via a frame counter,
  - configured to Remote Monitoring Mode.
- Up to eight individually programmable interrupt nodes can be used.
- CAN Analyzer Mode for bus monitoring is implemented.

The TwinCAN module has four IO lines. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding, and port control logic.

The CAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN nodes can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources in order to optimize the CAN bus traffic handling and to minimize the CPU load. The flexible combination of Full-functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and comfortable CAN bus traffic handling.

Depending on the application, each of the 32 message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timings for both CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connect each CAN node to a bus transceiver.

3.5 Serial Data Link Module (J1850)

Figure 3-3 shows a global view of the functional blocks of the J1850 interface.

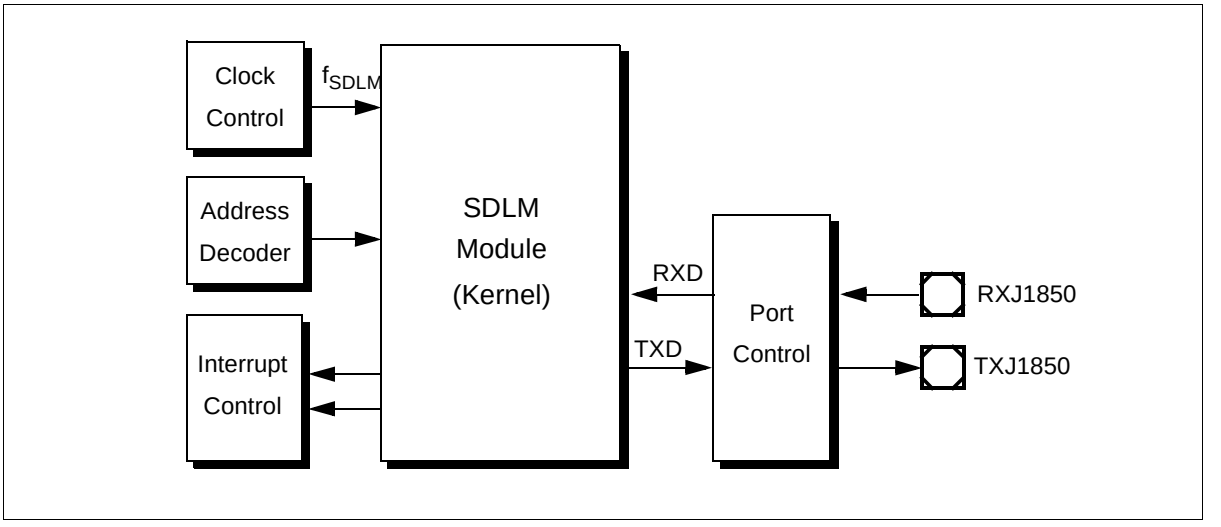

Figure 3-3 General Block Diagram of the SDLM Interface

The J1850 module communicates with the external world via two I/O lines, the J1850 bus. The RXD line is the receive data input signal and TXD is the transmit data output signal. The Serial Data Link Module provides serial communication to a J1850 based serial bus. J1850 bus transceivers have to be implemented externally in a system. The J1850 module is conform to the SAE Class B J1850 specification and compatible to class 2 protocol.

General SDLM Features:

- Compliant to SAE Class B J1850 specification
- Full support of GM class 2 protocol
- Variable Pulse Width (VPW) format with 10.4 kBaud
- High speed receive/transmit 4x mode with 41.6 kBaud
- Digital noise filter
- Power save mode and automatic wake up upon bus activity
- Support of single byte headers or consolidated headers
- CRC generation & check
- Support of block mode for receive and transmit

Data Link Operation Features:

- 11 bytes transmit buffer
- Double buffered 11 bytes receive buffer
- Support of In-frame response (IFR) types 1,2,3
- Advanced interrupt handling for RX, TX and error conditions
- All interrupt sources can be enabled/disabled individually
- Support of automatic IFR for types 1,2 for three byte consolidated headers

3.6 Timer Units (GPTU 0/1)

Figure 3-4 shows a global view of all functional blocks of one GPTU module.

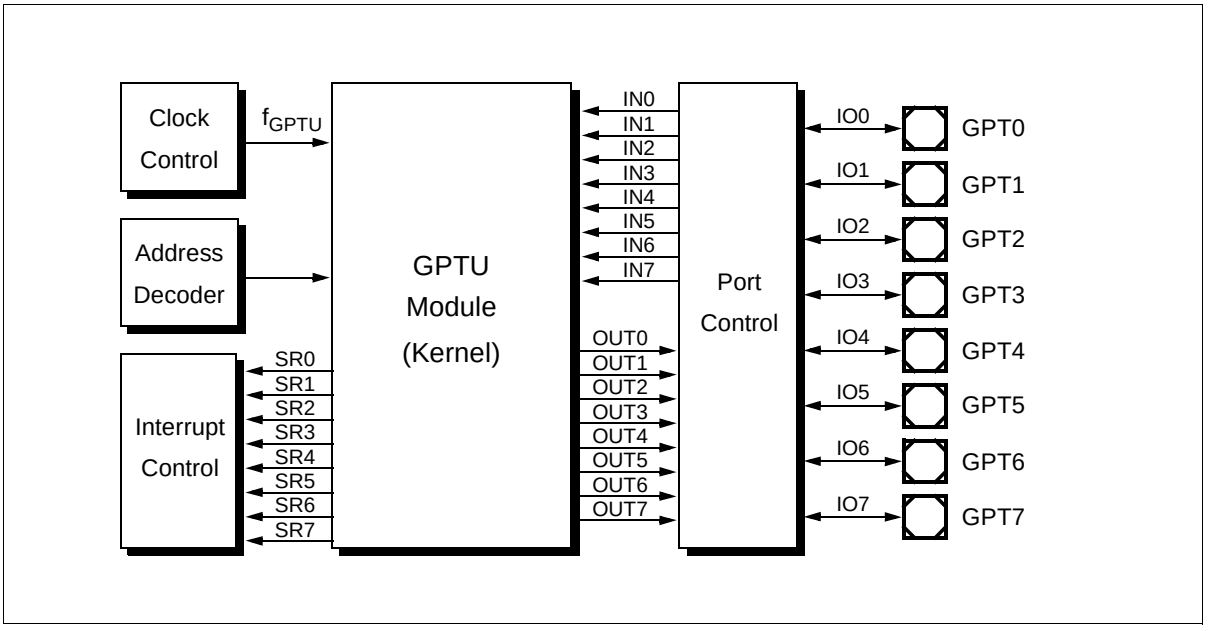

Figure 3-4 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs.

The three timers of the GPTU module T0, T1, and T2, can operate independently from each other, or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of $f_{GPTU}/2$.
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can determine a count option

Features of T2:

- Optionally count up or down
- Operating modes:
  - Timer
  - Counter
  - Incremental Interface Mode
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes.

3.7 Analog to Digital Converter (ADC)

Figure 3-5 shows a global view of the ADC module kernel with the module specific interface connections.

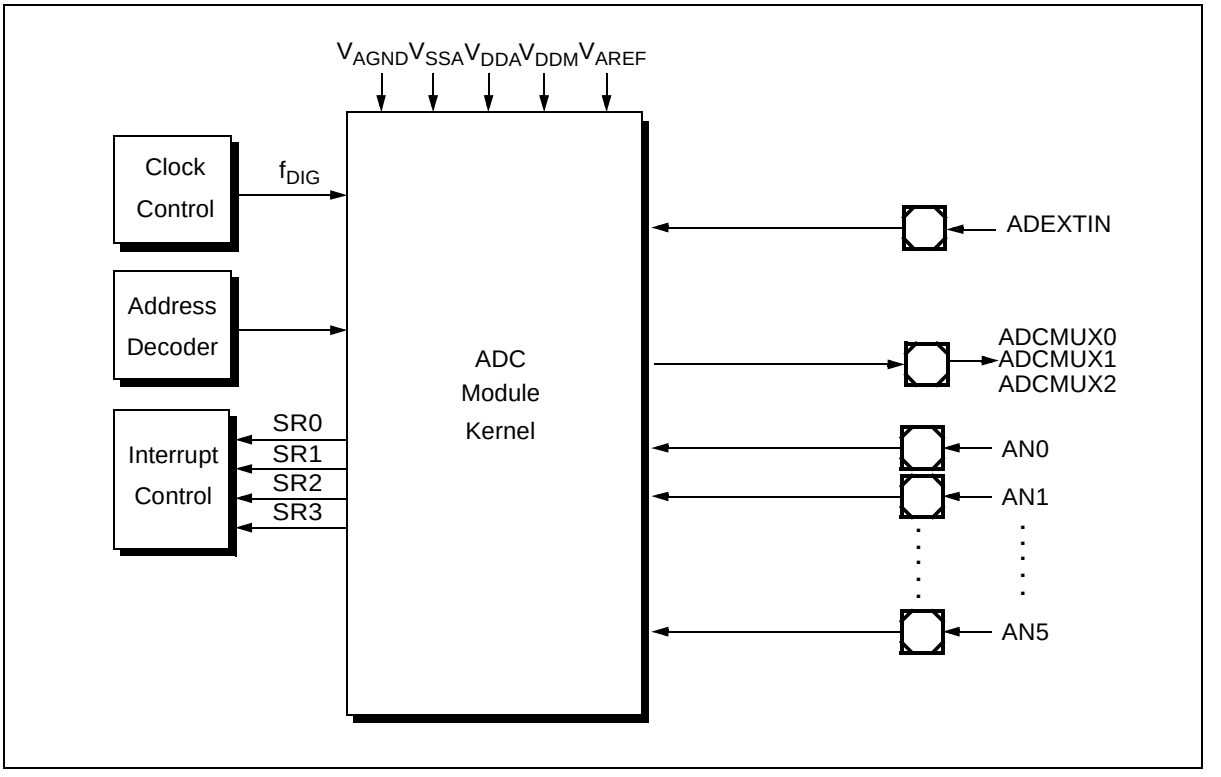

Figure 3-5 General Block Diagram of the ADC module

The on-chip ADC module of the TC1920 is an analog to digital converter with 8-bit, 10-bit or 12-bit resolution including sample & hold functionality. The A/D converter operates by the method of the successive approximation. A multiplexer selects between up to 6 analog input channels. Conversion requests are generated either under software control or by hardware. An automatic self-calibration adjusts the ADC module to changing temperatures or process variations.

Features:

The following functionality has been implemented in the on chip ADC module to fulfill the enhanced requirements of embedded control applications:

- 8-bit, 10-bit, 12-bit A/D Conversion
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ± 2 LSB @ 10-bit resolution
- Integrated sample and hold functionality
- 6 analog input channels
- Dedicated control and status registers for each analog channel
- Flexible conversion request mechanisms
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Automatic control of external analog multiplexer
- Equidistant samples initiated by timer
- External trigger inputs for conversion requests
- Power reduction and clock control feature

3.8 Real Time Clock Unit RTC

The Real Time Clock (RTC) module is basically an independent timer chain and counts clock ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work fully asynchronous to the system frequency and is optimized on low power consumption. RTC of the TC1920 does not support the power-off isolation mode.

Features:

The RTC serves different purposes:

- Absolute system clock to determine the current time and date
- Cyclic time based interrupt
- Alarm interrupt for wake up on a defined time
- 48-bit timer for long term measurements

3.9 Codec Interface

The speech A/D and D/A converters (called codec) is designed for telephone and speech recognition quality. They can be used for microphone / earpiece applications. The TC1920 configuration implements a dual channel speech codec connected to the FPI bus.

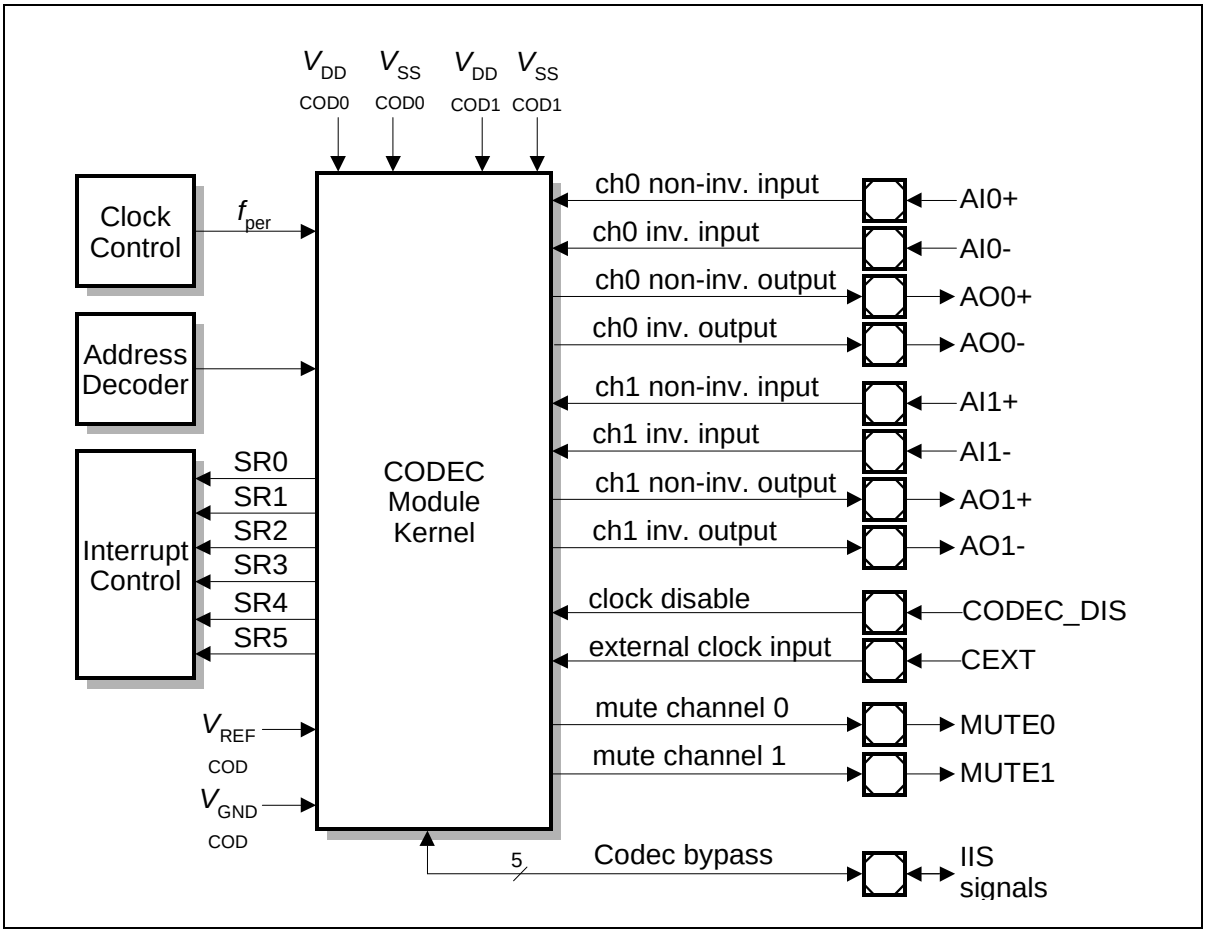

Figure 3-6 General Codec Overview

4 Device Aspects

4.1 General Purpose I/Os (GPIO)

- Push/pull output drivers
- 3.3 Volt operation for GPIO
- Programmable pull-up/-down devices at all pins
- CMOS-like input threshold
- Optional Open Drain Output Mode

4.2 Preliminary Electrical characteristics

- Dual Voltage supply: 1.8 Volt +/- 5 % for the core logic, and 3.3 Volts +/- 5% for the pads
- Compliant with automotive EMI requirements

4.3 Package

- BGA256 package
- Max chip power consumption is around 1.56W (estimation)

4.4 Temperature Ranges

- Ambient temperature : -40° to +85°C

4.5 System Clock Frequency

- Maximum System Clock Frequency: 100 MHz
- PLL module with selectable factors for input and output frequencies.

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Dr. Ulrich Schumacher

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