T3BwP™ Device
Channelized DS3 Access Solution
TXC-06826

DATA SHEET
PRODUCT PREVIEW

FEATURES

- Complete single-chip channelized DS3 solution
- RISC processor with royalty-free DD-AMPS™ firmware (Drivers, Data link, Alarms, Messaging, Performance/configuration objects, and Signaling)
- Host communication via royalty-free, message-based, POSIX-compatible API
- Integrated 672 X 4,096-channel DS0 cross-connect supports grooming, broadcast, off-bus hairpinning, and bonding
- Integrated DS1 cross-connect
- 28 DS1 line interfaces or 1 DS3 line interface
- Combination of unframed DS1, transmission DS1, and either MVIP or H.100/H.110 as terminal side interfaces
- Selectable DS3 clear channel functionality
- On-chip maintenance of 15-minute performance objects per IETF RFCs 2495, 2496 and 2494.
- Two DS1 monitor ports for monitoring any DS1 clock and data
- Test Access Port (IEEE 1149.1 boundary scan)
- +3.3 V I/O. 5 V tolerant
- 456-lead plastic ball grid array package (27 mm x 27 mm)

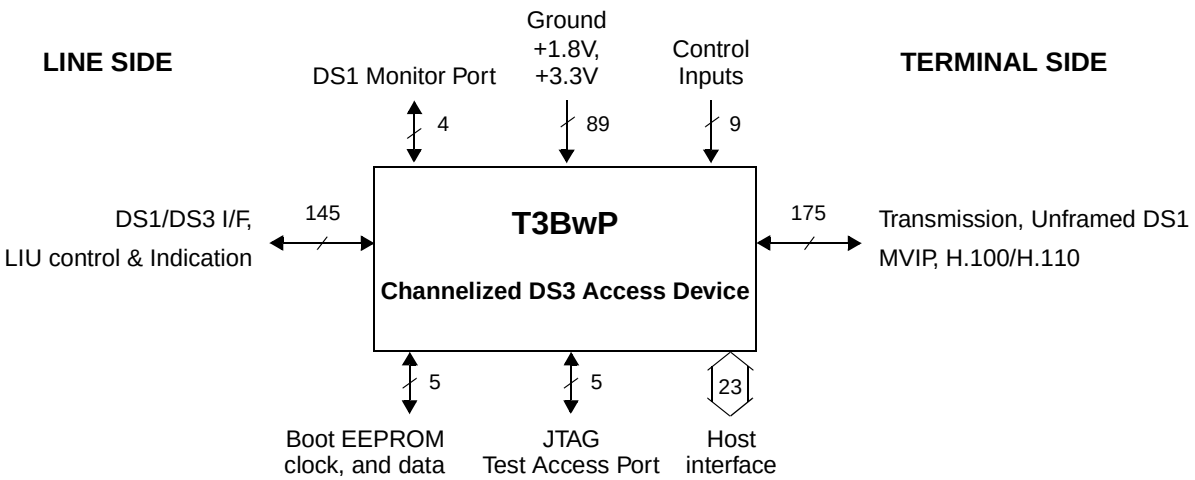
DESCRIPTION

T3BwP™ (TXC-06826) is a RISC processor based device that supports the requirements of next-generation channelized DS3 access systems. T3BwP integrates an M13 multiplexer, 28 DS1 framers, and a 672 X 4,096-channel DS0 cross-connect with an embedded high-performance microprocessor to provide a complete channelized DS3 solution on a single chip. The embedded processor firmware handles device drivers, data links, alarms, messaging, MIB performance objects, and signaling functions and allows communication to an external host via high-level API messages. The firmware is provided by TranSwitch and loaded from an external serial EEPROM at device boot-up.

The T3BwP can be configured to support a variety of modes of operation, which allows for design flexibility. T3BwP supports a combination of unframed DS1, transmission DS1 and H.100/H.110 bus or MVIPTM interfaces on the terminal side and either DS3 or DS1 on the line side. For TDM applications, all 672 DS0 channels can be switched to any of the 4,096 H.100/H.110 computer telephony (CT) bus channels.TheT3BwP can also be enabled to provide DS3 C-bit parity for unchannelized services. The on-chip firmware provides the control and management plane functionality to the host to configure, control and monitor all DS3, DS1, DS0 and digital cross-connect functions. The standards-based MIB functionality is provided for network management.

APPLICATIONS

- T-carrier Termination Equipment: Muxes, Inverse Muxes, Cross-connects, Groomers
- CT (Computer Telephony) Network Interface Boards
- VoP (Voice over Packet/Cell) Gateways
- MSADs (Multi-Service Access Devices)
- DSLAMs (Digital Subscriber Loop Access Multiplexers)
- ECUs (Echo Cancellation Units)



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OVERVIEW

The T3BwP is a highly integrated system-on-chip (SoC) solution for supporting the requirements of next-generation channelized DS3 access systems. An integrated M13 multiplexer, DS1 framers, DS1 and DS0 cross-connects, and a high-performance RISC processor with embedded firmware provided by TranSwitch make the T3BwP a complete channelized DS3 solution. The on-chip processor for the T3BwP is controlled by the host via a high-level message-based API (Application Program Interface), helping reduce the software integration effort and providing flexibility to address feature enhancements and standards changes through firmware upgrades. The on-chip firmware provides the control and management plane functionality to the host to configure, control and monitor the DS3, DS1, DS0 and cross-connect functions. The standards-based MIB object functionality is provided for network management.

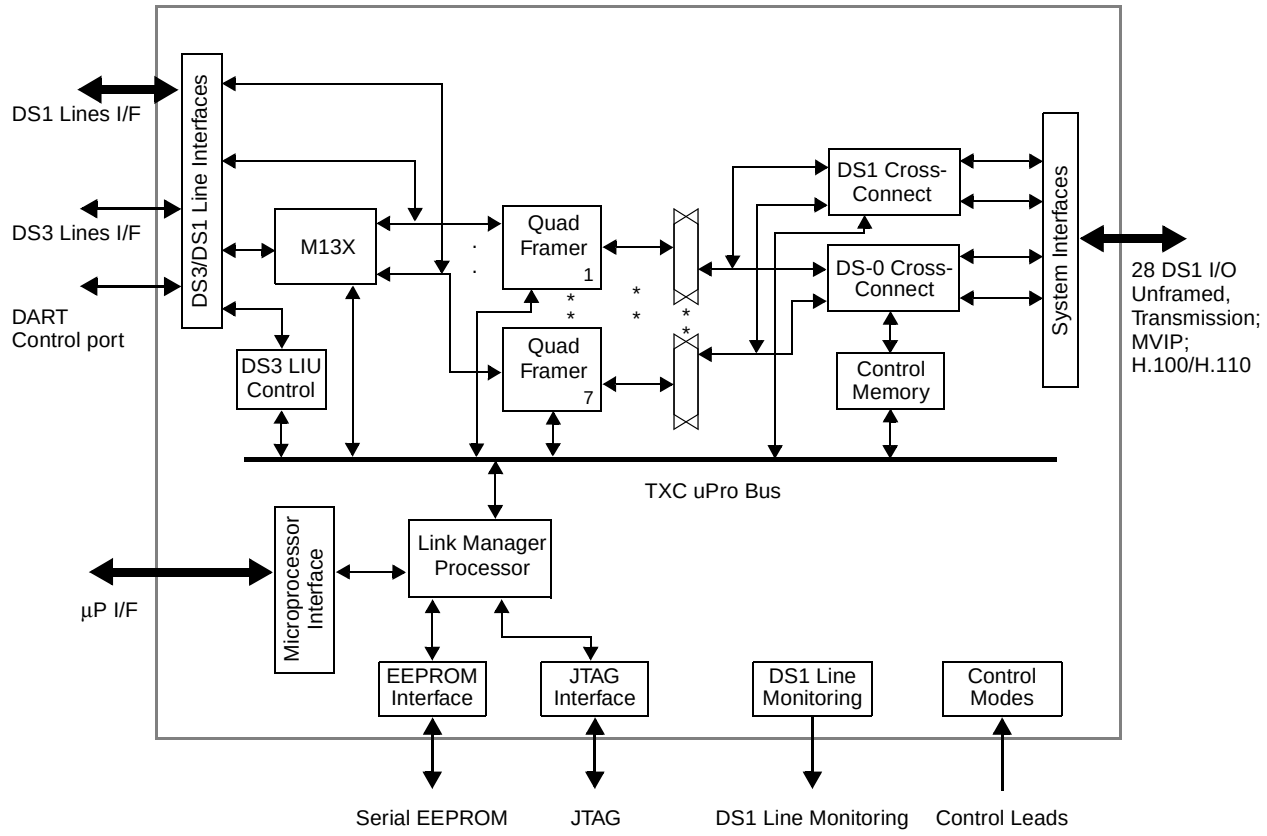


Figure 1. T3BwP TXC-06826 High Level Block Diagram

Figure 1 shows a block diagram for the T3BwP. The main blocks shown are: M13X, QT1F-*Plus*, Serial-to-Parallel converter, DS1/DS0 cross-connect, and Link Manager processor. External interfaces include 28 terminal-side framer access ports (supporting H.100/H.110, MVIP, transmission, and unframed modes), 28 DS1 line-side ports or one DS3 line-side port, a serial EEPROM interface for firmware and initial configuration data, a local microprocessor bus used to control external devices, two monitor ports to monitor any two DS1s, a control port to control the TranSwitch DART DS3 LIU, and a JTAG port for test access. For channelized DS3 applications, the DS1 framer line-side ports are M13 multiplexed to the DS3 line port; the terminal side DS1 ports may individually be used for direct M13 access.

The DS3 framer/multiplexer block is similar to the TranSwitch M13X DS3/DS1 mux/demux device (TXC-03305). The DS3 framer provides M frame and M sub-frame framing with AIS and LOS detection; DS3 loopbacks; and access to the C bits with processing of the FEAC channel (C3), path maintenance data link (full duplex HDLC controller over C13, C14 and C15), and FEBE (C10, C11 and C12. DS3 X-bit access, loss of signal, loss of frame, AIS, idle, C-bit parity (C7, C8 and C9) and P-bit parity are detected and generated. This block can operate in M13 mode or in a mode where the 21 C bits are used for stuff control of the 7 DS2s. DS2 framing (7 instances) is provided either all at a fixed rate (C bit parity mode at 6306.2723 kbit/s) or M13 mode. Each DS2 framer and multiplexer handles four DS1 signals. DS1 loss of signal and DS1 loop backs are provided under control of the FEAC channel or the DS2 stuff control bits (C bits). The DS1 signals are multiplexed directly from the DS1 framer blocks. The DS1 signals are demultiplexed and fed to the DS1 framer blocks via a dejitter buffer or with demultiplexing jitter, depending on application.

The DS1 framer blocks are similar to the TranSwitch QT1F-Plus quad T1 framer device (TXC-03103). Automatic performance report message generation, automatic SF/ESF detection, trunk conditioning, deep FDL slip buffers, one-second shadow registers, and interrupt on signaling change-of-state are accomplished by the RISC processor. Framing is provided to the T1 line ports or the M13. Alarm detection/generation, CAS/RBS signaling debounce and access/insertion/extraction, slip buffering, facility data link (FDL) support and diagnostic support using loop backs/PRBS generator/analyzer, etc. are provided.

The terminal side supports MVIP, H.100/H.110, transmission, and unframed modes with clock, frame, data and signaling leads. Common clock and frame signals are provided in MVIPTM and H.100/H.110 modes. External signaling access is not provided in transmission mode. T1 line access is provided using NRZ coding. A local microprocessor bus is provided for the internal RISC to control external devices such as T1 LIUs. The control of the TranSwitch DART DS3 LIU is fully supported.

The Link Manager RISC processor performs the following control- and management-plane functions:

1. Host interface using message queues
2. Device initialization, configuration and control
3. Alarm detection and propagation
4. Far end alarm generation (through FEAC channel/X-bits, FDL/payload bit)
5. Performance monitoring of near end and far end at DS1 and DS3 rates
6. Performance reporting to near and far end (e.g., DS1 PRMs in ESF mode), DS3 FEBE in C-bit parity mode)
7. Execution of maintenance and diagnostic requests from host or far end (e.g., loopbacks)
8. Maintenance of configuration and 15-minute performance objects

The flexible T3BwP architecture supports a variety of modes of operation, determined by the upgradeable firmware provided with the device. When used in conjunction with the firmware, T3BwP supports a combination of unframed DS1, transmission DS1, and H.100/H.110 or MVIPTM system interface on the terminal side. The T3BwP line side interface is either DS3, which interfaces directly with a DS3 LIU such as the TranSwitch DART (TXC-02030), or DS1, which interfaces directly with a T1 LIU or an AAL1/2 device such as the TranSwitch COBRA (TXC-05427C). The T3BwP can also provide C-bit parity unchannelized service at a 44.210 Mbp/s rate.

The integrated TSI (time slot interchange) allows for grooming, concentration, switching, and multiplexing, internal hairpinning, bonding, and broadcast.

When configured in MVIP mode, any of the 672 DS0 channels can be switched to any timeslot on any MVIP highway.

When configured in H.100/H.110 mode, any of the 672 DS0 channels can be switched to any timeslot on any H.100/H.110 highway. This allows for multiple T3BwP's and other H.100/H.110 devices to be interconnected via a single H.100/H.110 bus.

The T3BwP can switch any line-side DS1 to any terminal-side DS1 when configured in unframed mode or transmission mode.

T3BwP provides multiple flexible data signal paths between line side and terminal port interface:

- Data flow from DS3 line to DS1 terminal port (H.100/H.110, MVIP, and transmission modes): DS3 Line <--> M13 <--> DS1 Framer <--> Cross-Connect <--> DS1 Terminal Port

  The data are received and transmitted using the DS3 line port. The M13 multiplexes/de-multiplexes DS1 signals from/to the 28 T1 framers. The data can be switched using either the T1 or DS0 cross-connect depending on the terminal-side interface mode selected.

- Data flow from DS3 line to DS1 terminal port bypassing DS1 framer (unframed mode): DS3 Line <--> M13 <--> Cross-Connect <--> DS1 Terminal Port

  The data are received and transmitted using the DS3 line port. The M13 multiplexes/de-multiplexes data from/to the 28 T1 framers. The DS1 signals bypass the DS1 framer in unframed mode. The T1's are switched using the T1 cross-connect.

- Data flow from DS1 line to DS1 terminal port (H.100/H.110, MVIP, and transmission modes): DS1 Line <--> DS1 Framer <--> Cross-Connect <--> DS1 Terminal Port

  The data are received and transmitted using the 28 DS1 line ports. The M13 block is bypassed. Each DS1 signal is transmitted/received via the DS1 framers. The data can be switched using either the T1 or DS0 cross-connect depending on the terminal-side interface mode selected.

- Data flow from DS1 line to DS1 terminal port bypassing the DS1 framer (unframed mode): DS1 Line <--> Cross-Connect <--> DS1 Terminal Port

  The data are received and transmitted using the 28 DS1 line ports. The M13 block is bypassed. The DS1 signals bypass the DS1 framer in unframed mode. The T1's are switched using the T1 cross-connect.

- Data flow from DS3 line to DS3 clear channel terminal port: DS3 Line <--> M13 <--> DS3 clear channel terminal port

  The data are received and transmitted using the DS3 line port. When this function is enabled, the data are transmitted via the M13 in clear channel mode (framing and C-bits only) at a 44.210 Mbp/s rate.

The T3BwP is configured, controlled, and monitored via a message-based, POSIX-compatible host API. Source code and portation guide are provided by TranSwitch.

IEEE 1149.1 Boundary Scan is sorted for BYPASS, IDCODE, EXTEST and SAMPLE/PRELOAD.

STANDARD DOCUMENTS

The T3BwP device has been designed to meet the latest industry standards.

- ANSI T1.102 -1995, Digital Hierarchy - Electrical Interfaces.
- ANSI T1.107 -1995, Digital Hierarchy - Format Specifications.
- ANSI T1.231 -1997, Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring.
- ANSI T1.403 -CORE 1998, Network and Customer Installation Interfaces - DS1 Electrical Interface.
- ANSI T1.404 -1994, Network-to-Customer Installation- DS3 Metallic Interface Specification.
- AT&T PUB 62411, Accunet T1.5 Service Description and Interface Specification.
- AT&T PUB 54016, Requirements for Interfacing Digital Terminal Equipment To Services Employing the Extended Superframe Format, Sept. 1989.
- GR-499-CORE, Transport Systems Generic Requirements (TSGR): Common Requirements, (Issue 1, Dec. 1995).
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990.
- MVIP, H-MVIP Multi-Vendor Integration Protocol. Working Document, April 1995.
- Enterprise Computer Telephony Forum, H.100 Rev. 1.0 Hardware Compatibility Spec. CT Bus.
- ITU-T G.711 Pulse Code Modulation (PCM) of Voice Frequencies, 1972.
- ITU-T O.151 Error Performance Measuring Equipment Operating at the Primary Rate and Above. 10/92.

TRANSWITCH DOCUMENTS

- T3BwP API Users Reference Guide

T3BwP FEATURES

The T3BwP device includes the following features:

LINE-SIDE DS3 INTERFACE

- M13 block provides all of the functionality found in the TranSwitch M13X device (TXC-03305)
- DART LIU control port
  - Provides control to the TranSwitch DART (TXC-02030) LIU device
- Framing and C-bit support for unchannelized (cell/packet) traffic at 44.210 Mbp/s rate.

28 LINE SIDE DS1 INTERFACES

- Includes Tx and Rx Data (NRZ), Tx and Rx Clock, and Rx BPV.

TERMINAL-SIDE INTERFACES AND CROSS-CONNECT FUNCTIONALITY

- Integrated DS0 TSI allows for grooming, concentration, multiplexing, internal hairpinning, bonding, broadcast, and switching of any DS0 to any TDM bus (MVIP or H.100/H.110) time slot. A time slot written in frame N is read back out in frame N+1.
- Integrated DS1 cross connect
  - Any line-side DS1 may be switched to any terminal-side DS1 when configured in unframed mode or transmission mode.
- DS1 terminal port
  - Unframed Mode
  - Transmission Mode:
    - Through DS1 cross-connect; bypass DS0 TSI
    - 1.544 MHz plus 3ms multi-frame pulse
  - MVIP Mode:
    - Through DS0 TSI
    - 2.048 MHz plus 125 uS frame pulse
  - H.100/H.110
    - Through DS0 TSI
    - 8.192 MHz plus 125 uS frame pulse
- Terminal ports can be configured to operate in unframed DS1, transmission DS1, and either H.100/H.110 or MVIP TDM bus modes
- H.100/H.110 operation as bus slave
  - Edge error and frame error detection
  - Bus clock source selection, monitoring, and automatic switching
  - Hardware and software support for hot-swap per PICMG 2.1 R1.0

PRODUCT PREVIEW

ON-CHIP RISC PROCESSOR AND FIRMWARE

- RISC processor-based SoC with embedded DD-AMPS (Drivers, Data link, Alarms, Messaging, Performance/configuration objects, and Signaling) firmware
- On-chip maintenance of 15-minute performance objects per IETF RFCs 2495, 2496, and 2494
- Firmware and default configuration loaded via serial EEPROM interface

HOST SOFTWARE

- High-level message-based, POSIX-compatible API host interface
- Support for standard MIBs
- Source code and portation guide provided by TranSwitch upon request.

GENERAL

- Boundary scan
- 1.8V core power supply
- 3.3 V I/O power supply
- Maximum power dissipation of 1.7 Watt
- 456-lead mini-BGA (27 mm x 27 mm) package

Maintenance:

- DS3 local loopback and remote line loopback via the TranSwitch DART device
- DS1 remote line and payload loopback and DS1 local loopback
- NxDS0 channel loopback, NxDS0 local loopback
- NxDS0 remote loopback: detect loop-up (Fract T1 (2^7 - 1)) /loop-down (Fract T1 (2^7 - 1) invert) sequence; setup/remove NxDS0 channel loopback according to loop-up/loop-down sequence; initiate loop-up/loop-down sequence
- Pseudo-Random Binary Sequence (PRBS) generator and analyzer

  - Two sets of PRBS generators and analyzers for DS1 line: QRSS (2^{20} - 1); 2^{15} - 1
  - Two sets of PRBS generators and analyzers for either NxDS0 or DS3: 2^{23} - 1; QRSS (2^{20} - 1); 2^{15} - 1; 2^{11} - 1; 32-bit code word
  - Indicator for lock, out of lock,
  - OOL counter

The following features are independently selectable for each of the 28 DS1 framers:

Framing Modes:

- D4 SF (Superframe Format)
  - Programmable for Fs, Ft or both frame bits
- ESF (Extended Superframe Format) - FPS bits with or without a valid CRC-6
  - HDLC On-board Controller; 4 kbit/s Data Link
- Unframed (bypass)
- Automatic
  - Framer searches alternatively for SF or ESF; state of search status in automatic and manual modes
- Programmable out of frame control: 2 out of 4, 5, or 6 frame bits.

Line Code:

- NRZ: Clock polarity clock in/out selection; data inversion and clock edge options.

Signaling:

- A, AB, 9-state AB signaling for ANSI T.403 ROB applications (SF)
- A, AB, ABCD (ESF)
- Signaling enable/disable on per DS0 basis
- Signaling freeze on per line basis (separate Tx & Rx direction)
- Signaling freeze on LOS
- Per-DS0 enable with microprocessor read and substitution in both receive and transmit directions for call control and trunk conditioning
- Signaling de-bounce: 12 (SF) or 24 (ESF) consecutive T1 frames must be equal before a state-change message is sent to the host

Clock Management:

- Use any of three reference clocks: BITS, Local Stratum, or any of twenty-eight recovered T1 clocks
- Terminal side and line side clocks on receive and transmit are independent

Alarms and Errors:

- Detect and force “yellow” and “blue” (AIS) alarms. Detect RAI-CI and AIS-CI signature
- Detect Out-Of-Frame, Loss-Of-Signal, Severely-Errored-Frame, Change-Of-Frame-Alignment, Transmit Slips, and Receive Slips

- Detect, count, and force CRC errors (ESF only), frame bit errors, and line code errors (bipolar violations, with or without excessive zeros)
- Detect and force frame slips

Slip Buffer and DS0 Control:

- Separate Tx and RX frame slip buffers, with independent bypass
- Per-DS0 enable (independent receive and transmit) with microprocessor read and substitution in both receive and transmit directions
- Per-DS0 inversion in transmit and receive directions (after slip buffers) in Transmission, H.100/H.110, and MVIP Modes

Performance and Fault Monitoring:

- Framer-based per-DS1 performance monitoring in Rx direction (Transmission, MVIP, and H.100/H.110 Modes)
- Facility Data Link (FDL) HDLC controller
- Shadow registers for all alarms and counters
- Automatic generation and transmission of FDL performance report message for NE and FE maintenance of performance objects per RFC 2495

The following features are selectable for the M13 mux:

DS3 Framing Functions:

- Framing on 4 F bits in M Subframe
- Framing on 3 M bits in M Frame
- X bit read access (Far end SEF/AIS)
- X bit programmable value (Far end SEF/AIS)
- P bit parity generating, monitoring, and counting (16 bit)
- C bit parity or M13 mode selection
- C bit parity Unchannelized (44.210 Mb/s clear channel)
- FEAC channel (C3): read access of FEAC word, write access to set loopbacks; FEAC word Detection of codes; loopbacks and alarms RAI indication (DS3 and DS1 alarms)
- C bit access:
    - C1 identification
    - C bit parity (C7-9) generation, checking, and counting
    - C bit Path Maintenance Data Link (PMDL) HDLC controller (C13 -15)
    - FEBE generation (on M, F or C parity error), detection, and counting

DS2 Framing Functions:

- Frame alignment on F bits
- Multiframe alignment on M bits
- X bit access

Multiplexing/Demultiplexing Functions:

- 4 DS1s into a DS2 using stuff bit control (DS2 C bits)
- 7 DS2 into a DS3 using stuff bit controls (DS3 C bits) or C bit parity mode
- DS3 into 7 DS2s using stuff bit controls (majority vote DS3 C bits) or C bit parity mode
- DS2 into 4 DS1s using stuff bit controls (majority vote DS2 C bits)

Alarms and Errors:

- Detect and force: DS3 AIS (optional unframed 1010 or 11110), DS3 IDLE (framed 1100), DS3 FEAC alarms (all codes in C-bit parity mode), DS3 RAI, P-bit parity errors, C-bit parity errors, FEBE, and DS2 RAI
- Detect: DS3 Out Of Frame, Loss Of Signal, Severely Errored Frame, and DS2 OOF

Performance and Fault Monitoring:

- Maintenance Data Link HDLC controller
- P bit and C bit parity error counter
- Frame bit errors
- Maintenance of performance objects per RFC 2495

MICROPROCESSOR INTERFACE

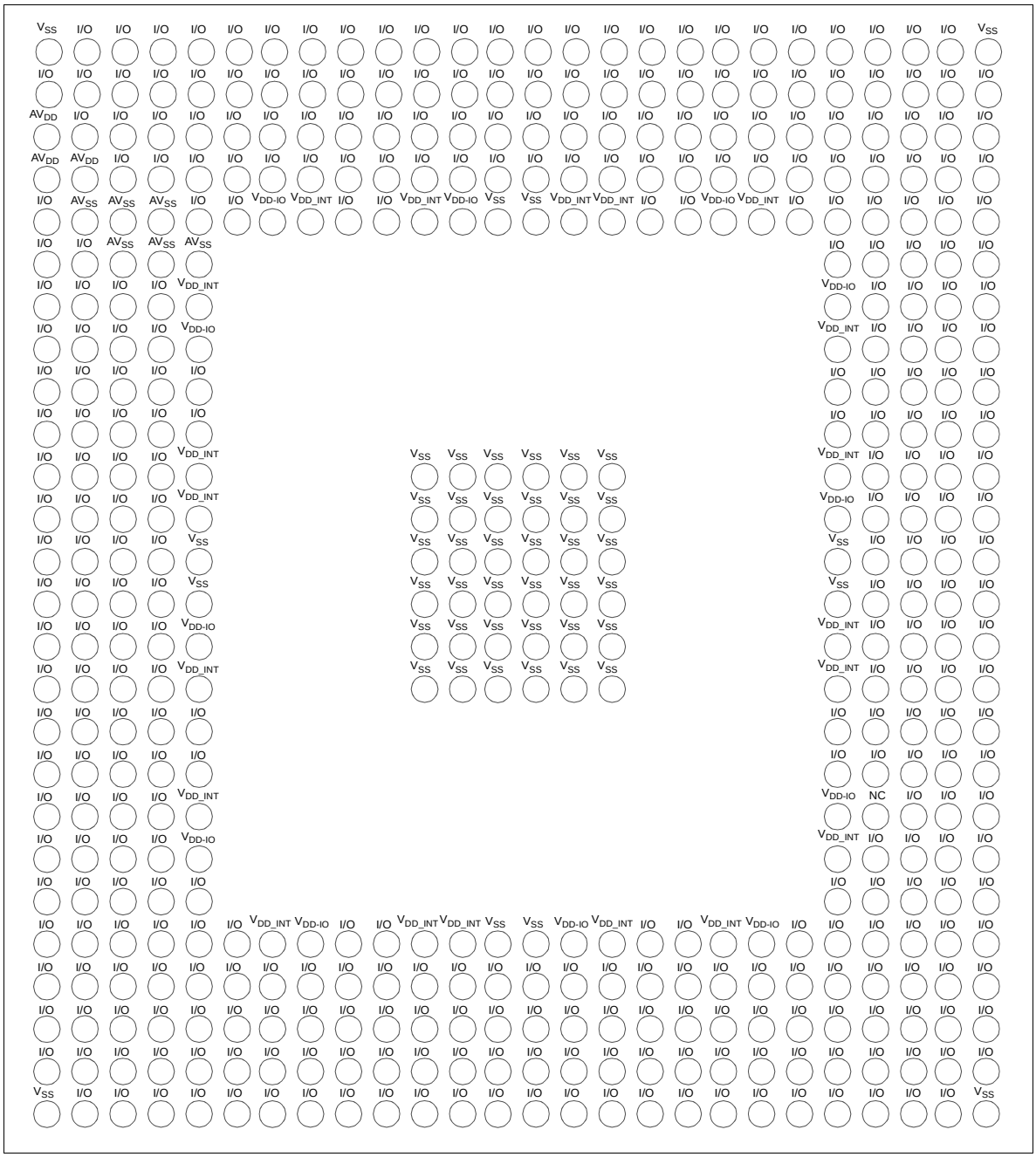
- 8-bit Motorola or Intel Address/Data De-multiplexed access mode
- 16-bit Multiplexed Address/Data access mode

OTHER

- Two DS1 monitor ports
- Ability to tristate all outputs for in-circuit testing
- IEEE 1149.1 boundary scan

PRODUCT PREVIEW

LEAD DIAGRAM



Viewed from Bottom Side

LEAD DESCRIPTIONS

VDD and Ground (80 + 9)

Symbol	Lead No.	I/O/P	Type	Name/Function
V_{DD-INT}	AB8, AB11, AB15, AB16, AB20, E7, E11, E12, E16, E19, G22, H5, L5, L22, M22, R5, T5, T22, W22, Y5	P		**Digital VDD:** +1.8 volt ±5% power
V_{DD-IO}	AB7, AB12, AB19, E8, E15, E20, G5, H22, M5, R22, W5, Y22	P		**Digital VDD:** +3.3 volt ±5% power
V_{SS}	A1, A26, AF1, AF26, E13, E14, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N22, N16, P5, P11, P12, P13, P14, P15, P16, P22, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AB13, AB14	P		**Digital Ground:**
AV_{DD}	AE23, AF23, AF24	P		**Analog VDD:** +1.8 volt ±5% power
AV_{SS}	AB21, AC21, AC22, AD21, AD22, AE22	P		**Analog Ground:**

Note: I=Input; O=Output; P=Power, T=Tristate

Spare Leads (1)

Symbol	Lead No.	I/O/P	Type	Name/Function
Spare	D8	I/O	TTL3V/ CMOS3V 2mA	Spare lead. Should be tied low (100 ohm pull down recommended).

Line Interface Signal and Control (Total Number of Leads: 145)

Symbol	Lead No.	I/O/P	Type	Name/Function
RE3G	L1	I	TTL3V	**Test Lead:** Should be tied low (100 ohm pull down recommended).
TE3G	M4	I	TTL3V	**Test Lead:** Should be tied low (100 ohm pull down recommended).
TDS3D	M3	O	CMOS3V 8mA	**Transmit DS3 Line Data Output (TDS3D):** Transmit C-bit parity or M13 formatted DS3 data is clocked out of the T3BwP on rising edges of the transmit clock (TDS3C).

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Symbol	Lead No.	I/O/P	Type	Name/Function
TDS3C	M2	I/O	CMOS3V 8mA	**Transmit DS3 Line Clock Output (TDS3D):** A 44.736 MHz clock which is derived from the external transmit clock input signal (XCK). When XCK fails, the T3BwP automatically switches to the RDS3C. **For Test Use:** input
RDS1D1/ RDS3D	M1	I	TTL3V	**Receive DS1 Line Data Input (RDS1D1):** This lead carries the receive NRZ data input signal for DS1 line 1. **Receive DS3 Line Data Input (RDS3D):** Use RDS1D1 Receive 44.736 Mbit/s data is clocked into the T3BwP on rising edges of the receive clock (RDS3C).
RDS1D2/LCV	N2	I	TTL3V	**Receive DS1 Line Data Input (RDS1D2):** This lead carries the receive NRZ data input signal for DS1 line 2. **DS3 Line Coding Violation Input (LCV):** Use RDS1D2 This lead is high when DS3 LIU device (i.e., DART) detects that incoming data violated B3ZS coding for bipolar violations or when three or more consecutive zeros occur in the input of data stream.
RDS1D3/$\overline{\text{EXZ}}$	P2	I	TTL3V	**Receive DS1 Line Data Input (RDS1D3):** This lead carries the receive NRZ data input signal for DS1 line 3. **DS3 Line Excessive Zeros Input ($\overline{\text{EXZ}}$):** Use RDS1D3 This lead is low when DS3 LIU device (i.e., DART) detects that three or more consecutive zeros occur in the input data stream for B3ZS coding.
RDS1D4/ $\overline{\text{DLOS}}$	R1	I	TTL3V	**Receive DS1 Line Data Input (RDS1D4):** This lead carries the receive NRZ data input signal for DS1 line 4. **DS3 Line Digital LOS Input ($\overline{\text{DLOS}}$):** Use RDS1D4 This lead is low when DS3 LIU device (i.e., DART) detects digital LOS.
RDS1D5/ $\overline{\text{ALOS}}$	R4	I	TTL3V	**Receive DS1 Line Data Input (RDS1D5):** This lead carries the receive NRZ data input signal for DS1 line 5. **DS3 Line Analog LOS Input ($\overline{\text{ALOS}}$):** Use RDS1D5 This lead is low when DS3 LIU device (i.e., DART) detects analog LOS.
RDS1D6/ $\overline{\text{DS3BIST}}$	T3	I	TTL3V	**Receive DS1 Line Data Input (RDS1D6):** This lead carries the receive NRZ data input signal for DS1 line 6. **DS3 LIU Built-In Self Test Input:** Use RDS1D6 An active low pulse to indicate that an invalid PRBS pattern. This lead is high when a valid unframed PRBS pattern is detected by DS3 LIU device (i.e., DART).

Symbol	Lead No.	I/O/P	Type	Name/Function
RDS1D7/ CDT	U2	I	TTL3V	**Receive DS1 Line Data Input (RDS1D7):** This lead carries the receive NRZ data input signal for DS1 line 7. **Transmit C-Bit Data:** Use RDS1D7 The transmit gapped clock (CCKT) is provided for clocking in the following C-bits: C2, C4, C5, C6, C16, C17, C18, C19, C20, and C21. This lead shall be set to high when external logic does not provide the C-bit through CDT.
RDS1D8-21	U4, V3, W2, V5, AA1, AB1, AB2, AB3, AA5, AD2, AB5, AF2, AC5, AE4	I	TTL3V	**Receive DS1 Line Data Input (RDS1D8-22):** These leads carry the receive NRZ data input signal for DS1 lines 8 to 21. These leads should be tied high or low when using DS3 line mode.
RDS1D22-28	AF4, AC7, AD7, AE7, AF7, AF8, AF9	I/O	TTL3V/ CMOS3V 2mA	**Receive DS1 Line Data Input (RDS1D22-28):** These leads carry the receive NRZ data input signal for DS1 lines 22 to 28. These leads should be tied high or low when using DS3 line mode. **For Test Use:** output
RDS1C1/ RDS3C	N3	I	TTL3V	**Receive DS1 Line Clock Input (RDS1C1):** An input for the 1544 KHz recovered clock from the external line interface transceiver for DS1 line 1. Control bit RXCP determines the clock edge on which the received line signals are to be clocked in (1 for rising edge). **Receive DS3 Line Clock Input (RDS3C):** Use RDS1C1 A 44.736 MHz clock is used as the time base for demultiplexing the DS3 data. When the loop timing feature is active (via LPTIME), or when the DS3 external transmit clock (XCK) fails, this clock becomes the transmit clock.
RDS1C2-21	P1, P4, R3, T2, U1, V1, V2, V4, W3, W4, AA2, AA3, AA4, AD1, AC3, AD3, AE2, AD4, AF3, AC6	I	TTL3V	**Receive DS1 Line Clock Input (RDS1C2-21):** Input for the 1544 KHz recovered clock from the external line interface transceiver for DS1 lines 2-21. These leads should be tied high or low when using DS3 line mode.
RDS1C22-28	AD6, AE6, AC8, AD8, AC9, AE9, AB10	I/O	TTL3V/ CMOS3V 2mA	**Receive DS1 Line Clock Input (RDS1C22-28):** Input for the 1544 KHz recovered clock from the external line interface transceiver for DS1 lines 22-28. These leads should be tied high or low when using DS3 line mode. **For Test Use:** output

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Symbol	Lead No.	I/O/P	Type	Name/Function
RBPVn (n=1-28)	N4, N1, P3, R2, T1, T4, U3, U5, W1, Y1, Y2, Y3, Y4, AC1, AC2, AB4, AE1, AC4, AE3, AB6, AD5, AE5, AF5, AF6, AB9, AE8, AD9, AC10	I	TTL3V	**Receive Bipolar Violation Indication Input:** The RBPVn lead provides an input for indications of external bipolar violations detected in the external line interface transceiver. A high indicates a bipolar violation, and increments the internal 16-bit coding violation counter. A bipolar violation is clocked in on rising edges of the receive line clock RDS1Cn. These leads should be tied low if not used.
TDS1D1/ RAIS	C7	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D1):** This lead carries the transmit NRZ data output signal for DS1 line 1. **DART Receive AIS Enable Output (RAIS):** Use TDS1D1 When RAIS is low, it enables generation of framed DS3 AIS on the receiver outputs of DS3 LIU (i.e., DART).
TDS1D2/ RXDIS	B6	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D2):** This lead carries the transmit NRZ data output signal for DS1 line 2. **DART Receive Output Disable Output (RXDIS):** Use TDS1D2 When RXDIS is low, it forces the receiver RP/RD and RN outputs of DS3 LIU (i.e., DART) to a low state.
TDS1D3/ TRLBK	D7	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D3):** This lead carries the transmit NRZ data output signal for DS1 line 3. **DART Terminal Loopback Enable Output (TRLBK):** Use TDS1D3 When TRLBK is low, it enables a digital loopback from the transmitter inputs to the receiver terminal side in DS3 LIU (i.e., DART).
TDS1D4/ LNLBK	B5	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D4):** This lead carries the transmit NRZ data output signal for DS1 line 4. **DART Line Loopback Enable Output (LNLBK):** Use TDS1D4 When is low, it enables an internal line loopback from the DI1/DI2 to the DOUT or DO1/DO2 outputs in DS3 LIU (i.e., DART).
TDS1D5/ ZERO	D6	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D5):** This lead carries the transmit NRZ data output signal for DS1 line 5. **DART Transmit Zero cable Enable Output (ZERO):** Use TDS1D5 When ZERO is low, it improves DOUT output mask for short cable length in DS3 LIU (i.e., DART).

Symbol	Lead No.	I/O/P	Type	Name/Function
TDS1D6/ DSXDIS	C4	O	CMOS3V 2mA	**Transmit DS1 Line Data (TDS1D6):** This lead carries the transmit NRZ data output signal for DS1 line 6. **DART Transmit DSX Output Disable (DSXDIS):** Use TDS1D6 When DSXDIS is low, it disables DOUT output and enable DO1/DO2 outputs in DS3 LIU (i.e., DART).
TDS1D7/ TEST0	B4	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D7):** This lead carries the transmit NRZ data output signal for DS1 line 7. **DART Test-in 0 Output (TEST0):**Use TDS1D7 When TEST0 is low, it enables an internal PRBS generator in DS3 LIU (i.e., DART).
TDS1D8/ TEST1	B3	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D8):** This lead carries the transmit NRZ data output signal for DS1 line 8. **DART Test-in 1 Output (TEST1):** Use TDS1D8 When TEST1 is low, it enables an internal analog terminal side loopback from the TP/TD and TN signals to the receiver outputs in DS3 LIU (i.e., DART).
TDS1D9/ PAT23	B2	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D9):** This lead carries the transmit NRZ data output signal for DS1 line 9. **DART PRBS 2^{23} Select Output (PAT23):** Use TDS1D8 When is low, it selects a 2^{23}-1 pattern for the PRBS analyzer and generator for DS3 LIU (i.e., DART). When this lead is high, it selects a 2^{15}-1 pattern.
TDS1D10/DJ SEL0	D4	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D10):** This lead carries the transmit NRZ data output signal for DS1 line 10. **Dejitter Block Control 0 Output (DJSEL0):** Use TDS1D10 1 of 2 control leads which control the dejitter buffer/dejitter PLL modes of DS3 LIU (i.e., DART).
TDS1D11/ DJSEL1	C2	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D11):** This lead carries the transmit NRZ data output signal for DS1 line 11. **Dejitter Block Control 1 Output (DJSEL1):** Use TDS1D11 1 of 2 control leads which control the dejitter buffer/dejitter PLL modes of DS3 LIU (i.e., DART).
TDS1D12/ DIVSEL	B1	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D12):** This lead carries the transmit NRZ data output signal for DS1 line 12. **Divide Select Output (DIVSEL):** Use TDS1D12 Selects the divisor in the divide-by block in the dejitter PLL of DS3 LIU (i.e., DART).
TDS1D13/ CCKT	C1	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D13):** This lead carries the transmit NRZ data output signal for DS1 line 13. **Transmit C-Bit Clock:** Use TDS1D13 A gapped clock signal is provided for clocking in selected transmit C-bit data (CDT). Data is clocked in on positive transitions.

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Symbol	Lead No.	I/O/P	Type	Name/Function
TDS1D14/ CFMT	D2	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D14):** This lead carries the transmit NRZ data output signal for DS1 line 14. **Transmit C-Bit Framing Pulse:** Use TDS1D14 This positive framing pulse occurs prior to the C2 bit.
TDS1D15/ CDCCT	D1	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D15):** This lead carries the transmit NRZ data output signal for DS1 line 15. **Transmit Data Link Indication:** Use TDS1D15 A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15).
TDS1D16/ CCKR	E1	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D16):** This lead carries the transmit NRZ data output signal for DS1 line 16. **Receive C-Bit Clock:** Use TDS1D16 A gapped clock signal is provided for clocking out the selected receive C-bit data. Data (CDR) is clocked out on positive transitions.
TDS1D17/ CDR	F3	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D17):** This lead carries the transmit NRZ data output signal for DS1 line 17. **Receive C-Bit Data:** Use TDS1D17 The following C-bits are provided at this interface: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21.
TDS1D18/ CFMR	F5	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D18):** This lead carries the transmit NRZ data output signal for DS1 line 18. **Receive C-Bit Framing Pulse:** Use TDS1D18 This positive framing pulse occurs prior to the C2 bit.
TDS1D19/ CDCCR	G3	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D19):** This lead carries the transmit NRZ data output signal for DS1 line 19. **Receive Data Link Indication:** Use TDS1D19 A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15).
TDS1D20-28	H4, J5, G1, J4, J3, J2, J1, K2, L4	O	CMOS3V 2mA	**Transmit DS1 Line Data Output (TDS1D20-28):** These leads carry the transmit NRZ data output signal for DS1 lines 20-28.
TDS1C1-28	E6, A6, C6, A5, C5, A4, D5, A3, A2, E5, E4, C3, D3, F4, E3, E2, G4, F2, F1, G2, H3, H2, H1, K5, K4, K3, K1, L3	I/O	TTL3V/ CMOS3V 2mA	**Transmit DS1 Line Clock Output (TDS1C1-28):** A 1544 KHz clock output for DS1 lines 1-28. Control bit TXCP determines the clock edge on which the received line signals are to be clocked out (1 for rising edge). If DS3 line interface is selected, set TXCP to '0'. **For Test Use:** input/output

Symbol	Lead No.	I/O/P	Type	Name/Function
XCK	L2	I	TTL3V	**External Transmit Clock Input (XCK):** An external clock having a frequency of 44.736 MHz and a stability of +/- 20 PPM is required to meet DSX-3 cross-connect requirements. The clock duty cycle shall be kept to (50 +/- 5)%. When the XCK fails, the device switches to RDS3C for multiplexer operation. This lead should be tied high if not used (4.7 k ohm pull up recommended).

System Side Interface Signals (175)

Symbol	Lead No.	I/O/P	Type	Name/Function
RCLK1/ CT_Frm_8/ RSYNC_2	E25	O	PCI	Transmission/Unframed Mode: **Receive Clock Output (RCLK1)**: This clock is used to clock the RDATA1 and RFRM1. The RDATA1 and RFRM1 are clocked out on the falling edge clock transition. H.100/H.110 Mode: **8 MHz Frame Sync Output (CT_Frm_8)**: Use RCLK1 It has a period of 125 µsec. MVIP Mode: **2 MHz Frame Sync output (RSYNC_2):** Use RCLK1 This is a negative true pulse with a period of 125 µsec.
RCLK2/ RSYNC_64	F23	O	CMOS3V 4mA	Transmission/Unframed Mode **Receive Clock Output (RCLK2)**: This clock is used to clock the RDATA2 and RFRM2. H.100/H.110/MVIP Mode: **64 MHz Frame Sync Output (RSYNC_64)**: For test use only.
RCLK3/ CT_CLK_8/ RCLK_2	G24	O	PCI	Transmission/Unframed Mode: **Receive Clock Output (RCLK3)**: This clock is used to clock the RDATA3 and RFRM3. H.100/H.110 Mode: **8 MHz Clock Output (CT_CLK_8)**: Use RCLK3 The clock frequency is 8.192 MHz. The duty cycle of this signal is nominally 50%. MVIP Mode: **2 MHz Clock Output (RCLK_2)**: Use RCLK3 The clock frequency is 2.048 MHz. The duty cycle of this signal is nominally 50%.
RCLK4/ RCLK_64	J22	O	CMOS3V 4mA	Transmission/Unframed Mode: **Receive Clock Output (RCLK4)**: This clock is used to clock the RDATA4 and RFRM4. H.100/H.110/MVIP Mode: **64 MHz Clock Output (RCLK_64)**: For test use only.

Symbol	Lead No.	I/O/P	Type	Name/Function
RCLK5-16	H25, H26, K23, K25, L24, M23, M26, N25, P26, R26, R23, T24	O	CMOS3V 4mA	Transmission/Unframed Mode: **Receive Clock Output (RCLK5-16)**: This clock is used to clock the RDATAn and RFRMn.
RCLK17/ RxCellPkt	U25	O	CMOS3V 8mA	Transmission/Unframed Mode: **Receive Clock Output (RCLK17)**: This clock is used to clock the RDATA17 and RFRM17. Clear channel mode: **Rx Cell/Packet Indication (RxCellPkt)**: Use RCLK17 When is low, it indicates the data byte is a packet payload. When is high, it indicates the data is a cell payload.
RCLK18/RxClk	U23	O	CMOS3V 4mA	Transmission/Unframed Mode: **Receive Clock Output (RCLK18)**: This clock is used to clock the RDATA18 and RFRM18. Clear Channel Mode: **Rx Clock Output (RxCLK)**: Use RCLK18 The clock frequency is 6.25 MHz. The duty cycle of this signal is nominally 50%.
RCLK19-28/ RLCnum0-9	V24, W25, V22, AA26, AB26, AB25, AA22, AB24, AD25, AC23	O	CMOS3V 4mA	Transmission/Unframed Mode: **Receive Clock Output (RCLK19-28)**: This clock is used to clock the RDATA18 and RFRM18. Clear Channel Mode: **Rx Link Channel Number Output (RLCnum0-9)**: Use RCLK19-28
RDATA1-8/ CTD0-7	E26, G23, F26, G25, G26, J24, J25, K24	I/O	PCI3V/ PCI	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA1-8):** This lead carries the time slots from the T3BwP to the system side. H.100/H.110 Mode: **Data Highway Input/Output (CTD0-7):** Serial Data lines 0-7. These leads can be tristated.
RDATA9-17	L23, L26, M25, N24, P23, P25, R24, T25, U26	O	CMOS3V 2mA	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA9-17):** This lead carries the time slots from the T3BwP to the system side.

Symbol	Lead No.	I/O/P	Type	Name/Function
RDATA18/ RCLKX8	V26	O	CMOS3V 4mA	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA18):** This lead carries the time slots from the T3BwP to the system side. Clear Channel mode: **Rx Clock x 8 (RCLKX8)**: Use RCLK18 Synchronous high speed serial clock (RCLKX8) for multi-cycle data processing. The clock frequency is 50 MHz. The duty cycle of this signal is nominally 50%.
RDATA19/ $\overline{\text{RxValid}}$	U22	O	CMOS3V 4mA	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA19):** This lead carries the time slots from the T3BwP to the system side. Clear Channel mode: **Rx Valid Signal Output ($\overline{\text{RxValid}}$)**: Use RCLK19 Active low when clear channel mode is enabled. It indicates the valid data byte when it is asserted.
RDATA20/ $\overline{\text{TxValid}}$	V23	O	CMOS3V 4mA	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA20):** This lead carries the time slots from the T3BwP to the system side. Clear Channel mode: **Tx Valid Signal Output ($\overline{\text{TxValid}}$)**: Use RCLK20 Active low when clear channel mode is enabled. It indicates the valid data byte when it is asserted.
RDATA21-28/ RxData1-8	W24, W23, AA25, AA24, AA23, AD26, AC24, AE25	O	CMOS3V 4mA	Unframed/Transmission/MVIP Mode: **Receive Data Highway Output (RDATA21-28):** This lead carries the time slots from the T3BwP to the system side. Clear Channel mode: **Rx Data Output (RxData1-8)**: Use RCLK21-28 When clear channel is enabled, the received data is clocked out from T3BwP on the negative edge of RxClk.
RFRM1-8/ RSIG1-8/ CTD8-15	D26, F24, F25, H23, H24, J23, K22, J26	I/O(T)	PCI3V/ PCI	Transmission Mode: **Receive Frame Pulse output (RFRM1-8):** This signal is used to synchronize external system circuitry from the T3BwP. For the transmission mode, the T3BwP sources the frame pulse and clock. MVIP Mode: **Receive Signaling Highway Output (RSIG1-8):** This lead carries to the system the signals that represent signaling information H.100/H.110 Mode: **Data Highway Input/Output (CTD8-15):** Serial Data lines 8-15. These leads can be tristated.

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Symbol	Lead No.	I/O/P	Type	Name/Function
RFRM9-16/ RSIG9-16	K26, L25, M24, N23, N26, P24, R25, T26	O	CMOS3V 2mA	Transmission Mode: **Receive Frame Pulse Output (RFRM9-16):** This signal is used to synchronize external system circuitry from the T3BwP. For the transmission mode, the T3BwP sources the frame pulse and clock. MVIP Mode: **Receive Signaling Highway Output (RSIG9-16):** This lead carries to the system the signals that represent signaling information.
RFRM17/ RSIG17/ TxCellPkt	T23	O	CMOS3V 8mA	Transmission Mode: **Receive Frame Pulse Output (RFRM17):** This signal is used to synchronize external system circuitry from the T3BwP. For the transmission mode, the T3BwP sources the frame pulse and clock. MVIP Mode: **Receive Signaling Highway Output (RSIG178):** This lead carries to the system the signals that represent signaling information. Clear channel mode: **Tx Cell/Packet Indication (TxCellPkt)**: Use RFRM17 When is low, it indicates the data byte is a packet payload. When is low, it indicates the data is a cell payload.
RFRM18/ RSIG18/ TxClk	U24	O	CMOS3V 4mA	Transmission Mode: **Receive Frame Pulse Output (RFRM18):** This signal is used to synchronize external system circuitry from the T3BwP. For the transmission mode, the T3BwP sources the frame pulse and clock. MVIP Mode: **Receive Signaling Highway Output (RSIG18):** This lead carries to the system the signals that represent signaling information. Clear channel mode: **Tx Clock Output (TxCLK)**: Use RFRM18 The clock frequency is 6.25 MHz. The duty cycle of this signal is nominally 50%.

Symbol	Lead No.	I/O/P	Type	Name/Function
RFRM19-28/ RSIG19-28/ TLCnum0-9	V25, W26, Y26, Y25, Y24, Y23, AC26, AC25, AB23, AE26	O	CMOS3V 4mA	Transmission Mode: **Receive Frame Pulse Output (RFRM19-28):** This signal is used to synchronize external system circuitry from the T3BwP. For the transmission mode, the T3BwP sources the frame pulse and clock. MVIP Mode: **Receive Signaling Highway Output (RSIG19-28):** This lead carries to the system the signals that represent signaling information. Clear channel mode: **Tx Link Channel Number Output (TLCnum0-9)**: Use RFRM19-28
TCLK1/ CT_Frm_A/ TSYNC_2_A	E24	I	$TTL3V_{ST}$	Transmission/Unframed Mode: **Transmit Clock Input (TCLK1):** This clock is sourced from the system. It is used to clock in the TFRM1 and TDATA1 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **Frame Sync Input (CT_Frm_A)**: Use TCLK1 This is a negative true pulse that straddles the beginning of the first bit of the first time-slot. It is driven by the 'A' clock master. It has a period of 125 µsec. MVIP Mode: **2 MHz Frame Sync Input (TSYNC_2_A):** Use TCLK1 This is a negative true pulse that straddles the beginning of the first bit of the first time-slot. It has a period of 125 µsec.
TCLK2/ CT_C8_A/ TCLK_2_A	F22	I	$TTL3V_{ST}$	Transmission/Unframed Mode: **Transmit Clock Input (TCLK2):** This clock is sourced from the system. It is used to clock in the TFRM2 and TDATA2 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **Bit Clock Input (CT_C8_A)**: Use TCLK2 The clock frequency is 8.192 MHz driven by 'A' clock master. The duty cycle of this signal is nominally 50%. MVIP Mode: **2 MHz Clock Input (TCLK_2_A)**: Use TCLK2 The clock frequency is 2.048 MHz. The duty cycle of this signal is nominally 50%.

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Symbol	Lead No.	I/O/P	Type	Name/Function
TCLK3/ TSYNC_64_A	C25	I	TTL3V	Transmission/Unframed Mode: **Transmit Clock Input (TCLK3):** This clock is sourced from the system. It is used to clock in the TFRM3 and TDATA3 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110/MVIP Mode: **64 MHz Frame Sync Input (TSYNC_64_A)**: For test use only. This lead should be tied high if not used (4.7 k ohm pull up recommended).
TCLK4/ TCLK_64_A	B26	I	TTL3V	Transmission/Unframed Mode: **Transmit Clock Input (TCLK4):** This clock is sourced from the system. It is used to clock in the TFRM4 and TDATA4 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110/MVIP Mode: **64 MHz Clock Input (TCLK_64A)**: For test use only. This lead should be tied high if not used (4.7 k ohm pull up recommended).
TCLK5/ CT_Frm_B	A25	I	$TTL3V_{ST}$	Transmission/Unframed Mode: **Transmit Clock Input (TCLK5):** This clock is sourced from the system. It is used to clock in the TFRM5 and TDATA5 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **Redundant Frame Sync Input (CT_Frm_B)**: Use TCLK5 This is a negative true pulse that straddles the beginning of the first bit of the first time-slot. It is driven by 'B' clock master. It has a period of 125 µsec.
TCLK6/ CT_C8_B	A24	I	$TTL3V_{ST}$	Transmission/Unframed Mode: **Transmit Clock Input (TCLK6):** This clock is sourced from the system. It is used to clock in the TFRM6 and TDATA6 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **Redundant Bit Clock Input (CT_C8_B)**: Use TCLK6 The clock frequency is 8.192 MHz driven by 'B' clock master. The duty cycle of this signal is nominally 50%.

Symbol	Lead No.	I/O/P	Type	Name/Function
TCLK7/ CT_EN	E21	I	TTL3V	Transmission/Unframed Mode: **Transmit Clock Input (TCLK7):** This clock is sourced from the system. It is used to clock in the TFRM7 and TDATA7 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **CT Enable (CT_EN)**: Indicates that J4 of an H.110 card is fully seated when low. CTD0-31 and CLK_8Kout are tristated when CT_EN is high. Set this lead low when hardware connection control is not implemented.
TCLK8/ CT_RESET	D21	I	TTL3V	Transmission/Unframed Mode: **Transmit Clock Input (TCLK8):** This clock is sourced from the system. It is used to clock in the TFRM8 and TDATA8 signals from system. This lead should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **CT Reset (CT_RESET)**: When low, CT bus is reset (Hi-Z). CTD0-31 and CLK_8Kout are tristated when CT_RESET is low. Set this lead high when not used.
TCLK9-28	D20, C20, B20, A20, A19, B18, C17, D16, A16, B15, C14, A13, D13, C12, B11, A10, C10, A8, D9, A7	I	TTL3V	Transmission/Unframed Mode: **Transmit Clock Input (TCLK9-28):** This clock is sourced from the system. It is used to clock in the TFRM9-28 and TDATA9-28 signals from system. These leads should be tied high if not used (4.7 k ohm pull up recommended).
TDATA1-8/ CTD16-23	D25, E23, D23, B25, B24, D22, B23, B22	I/O	PCI3V/ PCI	Transmission mode/MVIP/Unframed Mode: **Transmit Data Highway Input (TDATA1-8):** This lead carries the data time slots from the system interface to the T3BwP. These leads should be tied high if not used (4.7 k ohm pull up recommended). H.100 Mode: **Data Highway Input/Output (CTD16-23):** Serial Data lines 16-23. These leads can be tristated.
TDATA9-20	C21, A21, E18, B19, C18, D17, B17, C16, D15, A15, B14, B13	I	TTL3V	Transmission mode/MVIP/Unframed Mode: **Transmit Data Highway Input (TDATA9-28):** This lead carries the data time slots from the system interface to the T3BwP. These leads should be tied high if not used (4.7 k ohm pull up recommended).

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Symbol	Lead No.	I/O/P	Type	Name/Function
TDATA21-28/ TxData1-8	A12, D12, C11, A9, D10, E10, E9, C8	I	TTL3V	Transmission mode/MVIP/Unframed Mode: **Transmit Data Highway Input (TDATA 21-28):** This lead carries the data time slots from the system interface to the T3BwP. These leads should be tied high if not used (4.7 k ohm pull up recommended). Clear Channel mode: **Tx Data Output (TxData1-8)**: Use TDATA21-28 When clear channel is enabled, the transmit data is clocked into T3BwP on the negative edge of TxClk. These leads should be tied high if not used (4.7 k ohm pull up recommended).
TFRM1-8/ TSIG1-8/ CTD24-31	C26, D24, C24, E22 C23, C22, A23, A22	I/O	PCI3V/ PCI	Transmission Mode: **Transmit Frame Pulse Input (TFRM1-8):** This signal is used to synchronize the frame sync and is sourced by the system. These leads should be tied high if not used (4.7 k ohm pull up recommended). MVIP Mode: **Transmit Signaling Highway Input (TSIG1-8):** This lead carries from the system the signal s that represent signaling information. These leads should be tied high if not used (4.7 k ohm pull up recommended). H.100/H.110 Mode: **Data Highway Input/Output (CTD24-31):** Serial Data lines 24-31. These leads can be tristated.
TFRM9-28/ TSIG9-28	B21, D19, C19, D18, E17, A18, A17, B16, C15, D14, A14, C13, B12, A11, D11, B10, B9, C9, B8, B7	I	TTL3V	Transmission Mode: **Transmit Frame Pulse Input (TFRMn):** This signal is used to synchronize the frame sync and is sourced by the system. These leads should be tied high if not used (4.7 k ohm pull up commended). MVIP Mode: **Transmit Signaling Highway Input (TSIGn):** This lead carries from the system the signal s that represent signaling information. These leads should be tied high if not used (4.7 k ohm pull up recommended).
CLK_8Kout	AF22	O	CMOS3V 8mA	**Reference Clock Output (CLK_8Kout):** The output reference clock could be derived from one of the following: DS1 line received clock, local stratum source (1.544 MHz), or BITS (either 64 KHz or 2.048 MHz). It could be 8 KHz, 1.544 MHz, or 2.048 MHz output or direct output from selected source.
CLKDS1out	AC20	O	CMOS3V 4mA	**DS1 Clock Reference Output (CLKDS1out):** This clock reference is selected form one of recovered received clock from DS1 line N (1.544 MHz) or transmit reference clock.
DS1Frmout	AD23	O	CMOS3V 4mA	**DS1 Reference Framing Pulse Output (CLKDS1out):** This lead outputs transmit reference pulse when transmit reference clock is selected as CLKDS1out.

Symbol	Lead No.	I/O/P	Type	Name/Function
CLKRefin	AE24	I	TTL3V	**Reference Clock Input (CLKRefin):** The reference clock connected to this lead could be local stratum source (1.544 MHz), or BITS (8 KHz, 64 KHz or 2.048 MHz). This lead should be tied high if not used (4.7 k ohm pull up recommended).
DPLLClk	AF25	I	TTL3V	**Digital PLL clock Input (DPLLClk):** An external clock having a frequency of 50.0 MHz and stability of +/- 30 PPM for internal DPLL operation. The clock duty cycle shall be kept to (50 +/- 5)%.
PLL_Aux_ctrl	AD24	I	TTL3V	**PLL Bypass Control Input (PLL_Aux_ctrl):** Test use only. Should be tied low.
PLL_Aux_Clk	AB22	I	TTL3V	**PLL Bypass Clock Input (PLL_Aux_Clk):** Test use only. Should be tied low.

Note: $TTL3V_{ST}$ has Schmitt-trigger inputs.

Control Signals (9)

Symbol	Lead No.	I/O/P	Type	Name/Function
LM(2-0)	AD16, AE16, AF16	I	$TTL3V_d$	**Line interface select leads:** LM2 (DS3/E3) / LM1 (E1) / LM0 (VT) / Line Operation L / L / L / DS1 line I/F H / L / H / DS3 line I/F (clear DS3 channel) H / L / L / DS3 line I/F (DS3 to DS1) Others (Reserved) / Test mode
H100_sel	AC16	I	$TTL3V_P$	**H100/110 System Port Enable:** When set to high, the system ports 1-8 are operating under H.100/H.110. It disables the H.100/H.110 operation when set to low. This lead should be tied low when using only transmission and/or unframed modes.
$\overline{\text{RST\_SW}}$	AF17	I	$TTL3V_P$	**Reset Software:** A low to reset software.
$\overline{\text{RESET}}$	AE17	I	$TTL3V_P$	**Reset:** An active low signal for resetting and initializing the internal logic. The reset must be applied only after power is applied and the clocks have been stable for a minimum of 1 msec.
$\overline{\text{HIGHZ}}$	AD17	I	$TTL3V_P$	**High Impedance Select Input[2]:** A low forces all output leads (except TDO) to the high impedance state for board testing purposes. This lead must be held high for normal operation.
$\overline{\text{SCAN\_test}}$	AF18	I	$TTL3V_P$	**Scan Test Mode:** When set to low, put the part into scan test mode. Set to high for normal operation.

Symbol	Lead No.	I/O/P	Type	Name/Function
TEST_SE	AF21	I	$TTL3V_d$	**Test Scan Enable:** Scan flop mux control set to low for normal operation.

Notes:
1. $TTL3V_d$ input has internal pull-down resistor. $TTL3V_P$ has internal pull-up resistor.
2. All output leads can be in high impedance state.

Line Monitor Signal (4)

Symbol	Lead No.	I/O/P	Type	Name/Function
MONCLK1	AC18	O(T)	CMOS3V 2mA	**Monitor Clock Signal 1:** The MONCLK1 lead provides either a receive or transmit NRZ clock. This clock can be tristated.
MONDout1	AF20	O(T)	CMOS3V 2mA	**Monitor Data Signal 1:** The MONDTO1 in provides either a NRZ receive or transmit data signal. THis lead can be tristated.
MONCLK2	AE19	O(T)	CMOS3V 2mA	**Monitor Clock Signal 2:** The second DS1 monitor clock. The MONCLK2 lead provides either a receive or transmit NRZ clock. This clock can be tristated.
MONDout2	AD19	O(T)	CMOS3V 2mA	**Monitor Data Signal 2:** The second DS1 monitor data output. The MONDTO2 in provides either a NRZ receive or transmit data signal. This lead can be tristated.

Microprocessor Interface (23)

Symbol	Lead No.	I/O/P	Type	Name/Function
MOTO	AC15	I	TTL3V	Motorola/Intel microprocessor select. High = Motorola, Low = Intel.
ALE	AD14	O	CMOS3V 8mA	**Address Latch Enable Output (Multiplexed):** An active high enable signal generated by the microprocessor. When asserted, an address is put on the AD(15-0) bus during a read/write bus cycle.
A(7-0)/AD(15-8)	AF14, AF13, AE13, AD13, AC13, AF12, AE12, AD12	I/O	TTL3V/ CMOS3V 8mA	**Address Bus Output (Intel or Motorola Mode):** These leads are address line output that are used for accessing a register location for a read/write cycle. **Address/Data bus Input/Output (Multiplexed mode):** When the multiplexed interface is selected, it is the most significant byte during address and data phase.

Symbol	Lead No.	I/O/P	Type	Name/Function
D(7-0)/AD(7-0)	AC12, AF11, AE11, AD11, AC11, AF10, AE10, AD10	I/O	TTL3V/ CMOS3V 8mA	**Data Bus Input/Output (Intel or Motorola Mode):** Bidirectional data lines used for transferring data. **Address/Data bus Input/Output (Multiplexed mode):** When the multiplexed interface is selected, it is the least significant byte during address phase.
$\overline{SEL}$	AE14	O	CMOS3V 8mA	**Select:** A low enables data transfers between the T3BwP and the selected device.
$\overline{RD}$ or RD/$\overline{WR}$	AC14	O	CMOS3V 8mA	**Read (Intel mode) or Read/Write (Motorola mode):** Intel Mode - An active low signal generated by the T3BwP for reading the selected device register locations. Motorola Mode - An active high signal generated by the T3BwP for reading the selected device register locations. An active low signal is used to write to selected device register locations.
$\overline{WR}$	AF15	O	CMOS3V 8mA	**Write (Intel mode):** Intel Mode - An active low signal generated by T3BwP for writing to the selected device register locations.
RDY/ $\overline{DTACK}$	AE15	I	TTL3V	**Ready (Intel mode) or Data Transfer Acknowledge (Motorola mode):** Intel Mode - A high is an acknowledgment from the addressed register location that the transfer can be completed. A low indicates that the selected device cannot complete the transfer cycle, and T3BwP wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INT/ $\overline{IRQ}$	AD15	I	TTL3V	**Interrupt:** Intel Mode - A high on this input lead signals an interrupt request to the T3BwP. Motorola Mode - A low on this input lead signals an interrupt request to the T3BwP.

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Serial EEPROM Port Interface (5)

Symbol	Lead No.	I/O/P	Type	Name/Function
Reset/$\overline{OE}$	AC17	O(T)	CMOS3V 8mA	**EEPROM Reset and Output Enable:** This active low lead is used to enable the EEPROM output driver. When this lead is high, reset occurs for both the address and bit counter in EEPROM. An external 4.7 k ohm pull up resistor is needed.
SCK	AE18	O(T)	CMOS3V 8mA	**Serial EPROM Output Clock:** This clock lead is used for the serial EPROM interface.
$\overline{SCE}$	AB17	O(T)	CMOS3V 8mA	**Serial EPROM Chip Enable:** This active low lead is used to enable the serial EEPROM Chip. An external 4.7 k ohm pull up resistor is needed.
SDI	AD18	I	TTL3V	**Serial EPROM Data Input:** Data lead for the serial EPROM interface.
$\overline{LD\_OK}$	AF19	O	CMOS3V 8mA	**Load Success Indication Output:** Control signal that indicates a successful loading from the SEEPROM.

Boundary Scan (5)

Symbol	Lead No.	I/O/P	Type	Name/Function
TCK	AB18	I	TTL3V	**Test Clock:** IEEE 1149.1 test port serial scan clock.
TMS	AE20	I	TTL3V	**Test Mode Select:** IEEE 1149.1 test port mode select. This lead must be tied high (4.7 k ohm pull up recommended).
TDI	AC19	I	TTL3V	**Test Data Input:** IEEE 1149.1 test port serial scan data in. This lead must be tied high if not used (4.7 k ohm pull up recommended).
TDO	AD20	O(T)	CMOS3V 8mA	**Test Data Output:** IEEE 1149.1 test port serial scan data out.
$\overline{TRS}$	AE21	I	TTL3V	**Test Mode Reset:** IEEE 1149.1 test port reset lead. This pin can be held low (if Boundary Scan is unused) or asserted low, then high (pulsed low) to asynchronously reset the Test Access Port (TAP) controller. If using the Boundary Scan feature, after completion of a Reset this pin should be pulled up with an external resistor to comply with IEEE standard 1149.1.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD_wt}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD_IO}	-0.3	3.9		Notes 1, 4
DC input voltage	VIN	-0.5	5.5	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.8V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			20	° C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD_IO}	3.15	3.3	3.45	V	
I_{DD_IO}			389	mA	See Notes 1 and 2
P_{DD_IO}			1.4	W	See Notes 1 and 2
V_{DD_INT}	1.71	1.8	1.89	V	
I_{DD_INT}			151	mA	See Notes 1 and 2
P_{DD_INT}			0.3	W	See Notes 1 and 2
P_{DD_TOTAL}			1.7	W	

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input Parameters For TTL3V @ V_{DD-IO} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD-IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD-IO} \leq 3.45$
Input leakage current		±10 nA	±1 µA		V_{DD-IO} = 3.45, V_I = 3.3 V or 0 V
Input capacitance		3.1		pF	

Input Parameters For TTL3V$_P$ @ V_{DD-IO} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD-IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD-IO} \leq 3.45$
Input current		±10 nA	±1 µA		$V_I = V_{DD-IO}$
Input leakage current	25		65	µA	V_{DD-IO} = 3.45; Input = 0 volts
Input capacitance		3.1		pF	

Input Parameters For TTL3V$_d$ @ V_{DD-IO} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD-IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD-IO} \leq 3.45$
Input current		-10 nA	-1 µA		V_I= 0V
Input leakage current	28		71	µA	V_{DD-IO} =3.45; Input = 3.45 volts
Input capacitance		3.1		pF	

Input Parameters For TTL3V$_{ST}$ @ V_{DD-IO} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD-IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD-IO} \leq 3.45$
Input current		±10 nA	±1 µA		
Input capacitance		3.1		pF	

Output Parameters For CMOS 2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD-IO} = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD-IO} = 3.45; I_{OL} = 2.0
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage tristate		±10 nA	±1 µA	µA	0 to 3.3 V input
Output capacitance		3.1		pF	

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD-IO} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD-IO} = 3.45; I_{OL} = 4.0
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage tristate		±10 nA	±1 µA		0 to 3 V input
Output capacitance		3.1		pF	

Output Parameters For CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		7.5		pF	
V_{OH}	2.4			V	V_{DD-IO} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD-IO} = 3.45; I_{OL} = 8.0
t_{RISE}					
t_{FALL}					
Leakage tristate		±10 nA	±1 µA		0 to 3 V input

Input/Output Parameters For TTL/CMOS 2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3		5.5	V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
V_{IL}	-0.5		1.0	V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
Input leakage current		±10 nA	±1 µA		0 to 3.3 V input
Input capacitance		3.1		pF	
V_{OH}	2.4			V	$V_{DD\text{-}IO}$ = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	$V_{DD\text{-}IO}$ = 3.45; I_{OL} = 2.0
t_{RISE}				ns	
t_{FALL}				ns	

Input/Output Parameters For TTL/CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
Input leakage current		±10 nA	±1 µA		0 to 3.3 V input; see Note 1.
Input capacitance		3.1		pF	
V_{OH}	2.4			V	$V_{DD\text{-}IO}$ = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	$V_{DD\text{-}IO}$ = 3.45; I_{OL} = 8.0
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

Note: 1. The leakage current is from V_{DD}. It is most pronounced at -40 ^{O}C.

Input/Output Parameters For PCI3V/PCI: PCI compliant

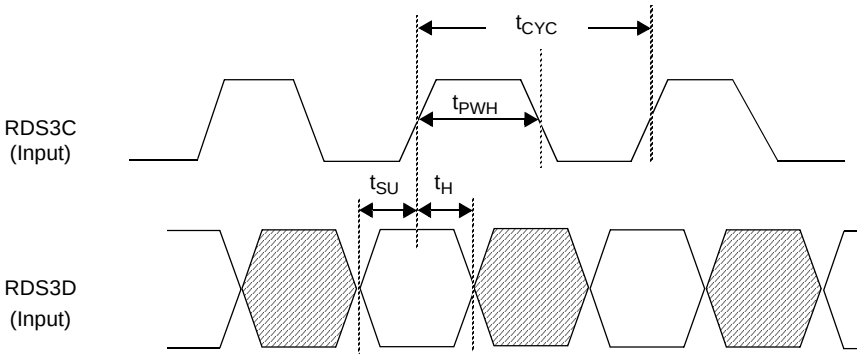
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD\text{-}IO} \leq 3.45$
Input leakage current		±10 nA	±10 µA*		0 to 3.3 V input; see Note 1.
Input capacitance		3.1		pF	
V_{OH}	2.84			V	I_{OH} = -0.5 mA
V_{OL}			0.345	V	I_{OL} = 1.5 mA

*Note: Refer to H.100/110 spec.

TIMING CHARACTERISTICS

Detailed timing diagrams for the T3BwP device are illustrated in Figures 2 through 22, with values of the timing intervals tabulated below the waveform diagrams in each figure. All output times are measured with a maximum 25 pF load capacitance, unless otherwise indicated. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated.

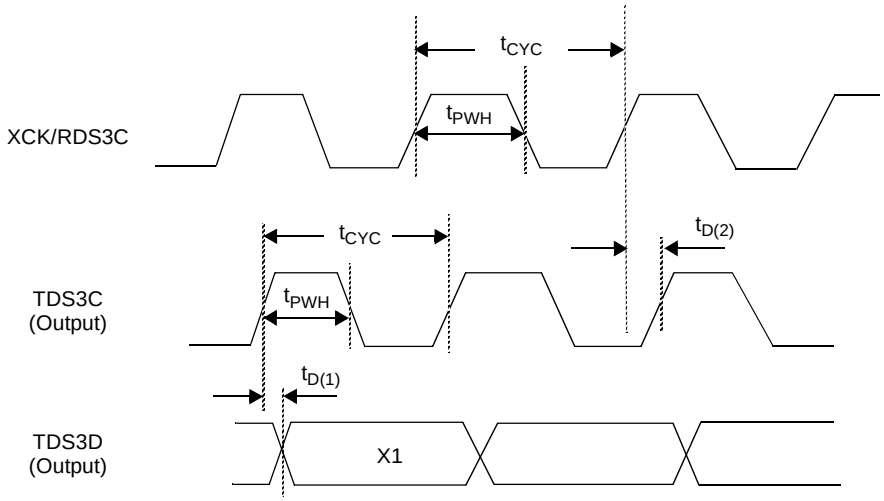
Figure 2. DS3 Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
RDS3C clock period	t_{CYC}	20.0	22.35		ns
RDS3C duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
RDS3D set-up for RDS3C↑	t_{SU}	-1.0			ns
RDS3D hold time after RDS3C↑	t_H	6.0			ns

Note: The DS3 mode is selected when leads LM2-0=HLH or HLL.

Figure 3. DS3 Transmit Timing



Parameter	Symbol	Min	Typ	Max	Unit
XCK/TDS3C clock period	t_{CYC}	20	22.35		ns
XCK/TDS3C duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TDS3DT output delay after TDS3C↑	$t_{D(1)}$	2.0		8.0	ns
TDS3CT↑ output delay after XCK/RDS3C↑	$t_{D(2)}$	5.0		17	ns

Note: The DS3 mode is selected when leads LM2-0=HLH or HLL.

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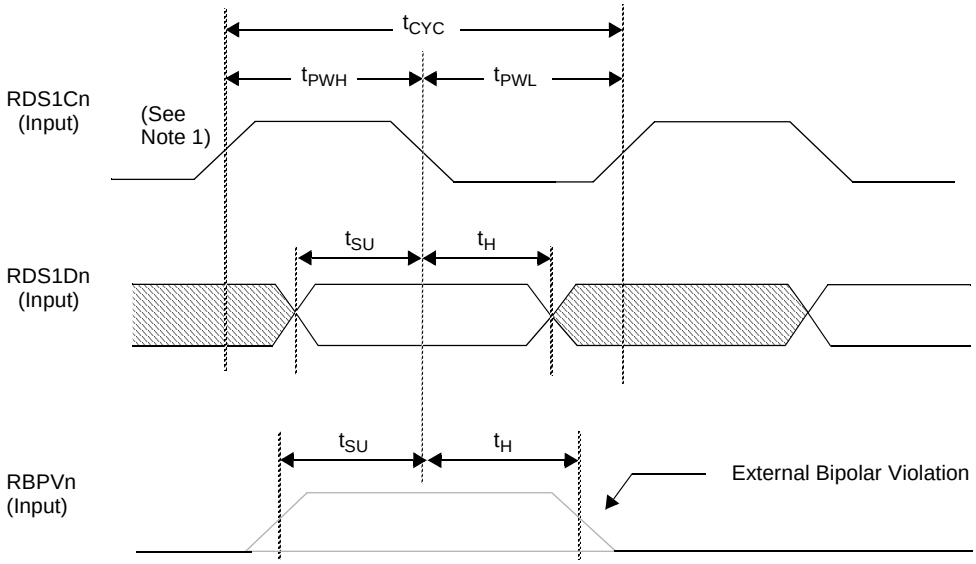
Figure 4. DS1 NRZ Receive Interface Timing (External Transceiver)



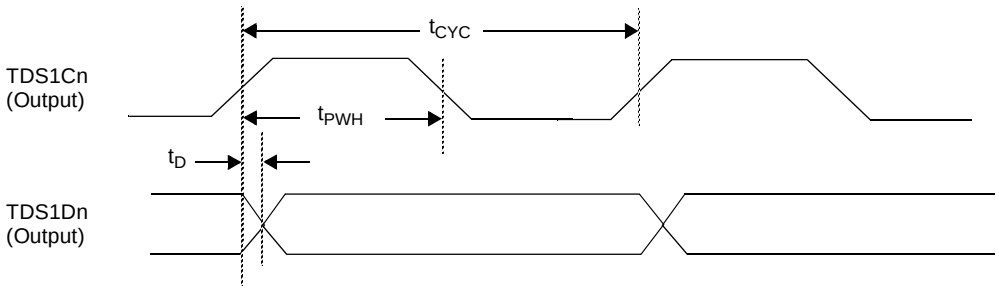
Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
RDS1Cn clock period (see Note 2)	t_{CYC}	560	648		ns
RDS1Cn high time	t_{PWH}	240	324		ns
RDS1Cn low time	t_{PWL}	240	324		ns
RDS1Dn/RBPVn set-up time to RDS1Cn↓	t_{SU}	5			ns
RDS1Dn/RBPVn hold time after RDS1Cn↓	t_H	15			ns

Notes:

1. RDS1Cn is shown for control bit RXCP (bit 6 in register X01H in framer) set to 0. RDS1Dn is clocked in on rising edges of RDS1Cn when control bit RXCP is a 1. The T3BwP accepts an inverted RDS1Dn signal when control bit RXNRZP (bit 0 in register X01H in framer) is a 1.
2. The DS1 mode is selected when leads LM2-0=LLL.

Figure 5. DS1 NRZ Transmit Interface Timing (External Transceiver)



Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
TDS1Cn clock period	t_{CYC}	637	648	656	ns
TDS1Cn duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TDS1Dn delay after TDS1Cn↑	t_D	10	15	20	ns

Notes:

1. TDS1Cn is shown for control bit TXCP (bit 7 in register X01H in framer) set to 1. TDS1Dn is clocked out on falling edges of TDS1Cn when control bit TXCP is a 0. The T3BwP provides an inverted TDS1Dn signal when control bit TXNRZP (bit 5 in register X06H in framer) is a 1.
2. The DS1 mode is selected when leads LM2-0=LLL.

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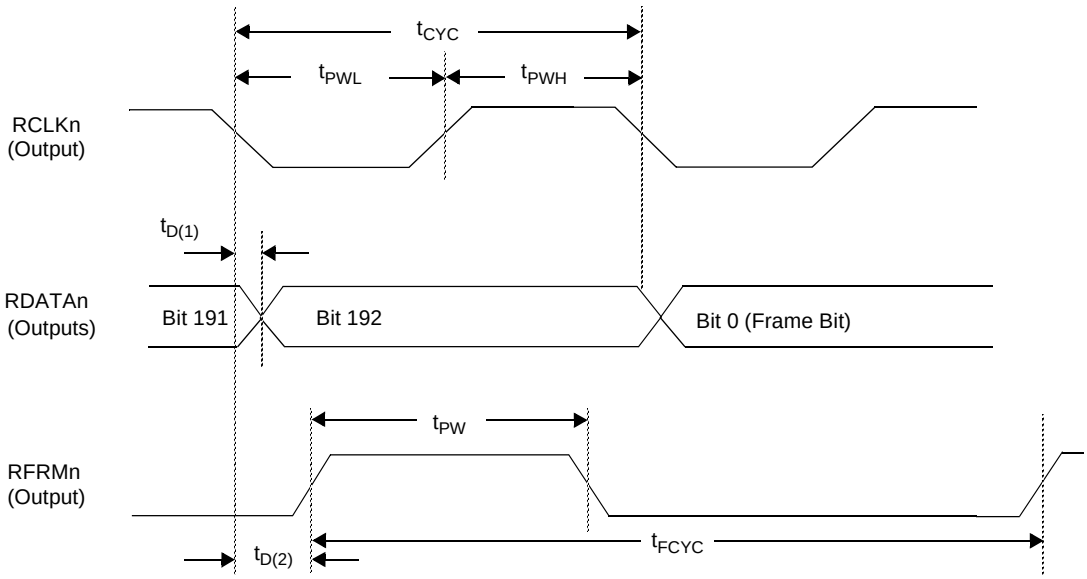
Figure 6. Receive Highway Timing - Transmission Mode (Recovered Receive Line Clock)

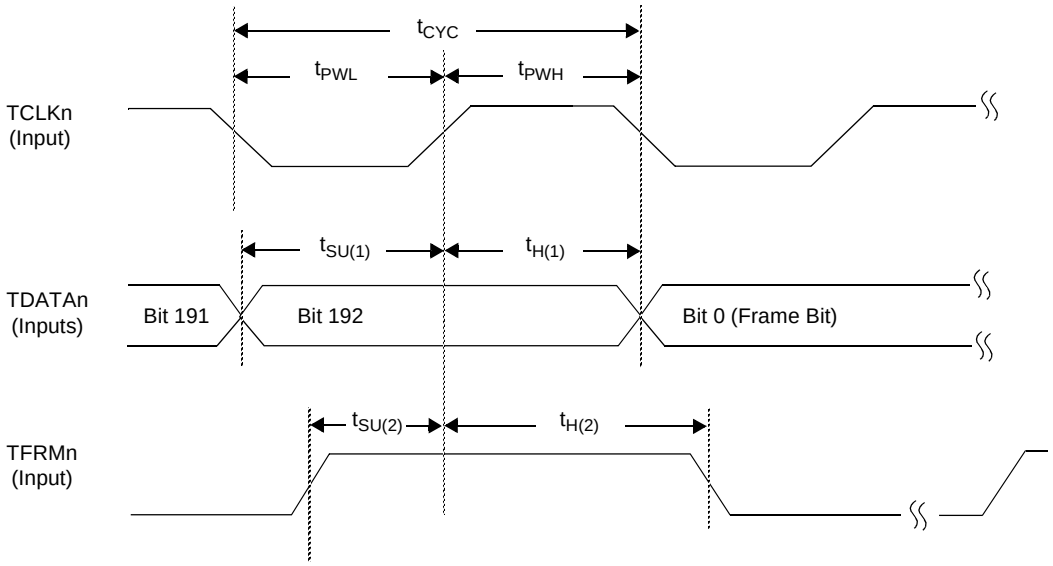


Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	560	648		ns
RCLKn low time	t_{PWL}	240	324		ns
RCLKn high time	t_{PWH}	240	324		ns
RDATAn delay after RCLKn↓	$t_{D(1)}$	5.0	10	20	ns
RFRMn delay after RCLKn↓	$t_{D(2)}$	5.0	10	20	ns
RFRMn pulse width	t_{PW}	500	648	750	ns
RFRMn period	t_{FCYC}		3.0		ms

Note: RSE enables/disables the receive slip buffer.

Figure 7. Transmit Highway Timing - Transmission Mode



Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	560	648		ns
TCLKn low time	t_{PWL}	240	324		ns
TCLKn high time	t_{PWH}	240	324		ns
TDATAn set-up time to TCLKn↑	$t_{SU(1)}$	12			ns
TDATAn hold time after TCLKn↑	$t_{H(1)}$	12			ns
TFRMn set-up time to TCLKn↑	$t_{SU(2)}$	12			ns
TFRMn hold time after TCLKn↑	$t_{H(2)}$	12			ns
TFRMn period	t_{FCYC}		3.0		ms

Note: TSE enables/disables the transmit slip buffer.

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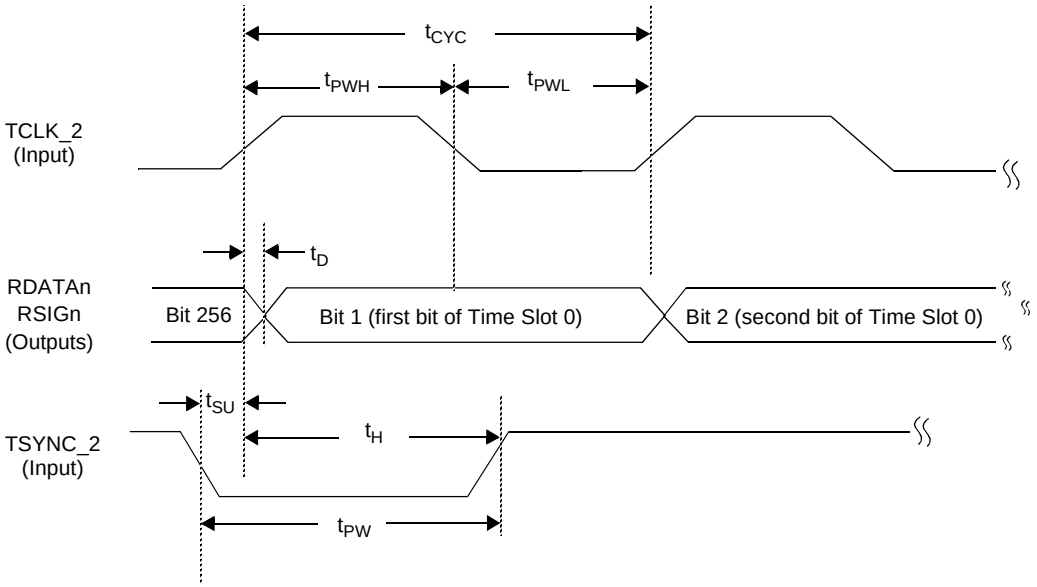
Figure 8. Receive Highway Timing - MVIP Mode

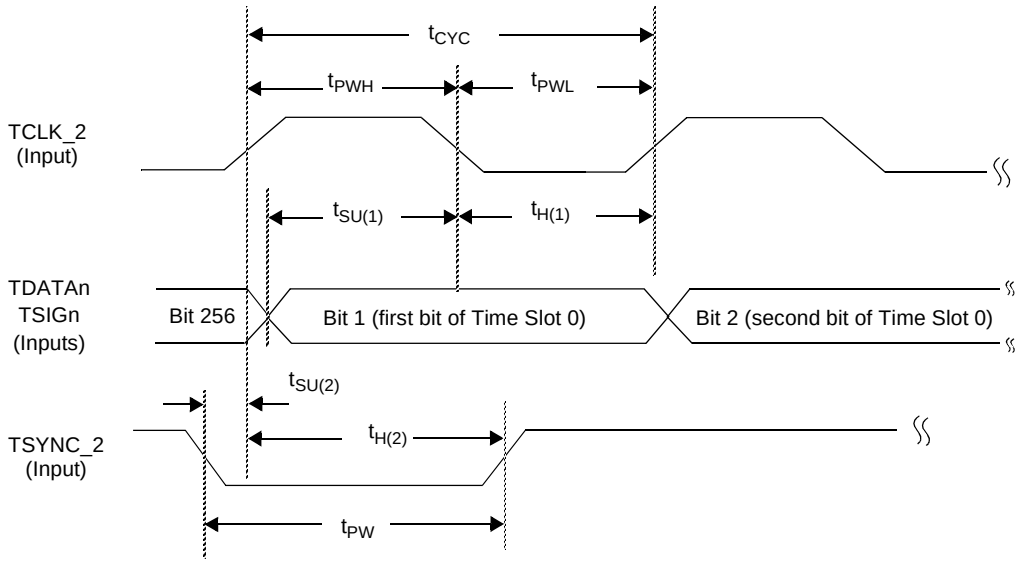


Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
TCLK_2 clock period	t_{CYC}	465	488.3	513	ns
TCLK_2 low time	t_{PWL}	220	244	268	ns
TCLK_2 high time	t_{PWH}	220	244	268	ns
RDATAn/RSIGn delay after TCLK_2↑	t_D	10	15	20	ns
TSYNC_2 set-up time to TCLK_2↑	t_{SU}	5.0			ns
TSYNC_2 hold time after TCLK_2↑	t_H	5.0			ns
TSYNC_2 pulse width low time	t_{PW}	200	488	500	ns
TSYNC_2 period	t_{FCYC}		125		µs

Note: The receive slip buffer is always enabled in this mode.

Figure 9. Transmit Highway Timing - MVIP Mode



Note: n=1 .. 28

Parameter	Symbol	Min	Typ	Max	Unit
TCLK_2 clock period	t_{CYC}	480	488.3	497	ns
TCLK_2 low time	t_{PWL}	220	244	268	ns
TCLK_2 high time	t_{PWH}	220	244	268	ns
TDATAn/TSIGn set-up time to TCLK_2	$t_{SU(1)}$	10			ns
TDATAn/TSIGn hold time after TCLK_2	$t_{H(1)}$	10			ns
TSYNC_2 set-up time to TCLK_2↑	$t_{SU(2)}$	5.0			ns
TSYNC_2 hold time after TCLK_2↑	$t_{H(2)}$	5.0			ns
TSYNC_2 pulse width low time	t_{PW}	200	488	500	ns
TSYNC_2 period	t_{FCYC}		125		µs

Note: The transmit slip buffer is always enabled in this mode.

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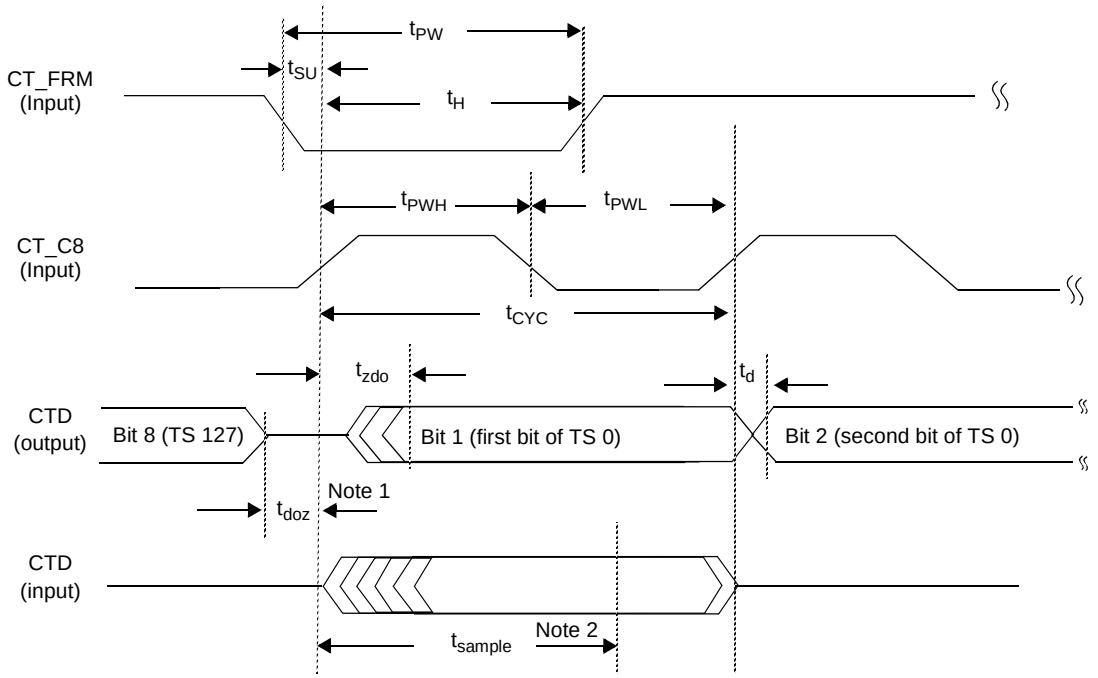
Figure 10. H.100/H.110 Data Bus Timing

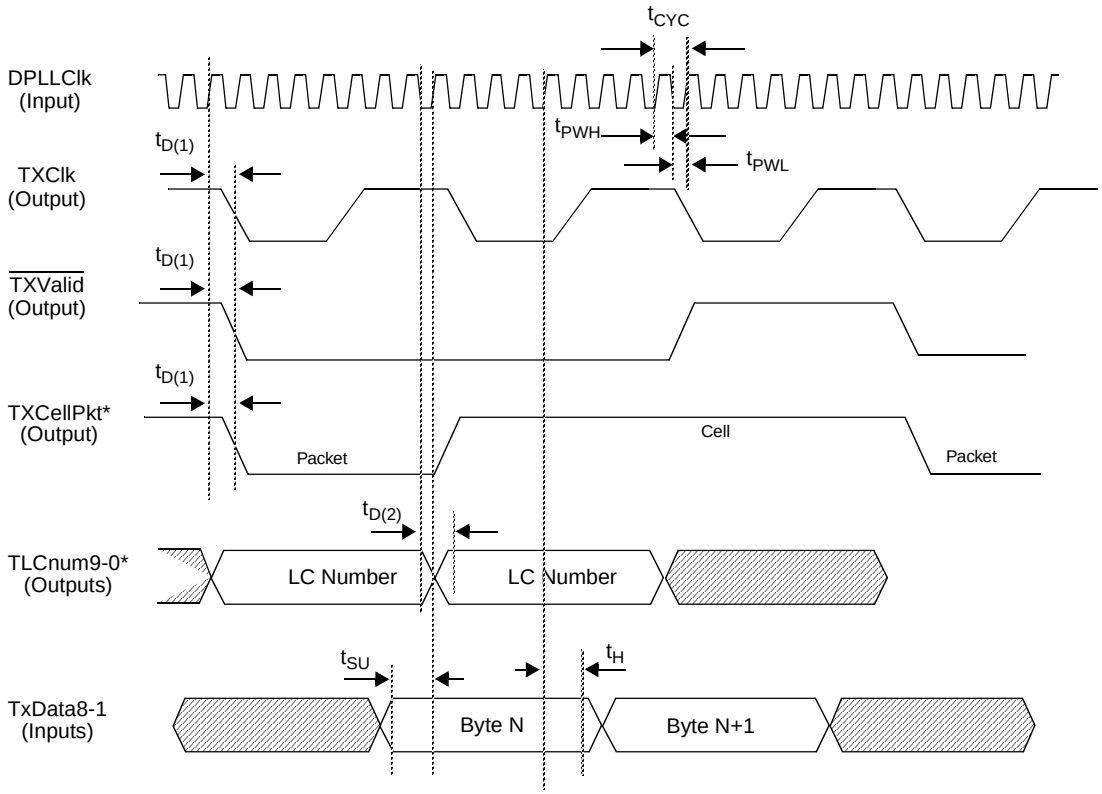


Parameter	Symbol	Min	Typ	Max	Unit
CT_C8 clock period	t_{CYC}		122		ns
CT_C8 low time	t_{PWL}	39		83	ns
CT_C8 high time	t_{PWH}	39		83	ns
CT_FRM set-up time to CT_C8↑	t_{SU}	5.0			ns
CT_FRM hold time after CT_C8↑	t_H	5.0			ns
CTD HiZ to ouput time after CT_C8↑	t_{ZDO}	0		22	ns
CTD output to HiZ time to CT_C8↑	t_{DOZ}	-20		0	ns
CTD output delay after CT_C8↑	t_D	2		22	ns
CT_FRM pulse width low time	t_{PW}	90	122	180	ns
	t_{sample}		90		ns

Notes:

1. in order to guarantee non-overlapped operation on the data bus, the last bit of time-slot N must be inactive before the first bit of time-slot N+1. Designs meeting the specified timing are guaranteed to be non-overlapping.
2. Data is nominally sampled at the 3/4 point of the bit cell.

Figure 11. DS3/NxDS0 Clear Channel Tx Direction Timing



*Note: Ignore for DS3 Clear Channel operation.

Parameter	Symbol	Min	Typ	Max	Unit
DPPClk clock period	t_{CYC}		20		ns
DPPClk low time	t_{PWL}	9	10		ns
DPPClk high time	t_{PWH}	9	10		ns
TxClk, $\overline{\text{TxValid}}$, TxCellPkt delay after DPPClk↑	$t_{D(1)}$			10	ns
TLCnum9-0 delay after DPPClk↓	$t_{D(2)}$			10	ns
TxData8-1 setup before DPPClk↑	t_{SU}	5			ns
TxData8-1 hold after DPPClk↑	t_H	0			ns

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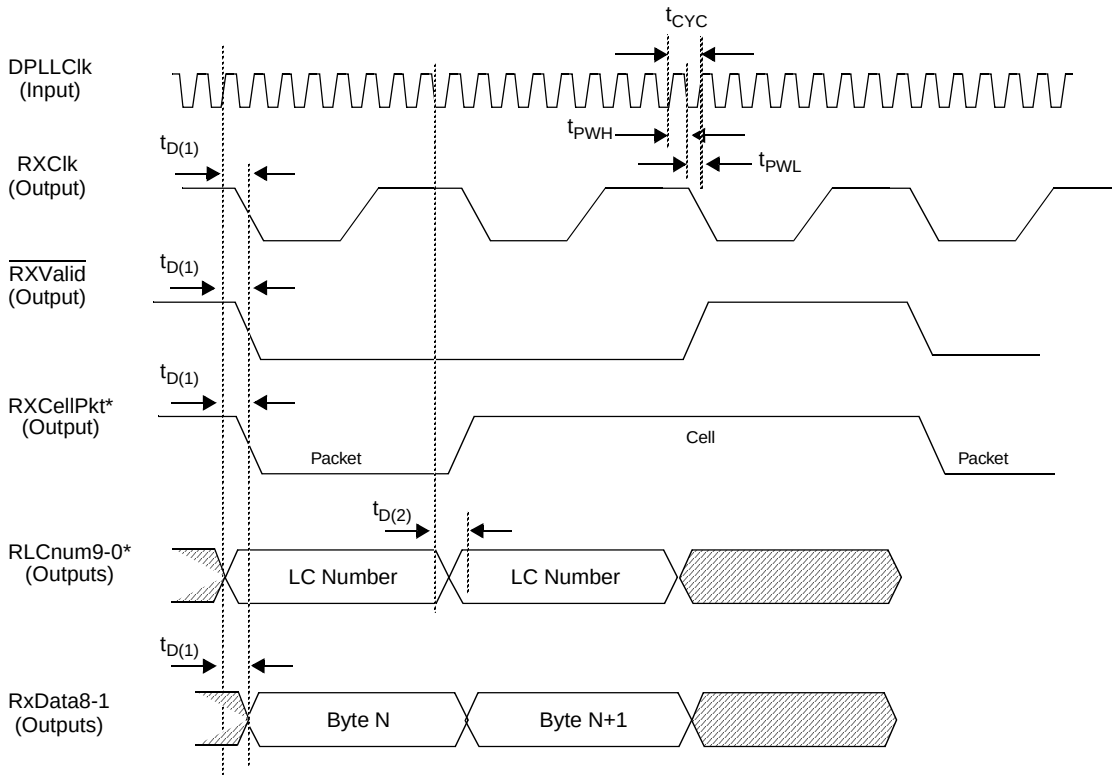
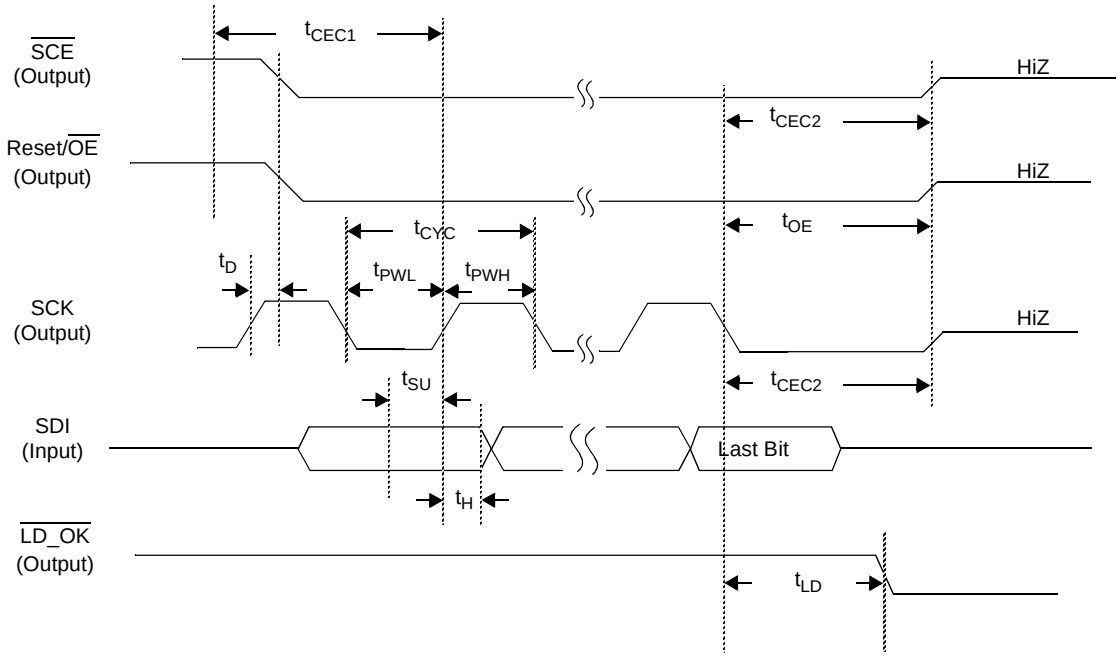
Figure 12. DS3/NxDS0 Clear Channel Rx Direction Timing



*Note: Ignored for DS3 Clear Channel operation.

Parameter	Symbol	Min	Typ	Max	Unit
DPPClk clock period	t_{CYC}		20		ns
DPPClk low time	t_{PWL}	9	10		ns
DPPClk high time	t_{PWH}	9	10		ns
RxClk, $\overline{\text{RxValid}}$, RxCellPkt delay, RxData8-1 after DPPClk↑	$t_{D(1)}$			10	ns
RLCnum9-0 delay after DPPClk↓	$t_{D(2)}$			10	ns

Figure 13. Read Instruction Timing for Serial EEPROM Interface



Parameter	Symbol	Min	Typ	Max	Unit
SCk clock period	t_{CYC}	100			ns
SCk pulse width high time	t_{PWH}	$0.4xt_{CYCLE}$		$0.6xt_{CYCLE}$	ns
SCk pulse width low time	t_{PWL}	$0.4xt_{CYCLE}$		$0.6xt_{CYCLE}$	ns
SDI set-up time before SCk↑	t_{SU}	5		t_{CYCLE}-5	ns
SDI hold time after SCk↑	t_H	0		5	ns
$\overline{SCE}$ or Reset/$\overline{OE}$ delay time to SCk↑	t_D	0		5	ns
$\overline{SCE}$ asserted/deasserted before SCK↑	t_{CEC1}			$2xt_{CYCLE}$	ns
$\overline{SCE}$/SCK time to HiZ	t_{CEC2}			$2xt_{CYCLE}$	ns
$\overline{SCE}$ pulse high to HiZ	t_{OE}			$2xt_{CYCLE}$	ns
$\overline{LD\_OK}$ pulse high to low	t_{LD}			$2xt_{CYCLE}$	ns

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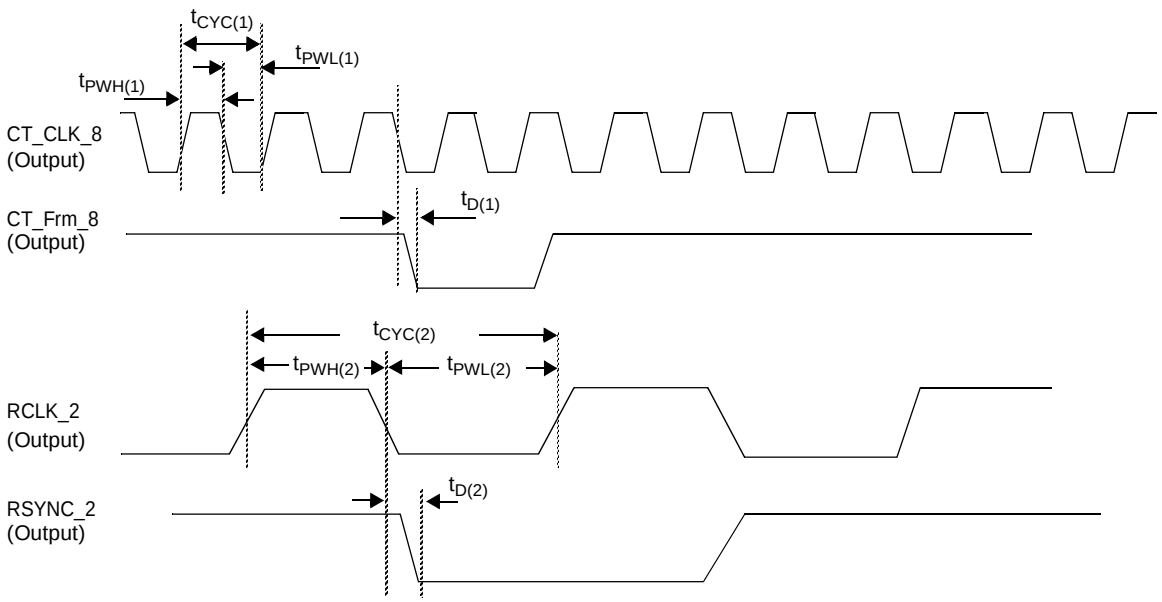
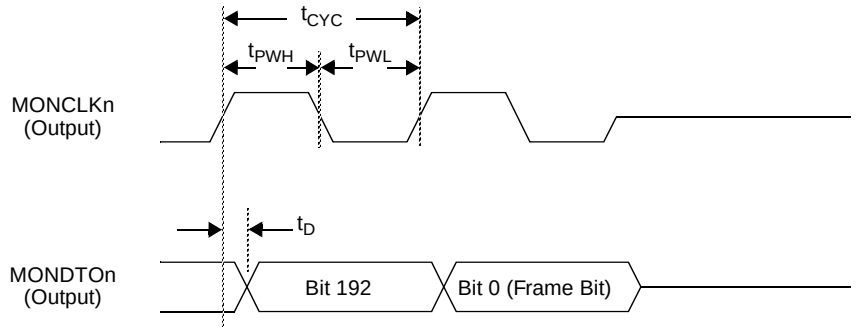
Figure 14. 8 MHz/2 MHz Clock and 8 KHz Framing Pulse



Parameter	Symbol	Min	Typ	Max	Unit
CT_CLK_8 clock period	$t_{CYC(1)}$		122		ns
CT_CLK_8 high time	$t_{PWH(1)}$		61		ns
CT_CLK_8 low time	$t_{PWL(1)}$		61		ns
RCLK_2 clock period	$t_{CYC(2)}$		488		ns
RCLK_2 high time	$t_{PWH(2)}$		244		ns
RCLK_2 low time	$t_{PWL(2)}$		244		ns
CT_Frm_8 output delay after CT_CLK_8	$t_{D(1)}$	-5		5	ns
RSYNC_2 output delay after RCLK_2	$t_{D(2)}$	-5		5	ns

Figure 15. Monitor Interface Timing

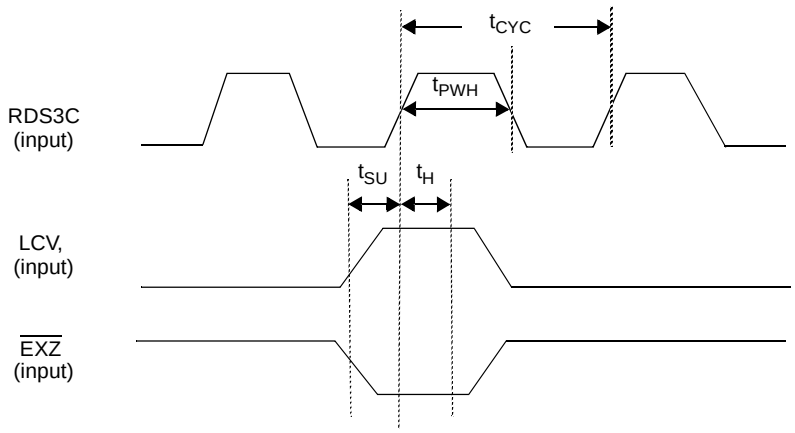


N=1, 2

Note: This timing is for Monitor Tx interface only.

Parameter	Symbol	Min	Typ	Max	Unit
MONCLKn clock period	t_{CYC}	637	648	700	ns
MONCLKn high time	t_{PWH}	240	324		ns
MONCLKn low time	t_{PWL}	240	324		ns
MONDTOn delay after MONCLK↑	t_D	5.0	10	15	ns

Figure 16. DS3 LIU LCU and EXZ Timing



Parameter	Symbol	Min	Typ	Max	Unit
RDS3C clock period	t_{CYC}	20.0	22.35		ns
RDS3C duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
LCV/$\overline{EXZ}$ set-up for RDS3C↑	t_{SU}	2.0			ns
LCV/$\overline{EXZ}$ hold time after RDS3C↑	t_H	2.0			ns

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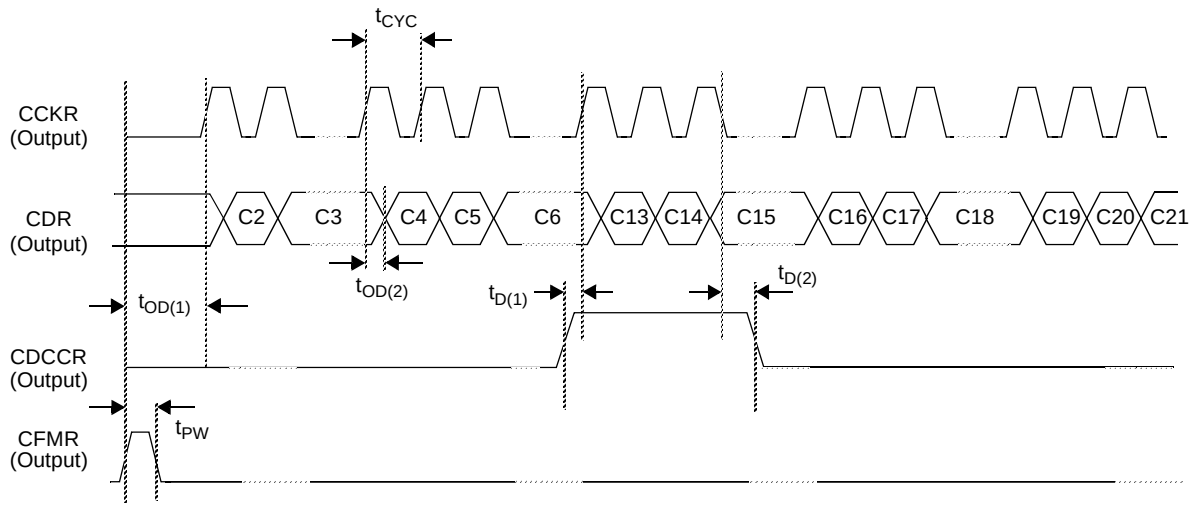
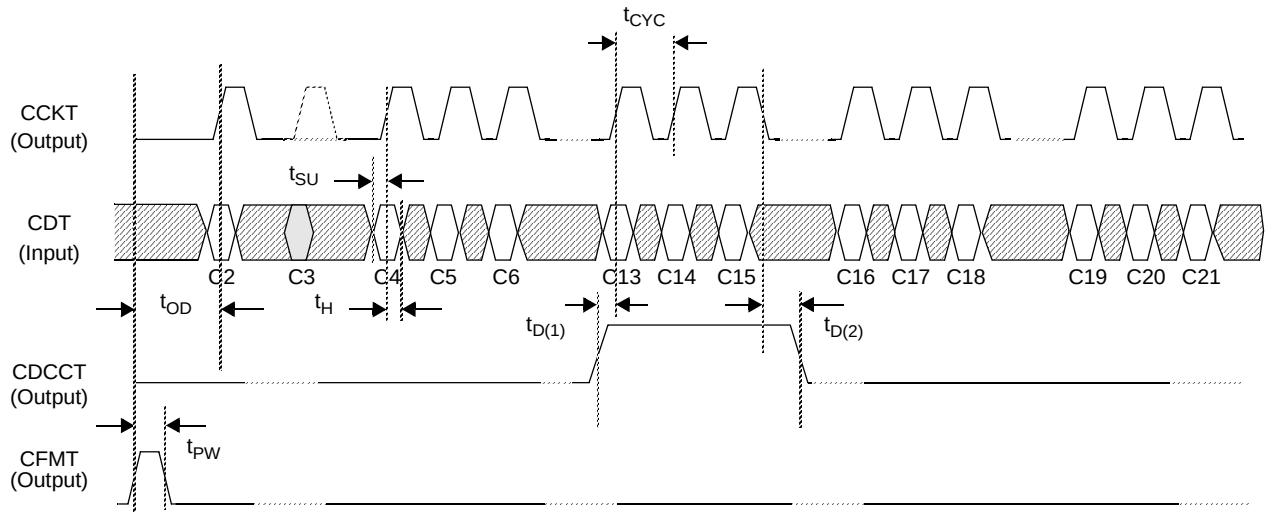
Figure 17. C-Bit Receive Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
CCKR clock period	t_{CYC}		3800		ns
CCKR output delay after CFMR↑	$t_{OD(1)}$		3800		ns
CDR output delay after CCKR↑	$t_{OD(2)}$	0	13	20	ns
CCKR↑ delay after CDCCR↑	$t_{D(1)}$		1900		ns
CDCCR↓ delay after CCKR↓	$t_{D(2)}$		3800		ns
CFMR pulse width (high)	t_{PW}		1900		ns

Figure 18. C-Bit Transmit Interface Timing



Note 1: A C-bit must be transmitted as a one when not needed.

Parameter	Symbol	Min	Typ	Max	Unit
CCKT clock period	t_{CYC}		3800		ns
CDT set-up time to CCKT↑	t_{SU}	25			ns
CDT hold time after CCKT↑	t_H	40			ns
CCKT output delay after CFMT↑	t_{OD}		3800		ns
CCKT↑ delay after CDCCT↑	$t_{D(1)}$		1900		ns
CDCCT↓ delay after CCKT↓	$t_{D(2)}$		3800		ns
CFMT pulse width	t_{PW}		1900		ns

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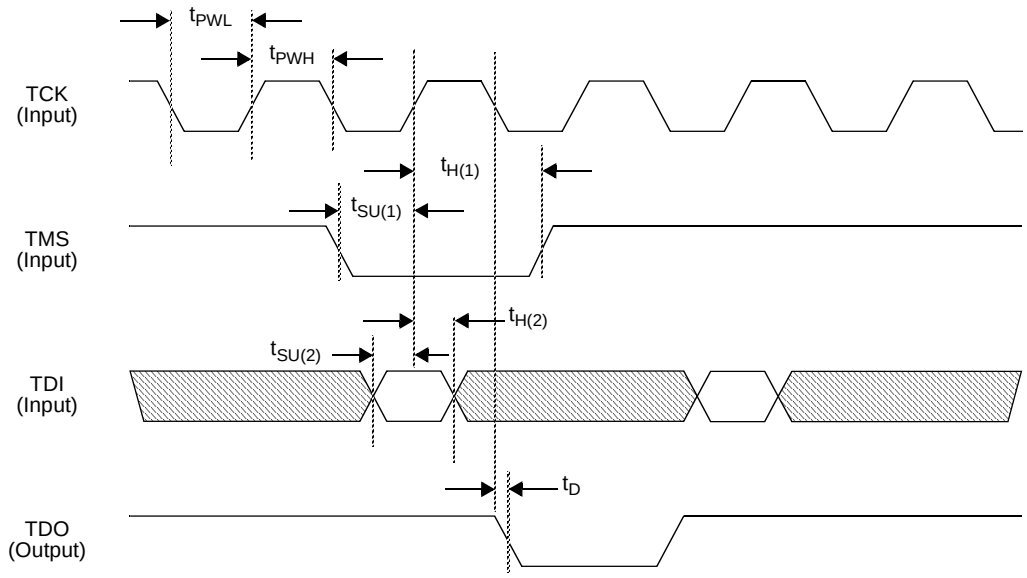
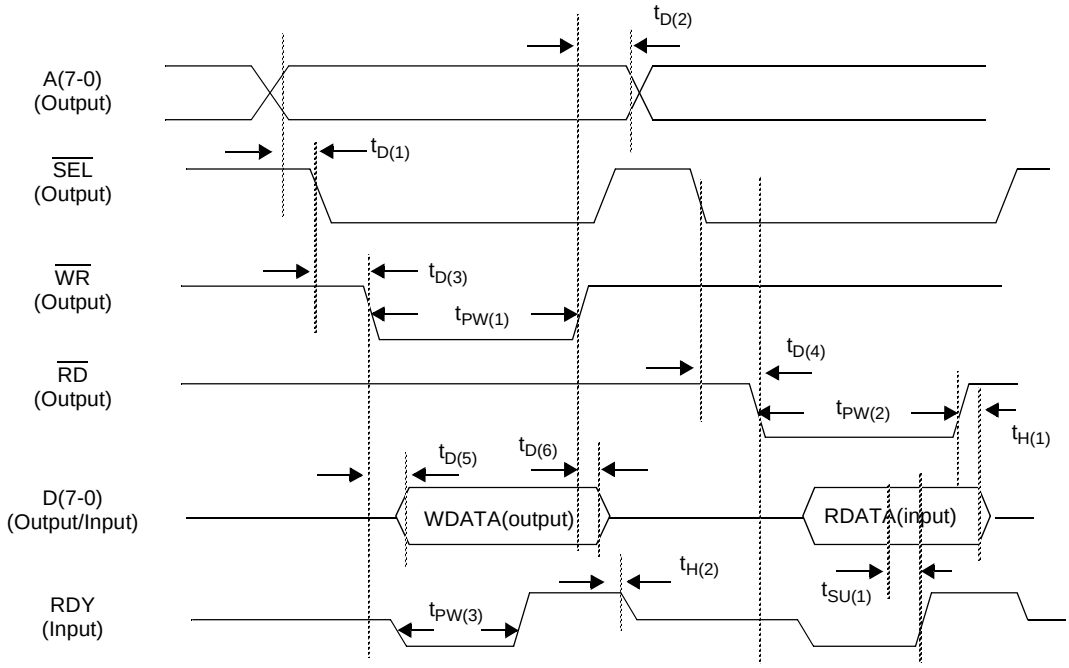
Figure 19. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	5.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	5.0	-	ns
TDO delay from TCK↓	t_D	5.0	10	ns

Figure 20. Intel Microprocessor Write/Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}$ delay after A(7-0)	$t_{D(1)}$	7	40		ns
A(7-0) delay after $\overline{WR}\uparrow$	$t_{D(2)}$	8			ns
$\overline{WR}$ delay after $\overline{SEL}\downarrow$	$t_{D(3)}$	7	40		ns
$\overline{RD}$ delay after $\overline{SEL}\downarrow$	$t_{D(4)}$	7	40		ns
D(7-0) delay after $\overline{WR}\downarrow$	$t_{D(5)}$	0			ns
D(7-0) valid delay after $\overline{WR}\uparrow$	$t_{D(6)}$	8			ns
D(7-0) hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0			ns
D(7-0) set-up time to RDY$\uparrow$	$t_{SU(1)}$	5			ns
RDY hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	80			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	80			ns
RDY pulse width	$t_{PW(3)}$	0		time-out	ns

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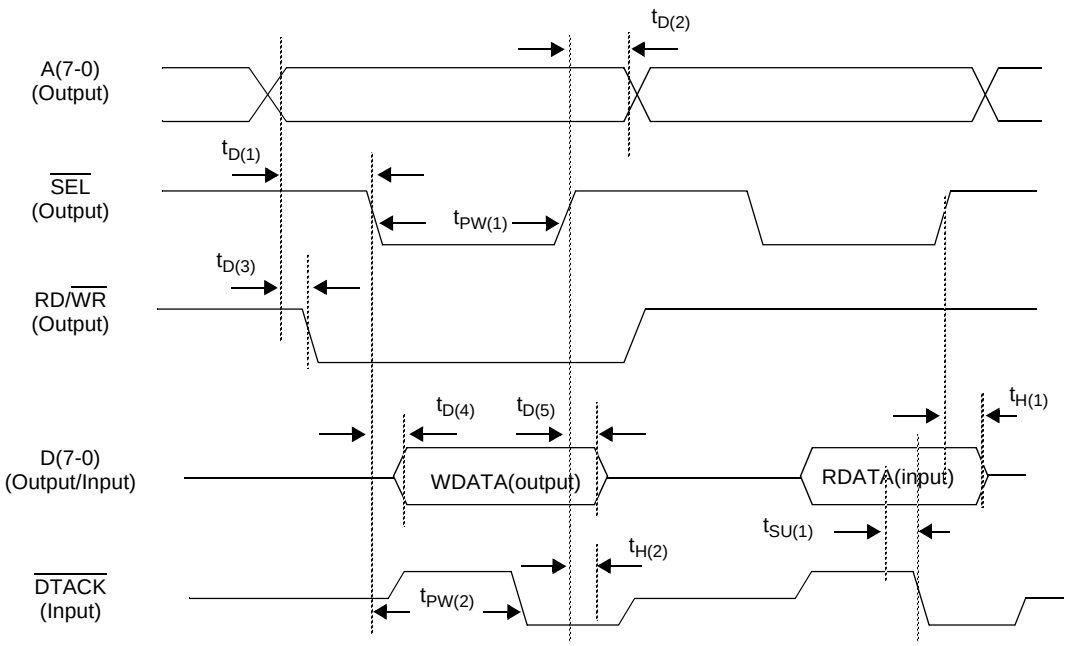
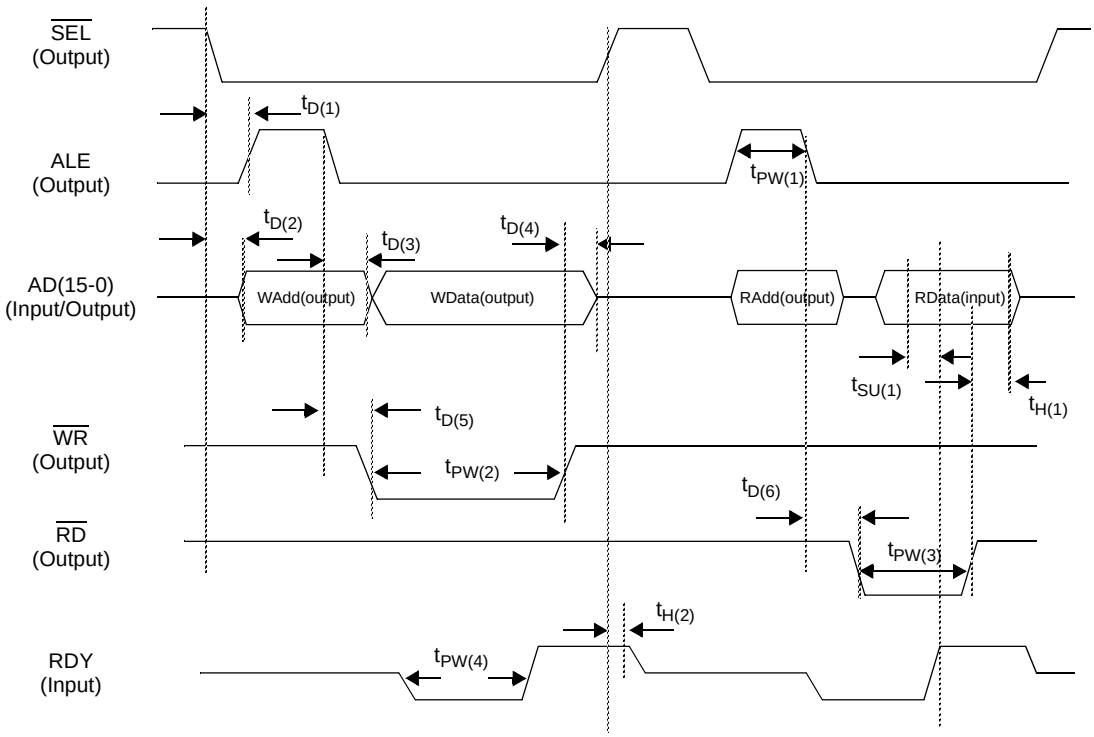
Figure 21. Motorola Microprocessor Write/Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}$ delay after A(7-0)	$t_{D(1)}$	7			ns
A(7-0) delay after $\overline{SEL}\uparrow$	$t_{D(2)}$	8			ns
RD/$\overline{WR}$ delay after A(7-0)	$t_{D(3)}$	40			ns
D(7-0) delay after $\overline{SEL}\downarrow$	$t_{D(4)}$	0			ns
D(7-0) valid delay after $\overline{SEL}\uparrow$	$t_{D(5)}$	8			ns
D(7-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0			ns
D(7-0) set-up time to $\overline{DTACK}\downarrow$	$t_{SU(1)}$	5			ns
$\overline{DTACK}$ hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	80			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0			ns

Figure 22. A/D Mux Write/Read Timing



Note: MOTO pin must be set low.

Parameter	Symbol	Min	Typ	Max	Unit
ALE delay after $\overline{SEL}\downarrow$	$t_{D(1)}$	0			ns
AD(15-0) delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	0			ns
AD(15-0) address valid delay after ALE$\downarrow$	$t_{D(3)}$	8			ns
AD(15-0) data valid delay after $\overline{WR}\uparrow$	$t_{D(4)}$	8			ns
$\overline{WR}$ delay after ALE$\downarrow$	$t_{D(5)}$	40			ns
$\overline{RD}$ delay after ALE$\downarrow$	$t_{D(6)}$	40			ns
AD(15-0) data hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0			ns
AD(15-0) set-up time to RDY$\uparrow$	$t_{SU(1)}$	5			ns
RDY hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	0			ns
ALE pulse width	$t_{PW(1)}$	40			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	40			ns
$\overline{RD}$ pulse width	$t_{PW(3)}$	40			ns
RDY pulse width	$t_{PW(4)}$	0			ns

OPERATIONS

The following sections detail the internal operation of the T3BwP.

LINE INTERFACE PORT

The T3BwP can enable either DS3 line interface or 28 T1 direct line access via a strap leads LM2-0. Note that both line interfaces can not be active at the same time.

DS-3 Line port:

If the Leads LM2-0=(H,L,L or H,L,H), the DS-3 line port is enabled. In the receive direction, DS3 data (RDS3D) is clocked into the M13X on positive transitions of the DS3 input clock (RDS3C). The data and clock signals may be derived from any line interface device such as TranSwitch's DART device or from other line circuitry.

In the transmit direction, DS3 data (TDS3D) is clocked out from M13X on positive transitions of the DS3 output clock (TDS3C). TDS3C, A 44.736 MHz clock, is derived from the external transmit clock input signal XCK or from the DS3 Receive Clock DS3CR when loop timing mode is enabled (via control bit LPTIME) or when the XCK clock fails. The XCK clock shall have a frequency of 44.736 MHz and a stability of +/- 20 ppm. The clock duty cycle shall be kept to (50 +/- 5)%.

28 T1 Line Access Ports:

For direct T1 line access, 28 T1 line access ports are enabled if leads LM2-0=(L,L,L). If T1 line access ports are selected, the internal M13X block are bypassed. To reduce the lead count, only NRZ mode is supported at T1 line port.

In the receive direction, the T1 data (RDS1Dn) is clocked into T1 framer on transition of input clock (RDS1Cn). In the transmit direction, the T1 data (TDS1Dn) is clocked out on transition of output clock (TDS1Cn). Control bits TXCP and RXCP enable the NRZ data to be clocked in and out of the T1 framer on either edge of the clocks. Control bits RXNRZP and TXNRZP enable the NRZ data polarity. See Memory Map for detail.

Leads LM2-0:

The line port operation is selected via setting control leads LM2-0 according to the Table 1.

Table 1. Operation Mode Set-up for Line Port

LM2 (DS3/E3)	LM1 (E1)	LM0 (VT)	Line Operation
L	L	L	DS1 line I/F
H	L	H	DS3 line I/F (clear DS3 channel); See Section "DS3 Clear Channel"
H	L	L	DS3 line I/F (DS3 to DS1)
Reserved			Test Use

Line port leads Assignment:

Table 2. Lead Assignment of Line Port

		Mode	
I/O Lead Name	I/O	DS1 line	DS3 line
RDS1D1/RDS3D	I	RDS1D1	RDS3D
RDS1C1/RDS3C	I	RDS1C1	RDS3C
TDS3D	O		TDS3D
TDS3C	I/O		TDS3C (O) Test Use (I)
RDS1D2-21 RDS1D22-28	I I/O	RDS1D2-21 RDS1D22-28 (I) Test Use (O)	Note 1
RDS1C2-21 RDS1C22-28	I I/O	RDS1C2-21 RDS1C22-28 (I) Test Use (O)	
TDS1D1-28/	O	TDS1D1-28	Note 2
TDS1C1-28	I/O	TDS1C1-28(O) Test Use (I)	

Notes:

1. The leads RDS1D2-6 are used as inputs from DART device: RDS1D2/LCV, RDS1D3/$\overline{\text{EXZ}}$, RDS1D4/$\overline{\text{DLOS}}$, RDS1D5/$\overline{\text{ALOS}}$, RDS1D6/$\overline{\text{DS3BIST}}$.
2. The leads TDS1D1-12 are used as output to DART device: TDS1D1/$\overline{\text{RAIS}}$, TDS1D2/$\overline{\text{RXDIS}}$, TDS1D3/$\overline{\text{TRLBK}}$, TDS1D4/LNLBK, TDS1D5/$\overline{\text{ZERO}}$, TDS1D6/DSXDIS, TDS1D7/TEST0, TDS1D8/TEST1, TDS1D9/PAT23, TDS1D10/DJSEL0, TDS1D11/DJSEL1, TDS1D12/DIVSEL.

SYSTEM PORTS

The T3BwP provides four different system port interfaces: Unframed, Transmission, MVIP, and H.100/H.110. The system ports operation could be any combination of Unframed, transmission, and either MVIP or H.100/H.110. This means the system ports could operate at combination of Unframed, Transmission, and either MVIP or H.100/H.110 but not both.

Unframed Mode

The API enables the unframed mode in nth T1 framer. For an unframed DS1 line, there are only data and clock signals for each transmit and receive direction at unframed mode. In this case, all of the signals, in and out, are independent in all respects. All receive clocks are independent and all transmit clocks are independent. The output received line clock (RCLKn) is used to clock out data (RDATAn) in the receive direction. The input transmit clock (TCLKn) is used to clock in the transmit data (TDATAn) in the transmit direction. Any of twenty-eight lines could be enabled as unframed mode. For the unframed T1 signals, the signals are transmitted through T1 cross-connect facility between T1 framer and system port. The configuration of T1/DS-0 cross-connect facilities assigns the I/O leads to unframed T1 line.

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Transmission Mode

The API enables the transmission mode in nth T1 framer. For a transmission mode DS1 line, there are clock, data, and framing pulse signals in each direction. It is possible that each transmission line is with independent receive timings and independent transmit timings. Each line can have different framing mode (i.e., unframed, D4SF, or ESF) via API. The receive and transmit slip buffers can be individually bypassed. The T1 signals are transmitted through T1 cross-connect facility between T1 framer and system port. The configuration of T1/DS-0 cross-connect facilities assigns the I/O leads to transmission T1 line.

The recovered receive line clock (RCLKn) and an internal sync pulse are sued to clock out data (RDATAn), and the sync pulse (RFRMn) to the system. The position of RFRMn with respect to the RDATAn signal can be off-set.

The input transmit clock (TCLKn) is used to clock in the transmit data (TDATAn) and input transmit framing pulse (TFRMn). The position of TFRMn with respect to the TDATAn signal can be offset.

Figure 23 below shows the general structure.

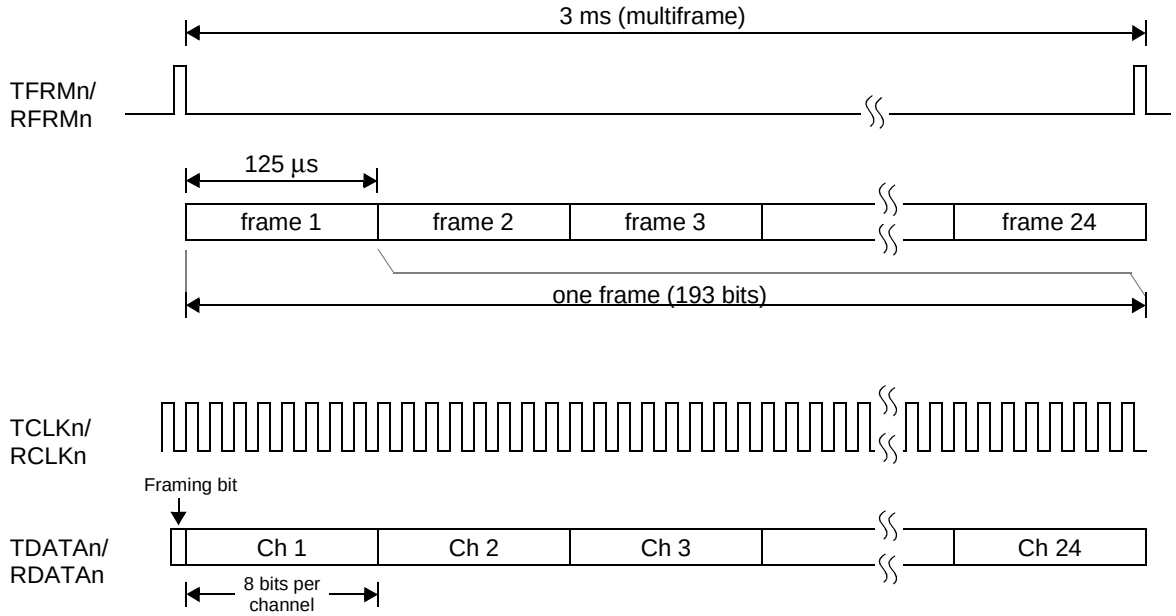

Figure 23. System Interface Framing Format for Transmission Mode

MVIP Mode

For a MVIP DS1 port, there are data and signaling signals for each transmit and receive direction. All MVIP ports share the clock and framing pulse signals.

To enable a MVIP port at system side, the input lead H100_sel is set to low. The API shall also enable MVIP mode in selected T1 framers and enable receive and transmit slip buffers for nth line before communicating via DS-0 cross-connect facility. By setting lead H100_sel to low, this enables the system port operating at MVIP mode at selected lines. The configuration of T1/DS-0 cross-connect facilities assigns the I/O leads to MVIP T1 line. However, by selecting the MVIP operation mode, it enables the system ports 1-4 operate as MVIP in default. The others system ports can also be assigned as MVIP ports if more then 4 MVIP ports are applied. See Table 3 for detail.

In the receive direction, the common input clock (TCLK_2) and common framing pulse (TSYNC_2) are used to clock out the received data (RDATAn) and signal (RSIGn). In the transmit direction, the common input clock (TCLK_2) and common framing pulse (TSYNC_2) are used to clock in the transmitted data (TDATAn) and signal (TSIGn).

Figure 24 below shows the general structure.

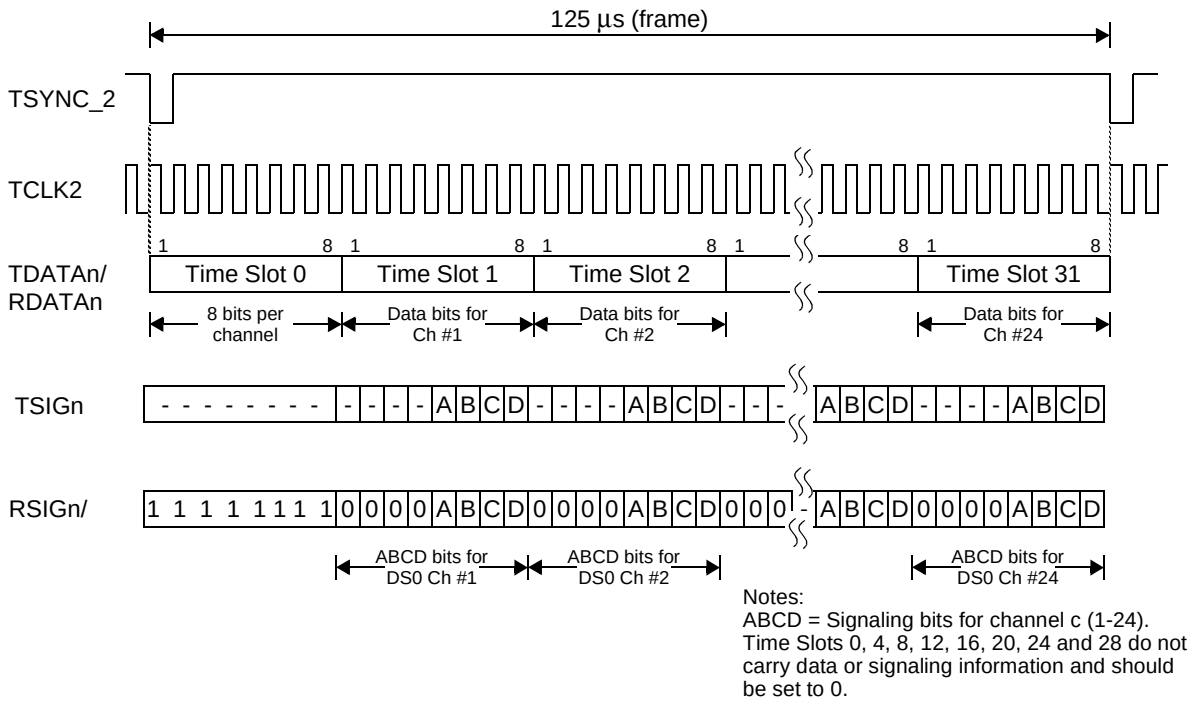

Figure 24. System Interface Format for MVIP Mode

H.100/H.110 Mode

The H.100/H.110 bus shares the clock and framing pulse signals. To select the H.100/H.110 mode at system port, the input lead H100_sel is set to high. The API shall also enable H.100/H.110 mode in selected T1 framers and enable receive and transmit slip buffers for nth line before communicating via DS-0 cross-connect facility. By selecting the H.100/H.110 operation mode, it enables the system ports 1-8 operate as H.100/H.110 bus. See Table 3 for detail.

Figure 25 below shows the general structure.

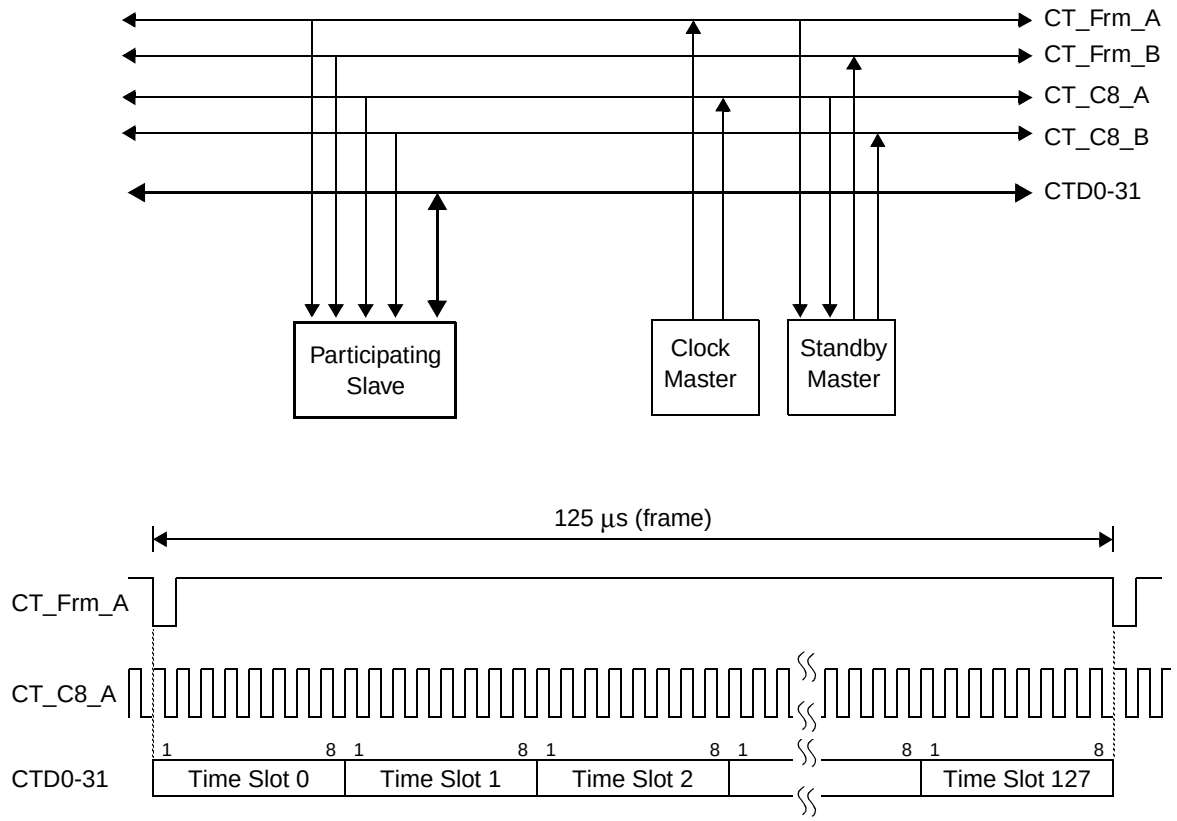

Figure 25. Data & Signaling Highways - 8 Mbit/s H.100/H.110 Mode

H.100/H.110 System Bus Clock Selection, Monitoring, and Automatic Switching

The users can select the system bus clock from either source A (CT_C8_A, CT_FRM_A) or source B (CT_C8_B, CT_FRM_B) via API. The bus clock selection can be one of the following modes:

- Select source A initially, and allow T3BwP switch to the other clock source automatically.
- Select and force source A, will NOT allow T3BwP switch to the other clock source automatically.
- Select source B initially, and allow T3BwP switch to the other clock source automatically.
- Select and force source B, will NOT allow T3BwP switch to the other clock source automatically.

For proper MVIP operation, the system bus clock selection shall be set “Select and force source A”.

To insure the reliability of H.100/H.110 bus, the T3BwP will detect and report either of the following two conditions on bus clock source:

1. Edge error: A received rising edge of CT_C8_A/B does not arrive within +/- 35 nsec of the expected time of that edge.
2. Frame error: The CT_FRM_A/B does not occur 125 µsec apart. There are not exactly 1024 clock period per frame.

Upon detecting edge or frame error, a internal status bit will be set for LMPro processing. The T3BwP will switch clock source automatically to the designated secondary clock source when either frame error or edge error occurs if allowed. If the clock source are selected and forced, it is up to host whether to switch the clock source. LMPro will report the error condition and current bus source to host via API.

Lead Assignment of System Ports

The configuration of T1 cross-connect and DS-0 cross-connect facilities assigns the I/O leads to Unframed, Transmission, MVIP, and H.100/H.110 T1 line. Table 3 shows the lead assignment under different modes. The system port can operate at any combination of Unframed, Transmission, and either MVIP or H.100/H.110. When the H.100/H.110 is selected, the leads for ports 1-8 are assigned to H.100/H.110. If any MVIP is selected, the leads for port 1-4 are assigned as MVIP ports due to the both framing pulses and clocks signals of MVIP are designated in leads of ports 1-4.

When system ports consist of H.100/H.110, Transmission, and Unframed modes: the ports 1-8 are assigned as H.100/H.110 ports. Any port from ports 9-28 can be assigned as either transmission mode or unframed mode.

When system ports consist of MVIP, Transmission, and Unframed modes: the ports 1-4 are assigned as MVIP ports. Any port from ports 9-28 can be assigned as either MVIP mode, transmission mode or unframed mode.

Table 3. Lead Assignment of System Port

		Mode				
I/O Lead Name	I/O/P	Unframed	Transmission	MVIP	H.100/H.110	DS3 or NxDS0 Bus (LCI)
RCLK1/RSYNC_2/ CT_Frm_8	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock	RSYNC_2[1]:	CT_Frm_8:	
RCLK2/RSYNC_64	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock	RSYNC_64[1]:	RSYNC_64:	
RCLK3/RCLK_2/ CT_CLK_8	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock	RCLK_2[1]:	CT_CLK_8:	
RCLK4/RCLK_64	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock	RCLK_64[1]:	RCLK_64:	
RCLK5-8	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock			
RCLK9-16	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock		Available for UnF, Trans[2]	
RCLK17/RxCellPkt	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock		Available for UnF, Trans[2]	RxCellPkt: Rx Cell/packet indication
RCLK18/RxClk	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock		Available for UnF, Trans[2]	RxClk: Rx 6.25 MHz
RCLK19-28/ RLCnum0-9	O	RCLK[1]: Receive Clock	RCLK[1]: Receive Clock		Available for UnF, Trans[2]	RLCnum0-9: Rx link channel number
RDATA1-8/CTD0-7	I/O	RDATA[1]: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	CTD:Serial data line (I/O)	
RDATA9-17	O	RDATA: Receive data highway output (O)	RDATA: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	Available for UnF, Trans[2]	

		Mode				
I/O Lead Name	I/O/P	Unframed	Transmission	MVIP	H.100/H.110	DS3 or NxDS0 Bus (LCI)
RDATA18/RCLKX8	O	RDATA: Receive data highway output (O)	RDATA: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	Available for UnF, Trans[2]	RCLKX8: 50 MHz
RDATA19/$\overline{\text{RxValid}}$	O	RDATA: Receive data highway output (O)	RDATA: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	Available for UnF, Trans[2]	$\overline{\text{RxValid}}$: Rx valid signal
RDATA20/$\overline{\text{TxValid}}$	O	RDATA: Receive data highway output (O)	RDATA: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	Available for UnF, Trans[2]	$\overline{\text{TxValid}}$: Tx valid signal
RDATA21-28/ RxData1-8	O	RDATA: Receive data highway output (O)	RDATA: Receive data highway output (O)	RDATA[1]: Receive data highway output (O)	Available for UnF, Trans[2]	RxData1-8: Rx data
RFRM1-8/ RSIG1-8/CTD8-15	I/O		RFRM[1]: Receive frame pulse (O).	RSIG[1]: Receive signaling highway output (O)	CTD: Serial data line (I/O)	
RFRM9-16/RSIG9-16	O		RFRM: Receive frame pulse (O)	RSIG[1]: Receive signaling highway output (O)	Available for Trans[2]	
RFRM17/RSIG17/ TxCellPkt	O		RFRM: Receive frame pulse (O)	RSIG[1]: Receive signaling highway output (O)	Available for Trans[2]	TxCellPkt: Tx cell/packet indication
RFRM18/RSIG18/ TxClk	O		RFRM: Receive frame pulse (O)	RSIG[1]: Receive signaling highway output (O)	Available for Trans[2]	TxClk: Tx 6.25 MHz
RFRM19-28/ RSIG19-28/ TLCnum0-9	O		RFRM: Receive frame pulse (O)	RSIG[1]: Receive signaling highway output (O)	Available for Trans[2]	TLCnum0-9: Tx link channel number
TCLK1/TSYNC_2_A/ CT_Frm_A	I	TCLK[1]: Transmit clock	TCLK[1]: Transmit clock	TSYNC_2_A[1]:	CT_FRM_A	
TCLK2/TCLK_2_A/ CT_C8_A		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock	TCLK_2_A[1]	CT_C8_A	
TCLK3/TSYNC_64_A		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock	TSYNC_64_A[1]:	TSYNC_64_A	
TCLK4/TCLK_64_A		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock	TCLK_64_A[1]	TCLK_64_A	
TCLK5/CT_FRM_B		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock		CT_FRM_B	
TCLK6/CT_C8_B		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock		CT_C8_B	
TCLK7		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock			
TCLK8		TCLK[1]: Transmit clock	TCLK[1]: Transmit clock			
TCLK9-28 (I)	I	TCLK: Transmit clock	TCLK: Transmit clock		Available for UnF, Trans[2]	

I/O Lead Name	I/O/P	Mode				
		Unframed	Transmission	MVIP	H.100/H.110	DS3 or NxDS0 Bus (LCI)
TDATA1-8/CTD16-23	I/O	TDATA[1]: Transmit data highway input	TDATA[1]: Transmit data highway input	TDATA[1]: Transmit data highway input	CTD: Serial data line (I/O)	
TDATA9-20 (I)	I	TDATA: Transmit data highway input	TDATA: Transmit data highway input	TDATA[1]: transmit data highway input	Available for UnF, Trans[2]	
TDATA21-28/ TxData1-8 (I)	I	TDATA: Transmit data highway input	TDATA: Transmit data highway input	TDATA[1]: transmit data highway input	Available for UnF, Trans[2]	TxData1-8: Tx data
TFRM1-8/TSIG1-8/ CTD24-31	I/O	-	TFRM[1]: Transmit frame pulse	TSIG[1]: Transmit signaling high-way input*	CTD: Serial data line (I/O)	
TFRM9-28/ TSIG9-28 (I)	I	-	TFRM: Transmit frame pulse	TSIG[1]: Transmit signaling high-way input	Available for Trans[2]	

Notes:

1. Lead is not available if H.100/H.110 is enabled.
2. Lead is available for Unframed or Transmission Mode.
3. Port 1-4 are for MVIP mode only if MVIP is enabled

Figure 26 shows a possible system port operation combining different modes.

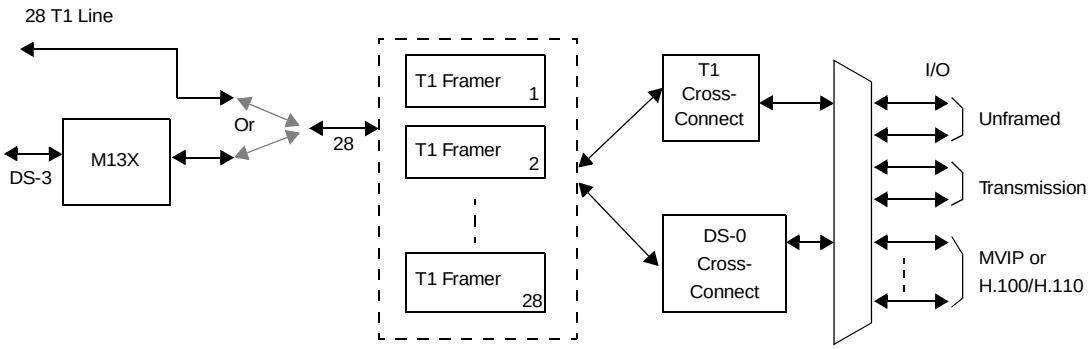

Figure 26. Example of System Port Assignment

DS-1 CROSS-CONNECT

The API configures the DS1 cross-connect facility. The T1 signals are transmitted via the T1 cross-connect facility if the T1 framer is operated at either “unframed” or “transmission” mode. The T1 data bypass slip buffer in T1 framer if unframed mode is selected. The receive and transmit slip buffers in the framer can be individually bypassed if transmission mode is selected. The T1 signals are then switched by T1 cross-connect facility.

In the receive direction, the T1 framer signals are switched or bypassed under the control registers configured by API. The T1 cross-connect facility also provides a loopback function. Any 2 of received T1 signals can be

loopback and any 2 of received T1 signals can be selected and analyzed for DS1 PRBS pattern (i.e., (2^{15} - 1) pattern or QRSS (2^{20} - 1)). In the transmit direction, the signals from system port are input into cross-connect facility. The system port signals are switched into framer or bypassed under the control registers configured by API. Any 2 of transmit T1 signals can be selected and generated for DS1 PRBS pattern (i.e., (2^{15} - 1) pattern or QRSS (2^{20} - 1)).

DS-0 TIME SLOT INTER-CHANGE

The API configures the DS0 cross-connect facility. The signals are transmitted via the DS-0 cross-connect facility if the T1 system port is operated at either MVIP or H.100/H.110 mode. In this case, the receive and transmit slip buffer in T1 framer will always be enabled for those T1 signals. In the receive direction, the T1 time slot data and signalling are read into receive buffer memory (RBM) and read out under receive control memory (RCM). In the transmit direction, the I/O signals are read into transmit buffer memory (TBM) and read out under transmit control memory (TCM).

Full connectivity DS-0 TSI are described as follows:

- Provide full DS-0 Time Slot Interchange (TSI) function:
- Time slot written in Frame N, read out in Frame N+1
- Data can be switched from any time slot to any time slot
- ABCD signalling can be switched from any time slot to any time slot
- All 672 DS0 channels including ABCD signalling can be switched to any of the 4096
- In received direction, time slot are sequentially written into Receive Buffer Memory (RBM), read out under Receive Control Memory (RCM)
- In the transmit direction, time slot are sequentially written into Transmit Buffer Memory (TBM), read out under Transmit Control Memory (TCM)

T3BwP LINK CHANNEL INTERFACE

The external logic can also transfer the data via the TranSwitch link channel interface for clear channel service.

DS-3 UnChannelized Service

The external device can transfer traffic (either cell or packet) into DS3 payload in C-bit parity unchannelized mode. The DS-3 clear channel mode can be enabled by setting leads LM2-0=HLH. These signals described as follows are brought out to provide the DS3 clear channel function in T3BwP.

Rx Direction:

RxData1-8 (RX Data; output): When DS3 clear channel is enabled (i.e., LM2-0=HLH), the received DS-3 payload is clocked out from T3BwP on the rising edge of DPLLClk.

$\overline{\text{RxValid}}$ (RX Valid Signal; output): Active low when DS3 clear channel is enabled; It indicates the valid data byte when it is asserted.

RxCellPkt (Receive cell/packet indication; output): When is low, it indicates the data byte is a packet payload. When is low, it indicates the data is a cell payload.

RxClk (Receive Clock; output): A 6.25 MHz clock that is used to indicate the byte boundary of RxData1-8.

Tx Direction:

TxData1-8 (TX Clear Channel Input Data; input): When DS3 clear channel is enabled (i.e., LM2-0=HLH), transmitted clear channel 44.736 Mbit/s data are clocked into T3BwP on rising edge of DPLLClk.

$\overline{\text{TxValid}}$ (TX Valid Signal; output): Active low when DS3 clear channel is enabled; It indicates that the valid data byte when it is asserted.

TxCellPkt (Transmit cell/packet indication; output): When is low, it indicates the data byte is a packet payload. When is low, it indicates the data is a cell payload.

TxClk (Transmit Clock; output): A 6.25 MHz clock which is used to indicate the byte boundary of TxData1-8.

NxDS0 Service

The external device can transfer traffic (either cell or packet) into NxDS0 link channel. The NxDS0 clear channel mode can be enabled via API. These signals described as follows are brought out to provide the NXDS0 clear channel function in T3BwP.

The leads assigned to NxDS0 clear channel port are system ports 17 to 28. Therefore, it is possible that the T3BwP can run at Transmission, H.100/H.110 or MVIP, and NxDS0 clear channel simultaneously.

Rx Direction:

RxData1-8 (RX Data; output): When DS3 clear channel is enabled (i.e., LM2-0=HLH), the received DS-3 payload is clocked out from T3BwP on the rising edge of DPLLClk.

$\overline{\text{RxValid}}$ (RX Valid Signal; output): Active low when DS3 clear channel is enabled; It indicates the valid data byte when it is asserted.

RxCellPkt (Receive cell/packet indication; output): When is low, it indicates the data byte is a packet payload. When is low, it indicates the data is a cell payload.

RxClk (Receive Clock; output): A 6.25 MHz clock that is used to indicate the byte boundary of RxData1-8.

RLCnum0-9 (Rx Link Channel Number; output): These leads indicates the link channel number for data transferring in the receive direction.

Tx Direction:

TxData1-8 (TX Clear Channel Input Data; input): When DS3 clear channel is enabled (i.e., LM2-0=HLH), transmitted clear channel 44.736 Mbit/s data are clocked into T3BwP on rising edge of DPLLClk.

$\overline{\text{TxValid}}$ (TX Valid Signal; output): Active low when DS3 clear channel is enabled; It indicates that the valid data byte when it is asserted.

TxCellPkt (Transmit cell/packet indication; output): When is low, it indicates the data byte is a packet payload. When is low, it indicates the data is a cell payload.

TxClk (Transmit Clock; output): A 6.25 MHz clock which is used to indicate the byte boundary of TxData1-8.

TLCnum0-9 (Tx Link Channel Number; output): These leads indicates the link channel number for data transferring in the transmit direction.

The T3BwP also provide a synchronous high speed serial clock (RCLKX8) for multi-cycle data processing. The RCLKX8 is 50 MHz output.

DS-3 C-BIT INTERFACE SERVICE

Transmit and receive DS3 C-Bit interfaces are provided for inserting and extracting a set of the DS3 C-Bits while operating in C-Bit Parity Format mode.

The TX C-Bit interface is comprised of four leads, CCKT (clock output), CDT (data input), CDCCT (data link indication output), and CFMT (frame output). The following DS3 C-Bits are accepted at this interface, C2, C13, C14, C15, C16, C17, C18, C19, C20, and C21.

The RX C-Bit interface is comprised of four leads, CCKR (clock output), CDR (data output), CDCCR (data link indication output), and CFMR (frame output). The following DS3 C-Bits are output at this interface, C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. Unlike the TX C-Bit interface, all of the indicated C-Bits are always available.

DART CONTROL PORT

This port is to control the DS3 line interface - TranSwitch DART device. The T3BwP maintains counters for DS3 line coding violation (LCV_cntr) and DS3 line excessive zeros (EXZ_cntr). The T3BwP increments the LCV_cntr or EXZ_cntr with respect to the asserted input signals LCV or $\overline{EXZ}$. The T3BwP also provides shadow registers for both coding violation and excessive zeros. The LLCV_cntr and LEXZ_cntr registers hold the coding violation and excess zeros count that occurred in the previous one second interval. The shadow register is updated once when one second signal is applied. The counter LCV_cntr and EXZ_cntr are reset after updating the shadow registers.

The DART asserts the $\overline{DLOS}$ or $\overline{ALOS}$ signal to indicate the detection of digital LOS or analog LOS. Upon receiving the LOS indication from DART, the status bit DLOS or ALOS will be set and interrupt will be generated if not masked. The T3BwP shall take appropriate actions when LOS is indicated. The DART sets the $\overline{DS3BIST}$ to low when an invalid unframed PRBS pattern is detected. Upon receiving the $\overline{DS3BIST}$ indication, the status bit $\overline{DS3BIST}$ will be set and interrupt will be generated if not masked. The current status bit is set when the event is occurring. The latched status bit is cleared on read.

The configuration of DART is also performed by T3BwP. The host issues a configuration request message to T3BwP via API. After decoding the request from host, T3BwP sets the output control leads according to host request via control registers. For request message format, see “Programming Reference Manual”. The output control leads are described as follows:

Control Lead	Functions
$\overline{RAIS}$	**DART Receive AIS Enable:** When $\overline{RAIS}$ is low, it enables generation of framed DS3 AIS on the receiver outputs of DART.
$\overline{RXDIS}$	**DART Receive Output Disable:** When $\overline{RXDIS}$ is low, it forces the receiver RP/RD and RN outputs of DART to a low state.
$\overline{TRLBK}$	**DART Terminal Loopback Enable:** When $\overline{TRLBK}$ is low, it enables a digital loopback from the transmitter inputs to the receiver terminal side in DART.
$\overline{LNLBK}$	**DART Line Loopback Enable:** When is low, it enables an internal line loopback from the DI1/DI2 to the DOUT or DO1/DO2 outputs in DART.
$\overline{ZERO}$	**DART Transmit Zero cable Enable:** When $\overline{ZERO}$ is low, it improves DOUT output mask for short cable length in DART.

Control Lead	Functions
$\overline{\text{DSXDIS}}$	**DART Transmit DSX Output Disable:** When $\overline{\text{DSXDIS}}$ is low, it disables DOUT output and enable DO1/DO2 outputs in DART.
$\overline{\text{TEST0}}$	**DART Test-in 0:** When $\overline{\text{TEST0}}$ is low, it enables an internal PRBS generator in DART.
$\overline{\text{TEST1}}$	**DART Test-in 1:** When $\overline{\text{TEST1}}$ is low, it enables an internal analog terminal side loopback from the TP/TD and TN signals to the receiver outputs in DART.
$\overline{\text{PAT23}}$	**DART PRBS 2^{23} Select:** When is low, it selects a 2^{23}-1 pattern for the PRBS analyzer and generator for DART. When this lead is high, it selects a 2^{15}-1 pattern.
DJSEL0	**Dejitter Block Control 0:** 1 of 2 control leads which control the dejitter buffer/dejitter PLL modes of DART.
DJSEL1	**Dejitter Block Control 1:** 1 of 2 control leads which control the dejitter buffer/dejitter PLL modes of DART.
DIVSEL	**Divide Select:** Selects the divisor in the divide-by block in the dejitter PLL of DART.

PRBS GENERATOR AND ANALYZER

The T3BwP provides the ability to separately generate a pseudo-random bit pattern or to detect a pseudo-random bit pattern on a per DS3 basis, or DS1 basis, or on a NxDS0 basis. Four Common generator/analyzer pairs are used.

The PRBS generator can generate four PRBS patterns:

- PRBS (2^{23} - 1) pattern defined in ITU-T O.151
- QRSS (2^{20} - 1) pattern defined in T1M1.3-005R1 (April 1993), and ANSI T1.403-1998
- PRBS (2^{15} - 1) pattern defined in ITU-T O.151 and T1M1.3-005R1
- PRBS (2^{11} - 1) pattern defined in ITU-T O.152
- 32-bit code word

DS1 Test Generation and Analysis:

Two Common generator/analyzer pairs are used for DS1. The DS1 test selects either (2^{15} - 1) pattern or QRSS (2^{20} - 1) pattern. The test could be for both unframed or framed DS1.

The enabling of DS1 PRBS generator and selecting of PRBS pattern is through API.

The enabling of DS1 PRBS analyzer and selecting of PRBS pattern is through API.

If the PRBS pattern is tested through a unframed DS1, the DS1 line should be enabled as “Unframed” mode. If the PRBS patter is tested through a framed DS1, the DS1 line should be enabled as “Transmission” mode.

DS0 Test Generation and Analysis:

The DS0 test selects either (2^{15} - 1) pattern, QRSS (2^{20} - 1) pattern, (2^{11} - 1) pattern, or 32-bit code word through API. The zero suppression can be enabled or disabled for 2^{11} - 1 pattern. The test should be for both Nx56K and Nx64K. The Nx64 is all 8 bits per DS0 are used. The Nx56 is 7 bits per DS0 are used. Bit 8 is set to one.

PRODUCT PREVIEW

DS3 Test Generation and Analysis:

The DS3 test selects either (2^{23} - 1) pattern, QRSS (2^{20} - 1) pattern, or (2^{15} - 1) pattern through API.

Status of PRBS Analysis:

There are four sets of PRBS generator and analyzer: two sets for DS1 test generation and analysis and two sets for DS3 and NxDS0 test generation and analysis. The results of PRBS analyzer are reflected into the out-of-lock registers. The T3BwP provides out-of-lock counters and indicator for lock, out-of-lock.

DS0 REMOTE LOOPBACK

The DS0 Fractional Channel Loopback requirement is specified in ANSI document T1.403-1998, Annex B. By definition, remote loopback is the transmission of remote loopback sequence by the local framer to the distant framer. The DS0 Fractional Channel Loopback can involve one or more DS0s, which may or may not be contiguous, and the DS0s may all be either 56 kbit/s or 64 kbit/s. Figure 27 is a simplified diagram of the code sequence generator. The sequence starting point and the ending point in the sequence are arbitrary.

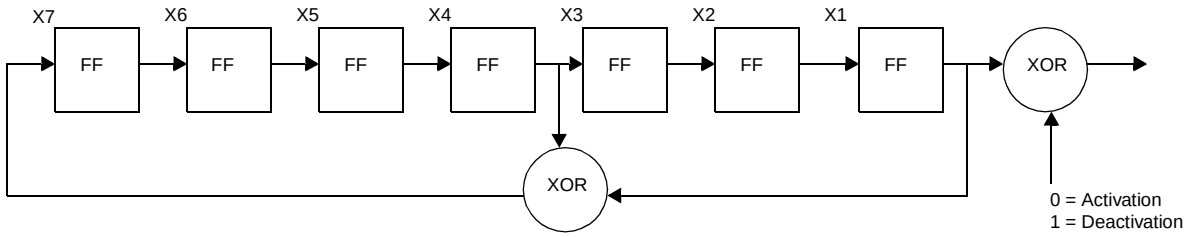

Figure 27. DS0 Remote Loopback Code Sequence Generator

To activate the DS0 remote loopback feature at the distant end, the loopback activation code for one or more DS0 channels is transmitted for a period of not less than 2 seconds. This will be followed by the transmission of an all ones pattern for not less than 2 seconds. The responding end (i.e., the distant end) should activate a loopback within the 2-second interval immediately following the end of the loopback activation code sequence.

To deactivate DS0 at the distant end, the loopback deactivation code is transmitted for a period of not less than 2 seconds, followed by transmission of an all ones pattern for not less than 2 seconds. The responding end should deactivate a loopback within the 2-second interval immediately following the end of the loopback deactivation code sequence.

All the DS0s in a fractional group may be 64 kbit/s clear channels or 56 kbit/s channels. For 56 kbit/s channels they may either have bit 8 forced to a one for all frames or they may have bit 8 forced to one for all frames except signaling frames in which signaling bits are inserted.

Transmit Direction:

The NxDS0 remote loopback activation/De-activation enabling and 56K/64K selection are through the API. The completion of the 4-second transmit DS0 sequence is also indicated back to host via API.

The Link Manager processor, upon reading the indication status bit, should inform Host that the transmission of the sequence is indeed complete. The Host can now write a new channel in which to send the activate code, or leave the channel the same for sending the deactivate code.

Receive Direction:

The receive side can monitor the NxDS0 channels that have been designated by the processor as a fractional channel. The 56K/64K selection is through the API. When 56K is selected, bit 8 (LSB) is ignored in the incoming DS0 channels for detection. That is because the fractional channel is conditioned for 56 kbit/s service. The T3BwP provides the capability of monitoring all fractional channel at round-robin fashion for the activate/deactivate sequence.

The standard (ANSI T1.403-1998) does not specify activation/deactivation detection parameters other than that there shall be a 2-second transition period which corresponds to the 2 seconds of all ones. For T3BwP, the activate/deactivate sequence is detected via multiple (5) windows. Each window is 50 bits. During each 50-bit window, the scanner starts next window if a “Unlock” is detected (i.e If error occurs before 50 bits, the process is restarted.) For consecutive 5 “unlock” window, the scanner moves to next fractional T1. The activate/deactivate sequence is detected if a “Lock” is detected within 5 windows zone. Once a sequence is detected, a 3 second timer is started. If 50 bits of ’1’ are received before the timer expired, a loop Up or down is detected. If 3 second timer expired during ’1’ detection phase, the scanner move to next channel.

The Link Manager processor will either setup or remove the NxDS0 loopback when activation or de-activation is detected. The host is also informed via API.

DS1 MONITOR PORT

For system applications that do not have direct T1 line access, the MONCLK1,2 and MONDATO1,2 leads can be configured to provide a T1 monitoring of any transmit or receive T1 line. These leads can be tristated to allow bussing of multiple T3BwPs.

The monitor port is enabled through API.

MICROPROCESSOR INTERFACE

The microprocessor interface is used to control external devices or mail box. This interface can be selected to communicate at Intel, Motorola, or Multiplexed mode. The Intel or Motorola mode is selected via lead MOTO. The multiplexed mode is enabled during SEEPROM loading.

CLOCK AND FRAMING PULSE INPUT/OUTPUT LEADS

This section describes the input/output clock and framing pulse usage for the T3BwP device.

CT_C8_A, CT_C8_B, CT_FRM_A, CT_FRM_B: Input

CT_C8_A, CT_FRAM_A: Main clock and framing pulse source for H.100/H.110 operation.

CT_C8_B, CT_FRAM_B: Redundant clock and framing pulse source for H.100/H.110 operation.

The H.100/H.110 bus clock source operation can be one of the following mode via API:

- Select source A initially, and allow T3BwP switch to the other clock source automatically.
- Select and force source A, will NOT allow T3BwP switch to the other clock source automatically.
- Select source B initially, and allow T3BwP switch to the other clock source automatically.
- Select and force source B, will NOT allow T3BwP switch to the other clock source automatically.

TCLK_2_A, TSYNC_2_A: Input

TCLK_2_A: It is a 2.048 MHz clock input for MVIP mode operation.

TSYNC_2_A: It is a framing pulse input with 125 µsec period for MVIP mode operation.

For proper MVIP operation, the bus clock source shall be set to “Select and force source A”.

TCLK_64_A, TSYNC_64_A: Input

For test use only.

CT_CLK_8, CT_Frm_8: Output

The T3BwP also provides 8.192 MHz clock and framing pulse when H.100/H.110 operation is selected. These outputs can be used as H.100/H.110 clock source if applicable. The 8.192 MHz can be derived from one of 28 received DS1 line clock, internal 50 MHz, or the input lead CLKRefin. The clock to CLKRefin can be 8 KHz, 64 KHz, 1.544 MHz, or 2.048 MHz via API.

RCLK_2, RSYNC_2: Output

The T3BwP also provides 2.048 MHz clock and framing pulse when MVIP operation is selected. These outputs can be used as MVIP clock source if applicable. The 2.048 MHz can be derived from one of 28 received DS1 line clock, internal 50 MHz, or the input lead CLKRefin. The clock to CLKRefin can be 8 KHz, 64 KHz, 1.544 MHz, or 2.048 MHz.

RCLK_64, RSYNC_64: Output

For test use only.

CLKRefin: Input

The T3BwP could use the input from CLKRefin as source to derive the output clock (e.g CLK_8Kout) and internal reference clock. The input to CLKRefin could be 8 KHz bits, 64 KHz bits, local Stratum 1.544 MHz, or 2.048 MHz. This is configured via API. This lead is tied to low if not used.

CLK_8Kout: Output

The output reference clock CLK_8Kout can be 8 KHz, 1.544 MHz, or 2.048 MHz or direct output from selected source. The CLK_8Kout is derived from either one of 28 received DS1 line clock or the input lead CLKRefin. The clock to CLKRefin can be 64 KHz, 1.544 MHz, or 2.048 MHz. For the H.100/H.110 bus operation, the CLK_8Kout can be used as secondary network timing reference (CT_NETREF). This lead can also be tristated if not used. This is configured via API.

CLKDS1out: Output

The CLKDS1out could be one of 28 received DS1 line clock (i.e., 1.544 MHz), transmit DS1 reference clock, or tristated. This is configured via API.

DS1Frmout: Output

This lead generates a transmission framing pulse when the transmit reference clock is selected as CLKDS1out.

RCLKX8: Output

This lead generates a a synchronous high speed serial clock for multi-cycle data processing when DS3 clear channel mode is enabled. It is a 50 MHz output.

PLL_Aux_Clk: Input

For test use only.

XCK: Input

An external clock having a frequency of 44.736 MHz and a stability of +/- 20 PPM is required to meet DSX3 cross-connect requirements. The clock duty cycle shall be kept to (50 ± 5)%.

DPLLclk: Input

An external clock having a frequency of 50.0 MHz and a stability of +/- 30 PPM for internal DPLL operation. This clock duty cycle shall be kept to (50 ± 5)%.

HARDWARE RESET

To apply hardware reset:

- Power-on
- Assert lead $\overline{\text{RESET}}$ for 1 msec

After hardware reset is applied, the T3BwP will take the following actions:

- T3BwP reads the contents from EEPROM.
- First block of information is the control header (controlling how the EEPROM is operated.)
- Lead $\overline{\text{LD\_OK}}$ is asserted once the loading is done (at the completion of actual data load operation.)
- If Lead $\overline{\text{LD\_OK}}$ is not asserted within a certain time, it is possible that
  - -- EEPROM is not program properly,
  - -- or EEPROM is blank,
  - -- or EEPROM I/F malfunction

FIRMWARE RESET

To apply firmware reset:

- Assert $\overline{\text{RST\_SW}}$ to “low” for 1 msec.

After firmware reset is applied, the T3BwP will take the following actions:

- Skip over normal run-time code and configuration code (i.e., no reloading) in EEPROM.
- Go to location where contains the debug software.
- Load the debug code from EEPROM into IRAM.
- $\overline{\text{LD\_OK}}$ is asserted once the loading is done (at the completion of actual data load operation.)
- If Lead $\overline{\text{LD\_OK}}$ is not asserted within a certain time, it is possible that
  - -- EEPROM is not program properly,
  - -- or EEPROM is blank,
  - -- or EEPROM I/F malfunction

INITIAL STATE OF SYSTEM INTERFACE OUTPUT LEADS

After the device is powered up, the output leads of the system interface are in Hi-Z state. The output system interface leads are enabled via API. After system port is enabled, the lead status are as follows:

- Transmission port: leads are still tristated until DS1 cross connect is programmed.

- H.100/H.110 mode: If H100_sel=high, it will enable the all leads of ports 0-7 (release them from Hi-Z). The other output leads are still tristated until DS1 cross connect is programmed.

JTAG BACKGROUND INFORMATION

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 28. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{TRS}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a 16-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first. A timing diagram for the boundary scan feature is provided in Figure 19.

Boundary Scan Support

T3BwP executes the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- IDCODE

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay. When JTAG test reset ($\overline{TRS}$) is asserted, the BYPASS instruction is loaded by default.

IDCODE Test Instruction:

The format of the IDCODE test instruction is “10”.

Boundary Scan Reset

Specific control of the $\overline{TRS}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the T3BwP. If boundary scan testing is to be performed and the lead is held low, then a pulldown resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the ‘Input, Output and Input/Output Parameters’ section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

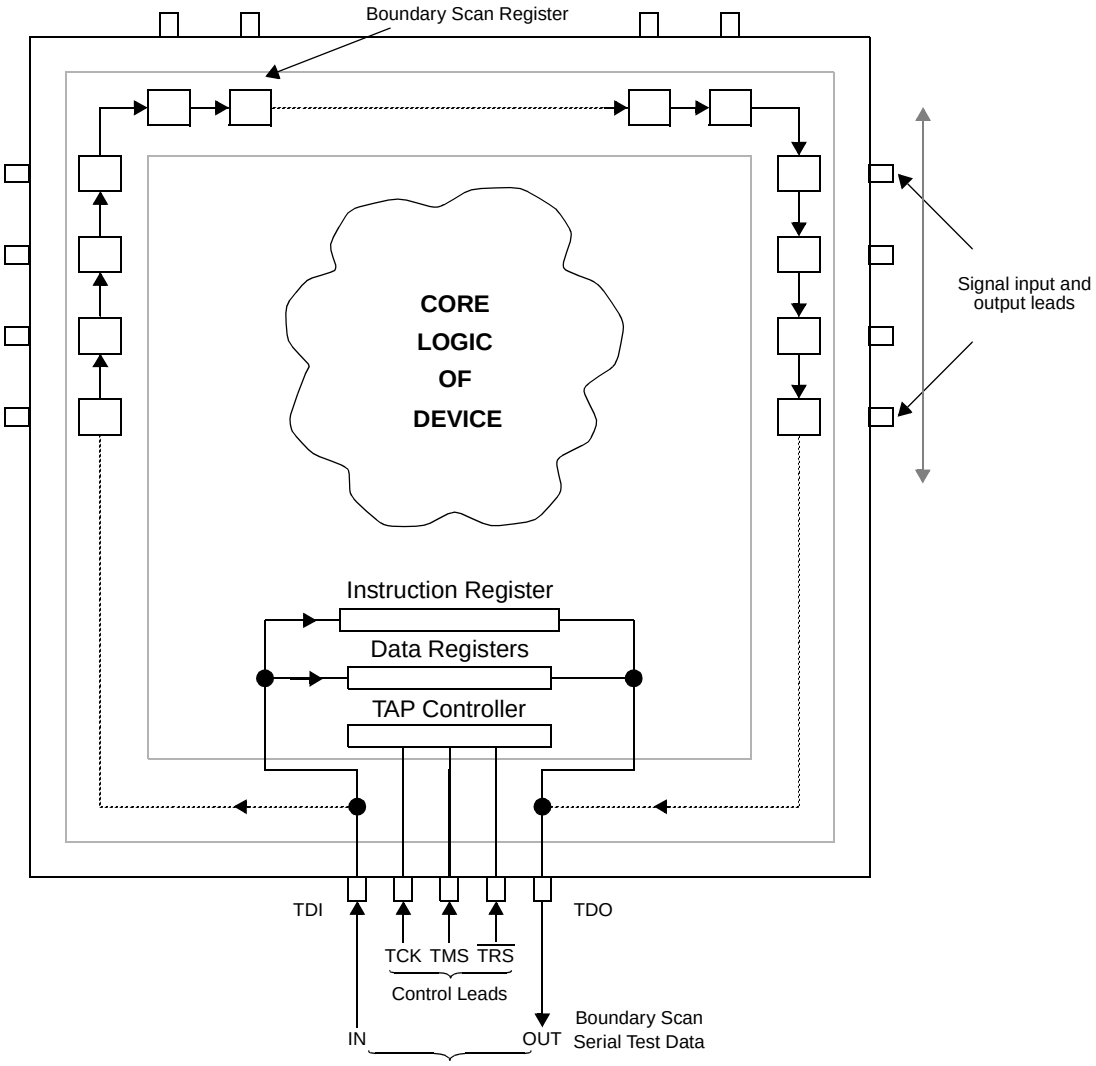

Figure 28. Boundary Scan Top-Level Block Diagram

In addition some TXC specific JTAG instructions are implemented.

MEMORY MAP

The control bits in the following read/write registers are set and accessed directly via read and write primitives. Please note that the T3BwP is mostly configured, controlled, and monitored via API.

Address	Bit	Symbol	Description
0M000N01 - line (Mx4 + N)[1] (M=0..6; N=1..4)	7	TXCP	**Transmit Clock Polarity Selection:** When set to 1, data for channel n is clocked out to the line on the rising edges of the transmit clock (TDS1Cn). When set to 0, data is clocked out on the falling edges of the transmit clock (TDS1Cn). This bit is set to '0' after hardware reset.
	6	RXCP	**Receive Clock Polarity Selection:** When set to 1, data for channel n is clocked in from the line on the rising edges of the receive clock (RDS1Cn). When set to 0, data is clocked in on the falling edges of the receive clock (RDS1Cn). This bit is set to '0' after hardware reset.
	5	TXNRZP	**Transmit NRZ Data Polarity Selection:** When set to 1, the polarity of the transmit NRZ data for channel n (TDS1Dn) is inverted. This bit is set to '0' after hardware reset.
	0	RXNRZP	**Receive NRZ Data Polarity Selection:** When set to 1, the polarity of the received NRZ data for channel n (RDS1Dn) is inverted. This bit is set to '0' after hardware reset.
0M000017 (M=0..6)[2]	7-0	TSD7-TSD0	**Transmit Sync Delay:** The value written into this register location specifies the number of transmit clock cycles (TCLKn) that the transmit Sync signal (TSYNCn) is delayed internal to the QT1F-*Plus*, in increments of one bit time. The default value is 00 hex.
0M000018 (M=0..6)[2]	7-0	RSD7-RSD0	**Receive Sync Delay:** The value written into this register location specifies the number of receive clock cycles (RCLKn) that the receive Sync signal (RSYNCn) is delayed internal to the QT1F-*Plus*, in increments of one bit time. The default value is 00 hex. This function is only available when RCLKn and RSYNCn are inputs (control bit RXC is set to 0).
07000000	1	XR2	**Receive DS3 X-bit Number 2:** This bit position indicates the receive state of X2. This bit position is updated each frame.
	0	XR1	**Receive DS3 X-bit Number 1:** This bit position indicates the receive state of X1. This bit position is updated each frame.
07000002	3	LPTIME	**Receive Loop Timing:** A one disables the transmit clock input (i_XCK), and causes the DS3 receive clock to become the DS3 transmit clock. If the DS3 receive clock fails in this mode, the M13X switches over to the transmit clock (i_XCK). The demultiplexer becomes inoperative, but the multiplexer and microprocessor interface continue to function.
07000019	7	C3CLKI	**C-Bit Parity C3 Clock Inhibit:** A zero enables the M13X to generate an extra clock pulse in the CCKT clock signal for clocking the C3 bit in from external logic. A one disables the generation of the C3 clock pulse. This bit must be set to 1 if the FEAC register 1CH is used to transmit FEAC codes or if register 07H is used to send a remote loopback request via a double word FEAC message (LBSEL = 1). If this bit is set to 0, then the FEAC messages are derived from the external C-bit interface.

Notes:

1. Each bit control setting for one DS1 line. For examples: M=0, N=1 is for DS1 line 1; M=6, N=4 is for DS1 line 28.
2. Each setting is set for 4 DS1 lines. Ex: M=0: for DS1 lines 1-4; M=6: for DS1 lines 25-28.

FIRMWARE/SOFTWARE ARCHITECTURE OVERVIEW

Figure 29 shows the connectivity model for the T3BwP device. The device contains a high performance processor that is responsible for interacting, controlling, and initializing the “cores” inside the T3BwP. The microprocessor controls the following core blocks:

1. DS3 block: this block provides the means to multiplex DS1 channels into DS3 channel and demultiplex DS3 data into its DS1 channels. The block is managed with the appropriate device driver that runs in the on-chip processor LMPro.
2. DS1 block: this block provides the framing for up to 28 DS1 lines. Similarly as in the DS3 case, the on-chip processor LMPro runs the device driver that controls the DS1 links.
3. Cross-connect block: two levels of cross-connect are available. The first is a DS1 cross-connect which can connect any input DS1 to any output DS1. The second is a cross-connect that can connect any DS0 to any DS0.

Additionally, the on-chip processor LMPro is responsible for managing the interface layer between the device drivers and the external message interface. This message interface provides the connectivity from specific user function calls to the T3BwP device and the actual device registers manipulations, which are transparent to the user.

The mechanism for message passing is provided by a shared media device. The interface is a set of FIFOs that can be accessed by both the host processor and the T3BwP’s on-chip processor. Some additional logic may be required to handle the control signals between both the host processor and the on-chip processor.

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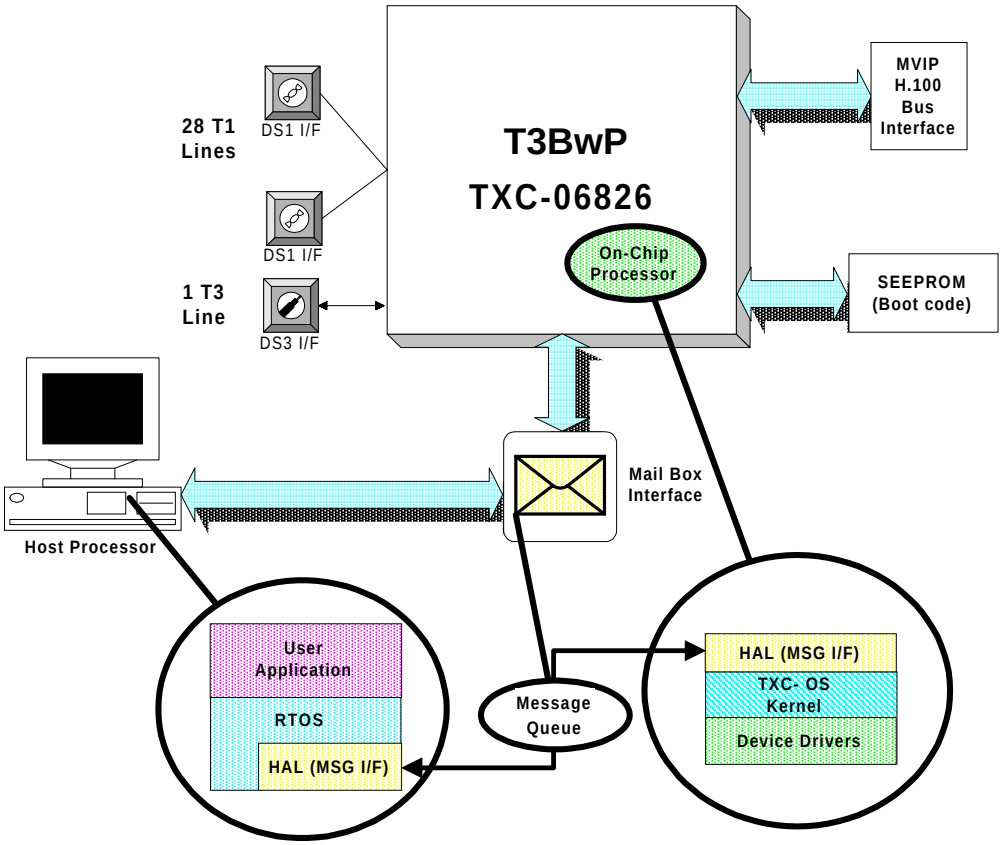


Figure 29. Software/Hardware Interaction for T3BwP

The “device driver library” will provide the hardware abstraction layer between the host application software and the device. An overview of the software layers and interfaces is given in Figure 30.

Host microprocessor software

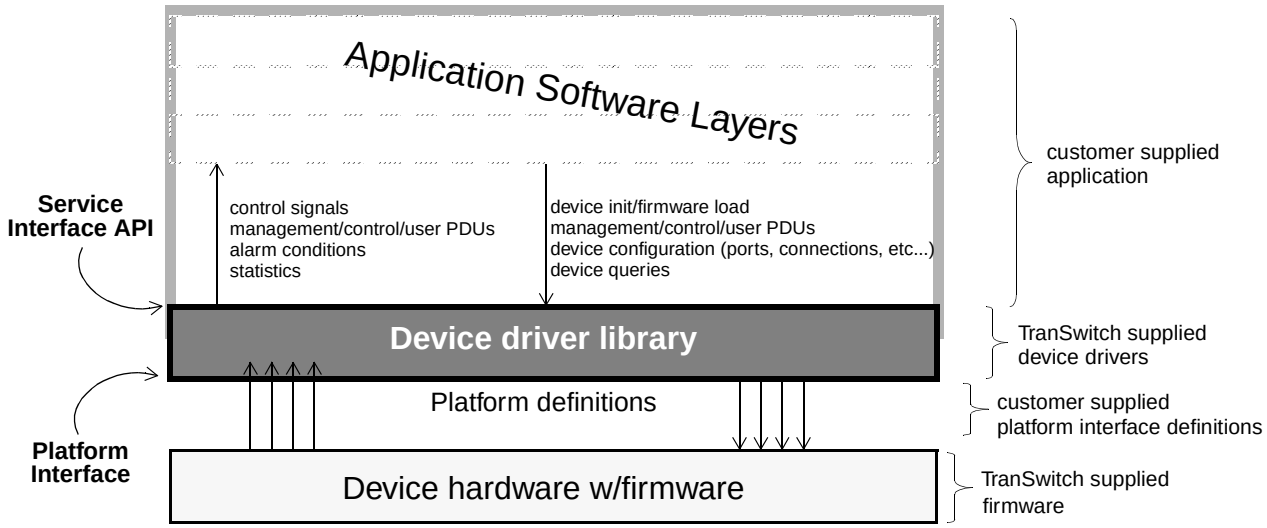


Figure 30. Software Interfaces

Application software communicates with the device driver via an Application Program Interface (API). The definition of the T3BwP API is provided in the T3BwP API Users Reference.

APPLICATIONS

The application diagram in Figure 31 shows the usage of the T3BwP in a telephony application.

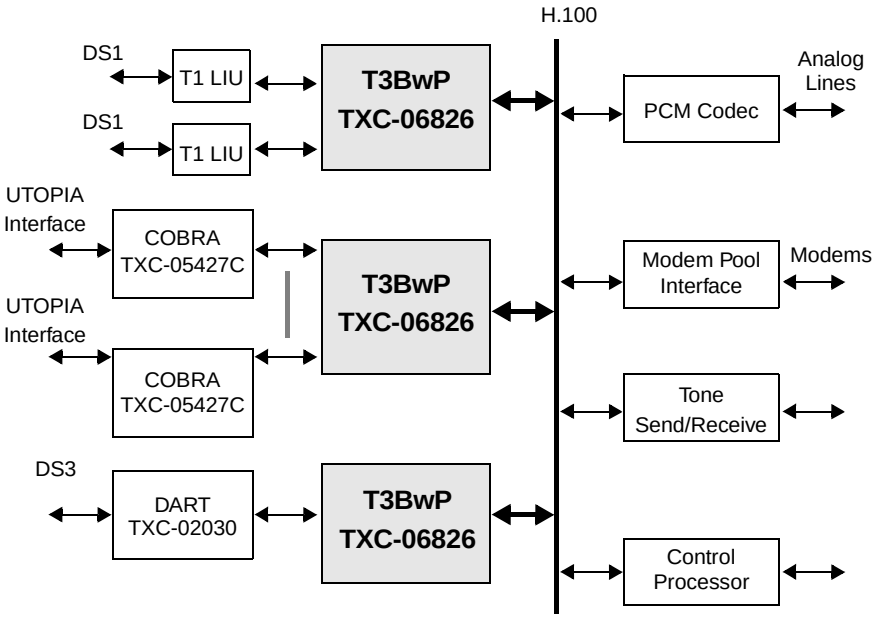


Figure 31. Telephony Application Using the T3BwP TXC-06826

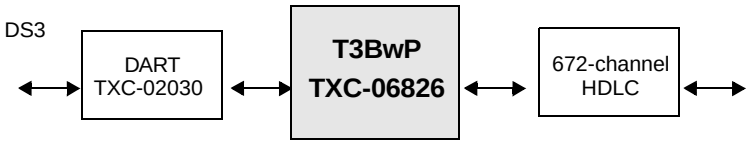
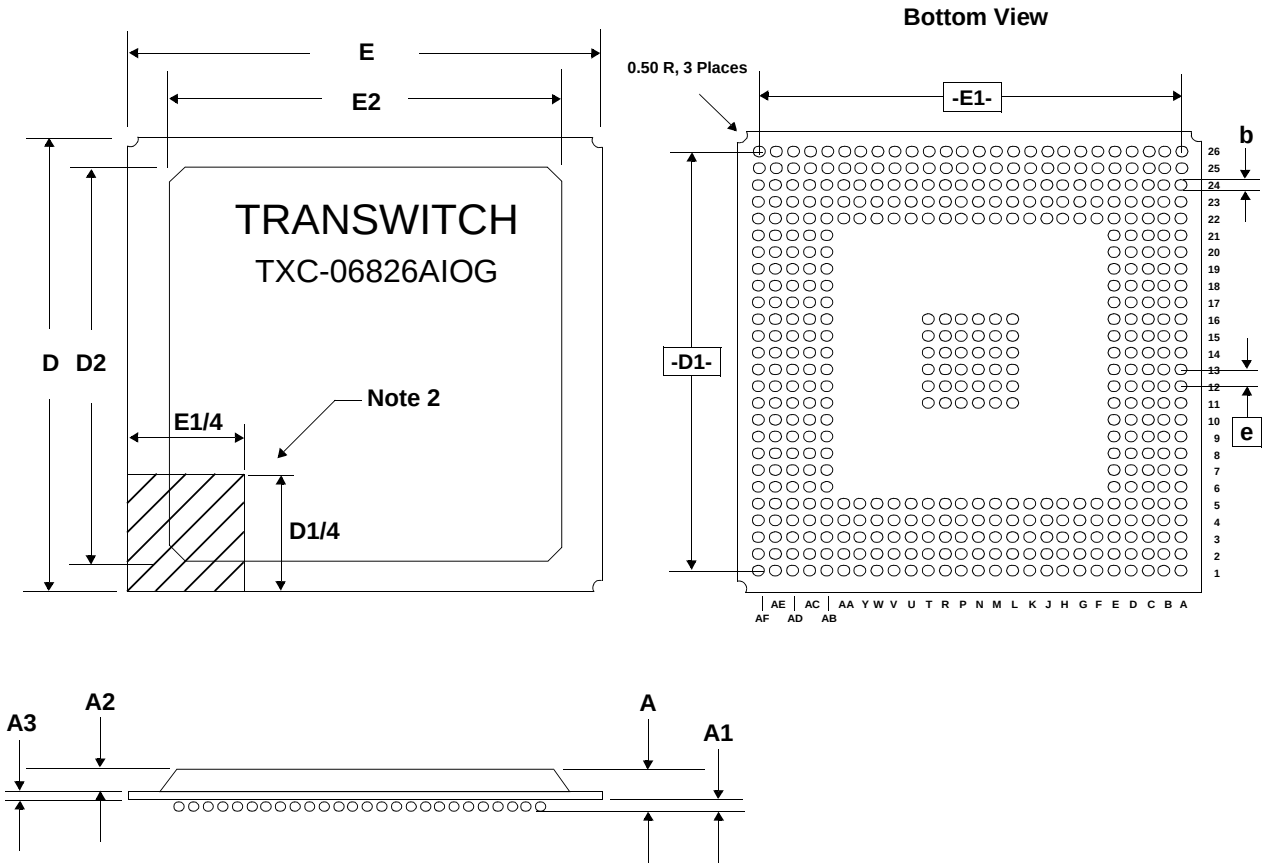


Figure 32. Complete DS3 RAC Using the T3BwP TXC-06826

PACKAGE INFORMATION

The T3BwP device is packaged in a 456-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 33.



Dimension (Note 1)	Min	Max
A (Nom)	2.23	
A1	0.40	0.60
A2 (Nom)	1.12	1.22
A3 (Nom)	0.56	
b (Ref.)	0.63	
D	27.00	
D1 (Nom)	25.00	
D2	23.95	24.70
E	27.00	
E1 (Nom)	25.00	
E2	23.95	24.70
e (Ref.)	1.00	

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.

Figure 33. T3BwP TXC-06826 456-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06826AIOG 456-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). The L3M maps a DS3 line signal into a STM-1 TUG-3 or STS-3/STS-1 SPE or STS-1 SPE SDH/SONET Signal.

TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). Maps seven 1.544 Mbit/s DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 virtual tributaries carried in a SONET or SDH synchronous payload envelope.

TXC-05150, CDB VLSI Device Cell Delineation Block (CDB). This device provides cell delineation for ATM cells carried in a physical line at rates of 1.544 Mbit/s to 155.52 Mbit/s.

TXC-05427C, COBRA VLSI Device (Constant Bit Rate ATM Adaptation Layer 1). Provides ATM AAL1 Structured and Unstructured service for four T1, E1 or n x 64k constant bit rate interfaces.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides SONET STS-1 overhead termination with section, line and path overhead processing.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: (650) 949-6700
Fax: (650) 949-6705
Web: www.atmforum.com

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79

ATM Forum Asia-Pacific Office

Hamamatsu-cho Suzuki Building 3F
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: (800) 854-7179 (within U.S.A.)
Tel: (314) 726-0444 (outside U.S.A.)
Fax: (314) 726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (508) 650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 693-6232 (outside U.S.A.)
Fax: (503) 693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: (800) 521-CORE (within U.S.A.)
Tel: (908) 699-5800 (outside U.S.A.)
Fax: (908) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsu-cho Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This updated Edition 3 Data Sheet has a number of changes relative to the Edition 2A. The following list of changes identifies the areas within this Edition 3 Data Sheet that have significant differences relative to the prior and now superseded Edition.

Updated T3BwP device Data Sheet: *PRODUCT PREVIEW* Edition 3, October 2001

Previous T3BwP device Data Sheet: *PRODUCT PREVIEW* Edition 2A, January 2001

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
Where occurs	Removed “ART” text from Data Sheet.
1	Changed Features, Description and Applications sections.
3, 4	Updated Table of Contents and List of Figures.
5	Changed first and last paragraph.
6	Changed text of all paragraphs. In the numbered list, changed the first and added the last.
7	Text on this page was changed extensively.
9 - 13	Changed the T3BwP Features section.
15	Changed Name/Function text for Symbols AV_{DD}, AV_{SS}, Spare, RE3G and TE3G. Provided entries for the I/O/P and Type columns for the Spare Leads (1) Table.
16	Changed Name/Function text for Symbols LCV, and $\overline{EXZ}$.
17-18	Added last sentence to Name/Function text for Symbols RDS1D8-21, RDS1D22-28, RDS1C2-21and RDS1C22-28.
19	Added last sentence to Name/Function text for Symbol RBPVn. Changed the symbol PAT23 to $\overline{PAT23}$ in the Symbol and Name/Function columns.
21	Added last sentence to Name/Function text for Symbol XCK. Changed Table heading.
22	For Symbol RCLK17, changed Type to CMOS3V 8mA changed last sentence of Name/Function text to read “When is high...”. Changed Symbol RDATA1-8/CTD1-8 to RDATA1-8/CTD0-7, changed Name Function text accordingly.
23	Changed Type to CMOS3V/4mA for Symbols RDATA18/RCLKX8, RDATA19/$\overline{RxValid}$, RDATA20/TxValid and RDATA21-28/RxData1-8. In the last row on the page, changed Symbol CTD9-16 to CTD8-15 and changed name function text accordingly.
24	Changed Type to 8mA for Symbol RFRM17/RSIG17/TxCellPkt. Changed Type to 4mA for Symbol RFRM18/RSIG18/TxClk.

Page Number of Updated Data Sheet	Summary of the Change
25	Changed Type to 4mA for Symbol RFRM19-28/RSIG19-28/TLCnum0-9. Added last sentence to Name/Function text for Symbols TCLK1 and TCLK2.
26	Added last sentence to the Name/Function text for each symbol on the page except CT_C8_B.
27	Added Symbol TCLK7/$\overline{\text{CT\_EN}}$ for Lead E21. Added Symbol TCLK8/$\overline{\text{CT\_RESET}}$ for Lead D21. Changed Symbol and associated Name/Function text from TCLK7-28 to TCLK9-28. Changed Symbol and associated Name/Function text from CTD17-24 to CTD16-23. Added last sentence to the Name/Function text for TLCK7, TLCK8, TCLK9-28, TDATA1-8, and TDATA9-20.
28	Added last sentence to Name/Function text to each Symbol in the first three rows. In the Name/Function text of the first row changed the first bold text in parenthesis to TDATA21-28. In the Name/Function text of the second row, changed the Symbol and associated Name/Function text from CTD25-32 to CTD24-31. Changed Type to 8mA for Symbol CLK_8Kout.
29	Added last sentence to the Name/Function text of CLKRefin. Changed the Name/Function text for Symbol PLL_Aux_ctrl and PLL_Aux_Clk. Changed last sentence to read “This lead should be tied low...” in the Name/Function text for Symbol H100_sel.
30	Changed of the I/O/P column to O(T) for Symbols MONCLK1, MONDout1 and MONCLK2. For Symbol MOTO added the last line to Name/Function text.
32	For symbols Reset/$\overline{\text{OE}}$ and $\overline{\text{SCE}}$ added last sentence which states the need for a pull up resistor to the Name/Function column. Changed the contents of the I/O/P column to O for Symbol $\overline{\text{LD\_OK}}$. Added last sentence to Name/Function text for Symbols TMS and TDI. For symbol $\overline{\text{TRS}}$ replaced text of the Name/Function column.
34	Added the $P_{DD\text{-}TOTAL}$ row to the end of the power requirements table.
35	In the Input Parameters Table for TTL3V$_P$ @ $V_{DD\text{-}IO}$ = +3.3V changed the test conditions symbol to $V_{DD\text{-}IO}$ for the Input Leakage Current row.
36	For V_{OL} in the three tables, changed $V_{DD\text{-}IO}$ to 3.45 in the Test Conditions column. For all three tables deleted the I_{OL} and I_{OH} rows.
37	For the first two Tables on the page changed $V_{DD\text{-}IO}$ to 3.45 in the Test Conditions column and deleted the I_{OL} and I_{OH} rows. In the last Table changed the Max value for the Input Leakage Current row, added Note and entered values for V_{OH} Min, V_{OL} Max, and deleted the I_{OL}, I_{OH} t_{RISE} and t_{FALL} rows.
39	Changed Figure 3 so that TDS3C (output) and TDS3D (output) are shown unbroken.
47, 48	For Figures 11 and 12, changed the heading text and added the Note below the last signal.
49	In Figure 13 added the signal $\overline{\text{LD\_OK}}$ to the diagram and table. In the Table changed the Min and Max values for Symbols t_{CEC1}, t_{CEC2} and t_{OE}.

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Page Number of Updated Data Sheet	Summary of the Change
50	Added Figure 14 and changed the Figure numbers to end of document.
51	Inside Figure 15, added a Note which begins “This timing is...”. In Figure 16 changed the name of the last signal to $\overline{EXZ}$ (input).
56	For Figure 22 changed the heading and added a Note which begins “MOTO pin must...”.
57	Deleted Figure 23, A/D Mux Write/Read Timing - Motorola Mode, renumbered Figures following Figure 22.
59	In Note 2 below the table, changed the lead name from PAT23 to $\overline{PAT23}$.
62	Changed heading for Figure 25.
63	In the tenth row of Table 3 changed the I/O lead name to RDATA1-8/CTD0-7 and changed the right column heading.
64	Changed the right column heading.
65	Changed the I/O lead names in the first and fourth rows to TDATA1-8/CTD16-23 and TFRM1-8/TSIG1-8/CTD24-31 respectively. Changed the right column heading.
69	Changed the Control Lead name from PAT23 to $\overline{PAT23}$ in the fourth row of the Table.
71	Changed last sentence of the Microprocessor Interface paragraph.
72	Changed TCLK_64_A, TSYNC_64_A: Input and RCLK_64, RSYNC_64:Output sections to indicate For test use only.
73	Changed PLL_Aux_Clk: Input section to indicate For test use only.
81	Replaced the paragraph below Figure 30.
84	Removed ART device description from the Related Products section.

- NOTES -

- NOTES -

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