

# TISP61089

## DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

NOVEMBER 1995 - REVISED FEBRUARY 1998

### PROGRAMMABLE SLIC OVERVOLTAGE PROTECTION FOR LSSGR '1089

- **Dual Voltage-Programmable Protectors**
  - Wide 0 to -85 V Programming Range
  - Low 5 mA max. Gate Triggering Current
  - High 150 mA min. Holding Current

- **Rated for LSSGR '1089 Conditions**

| WAVE SHAPE      | '1089 TEST CLAUSE<br>AND TEST # | $I_{TSP}$<br>A |
|-----------------|---------------------------------|----------------|
| 2/10 $\mu$ s    | 4.5.8 Second-Level 1            | 120            |
| 10/1000 $\mu$ s | 4.5.7 First-Level 3             | 30             |

| 60 Hz POWER<br>FAULT TIME | '1089 TEST CLAUSE<br>AND TEST # | $I_{TSM}$<br>A |
|---------------------------|---------------------------------|----------------|
| 100 ms                    | 4.5.13 Second-Level 2           | 11             |
| 1 s                       | 4.5.13 Second-Level 2           | 4.5            |
| 5 s                       | 4.5.13 Second-Level 2           | 2.4            |
| 300 s                     | 4.5.13 Second-Level 1           | 0.95           |
| 900 s                     | 4.5.13 Second-Level 1           | 0.93           |

- **2/10 Protection Voltage Specified**

| ELEMENT                     | FIRST-LEVEL<br>V @ 56 A | SECOND-LEVEL<br>V @ 100 A |
|-----------------------------|-------------------------|---------------------------|
| Diode                       | 6                       | 8                         |
| Crowbar<br>$V_{GG} = -48$ V | -57                     | -60                       |

- **Also Rated for ITU-T 10/700 impulses**
- **Surface Mount and Through-Hole Options**
  - TISP61089P for Plastic DIP
  - TISP61089D for Small-Outline
  - TISP61089DR for Small-Outline Taped and Reeled

### description

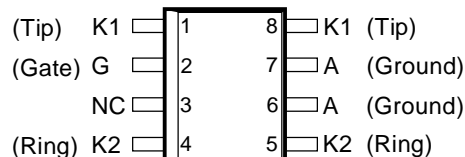
The TISP61089 is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on

the telephone line caused by lightning, a.c. power contact and induction. The TISP61089 limits voltages that exceed the SLIC supply rail voltage. The TISP61089 parameters are specified to allow equipment compliance with Bellcore GR-1089-CORE, Issue 1.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -10 V to -75 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will then track the negative supply voltage the overvoltage stress on the SLIC is minimised.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then

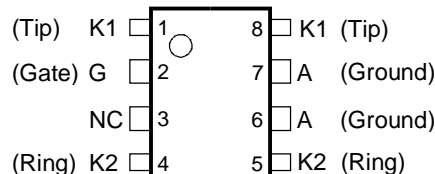
**D PACKAGE  
(TOP VIEW)**



MD6XAN

NC - No internal connection  
Terminal typical application names shown in parenthesis

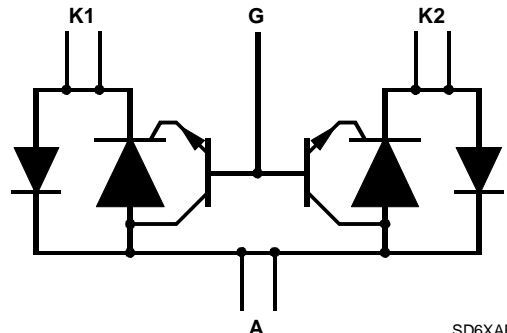
**P PACKAGE  
(TOP VIEW)**



MD6XAV

NC - No internal connection  
Terminal typical application names shown in parenthesis

### device symbol



SD6XAE

Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage,  $V_{GG}$ , applied to the G terminal.

# TISP61089

## DUAL FORWARD-CONDUCTING P-GATE THYRISTORS

### PROGRAMMABLE OVERVOLTAGE PROTECTORS

NOVEMBER 1995 - REVISED FEBRUARY 1998

the protector will crowbar into a low voltage on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup.

The TISP61089 is intended to be used with a series combination of a 25  $\Omega$  or higher resistance and a suitable overcurrent protector. Power fault compliance requires the series overcurrent element to open-circuit or become high impedance (see Applications Information). For equipment compliant to ITU-T recommendations K20 or K21 only, the series resistor value is set by the power cross requirements. For K20 and K21, a minimum series resistor value of 10  $\Omega$  is recommended.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISP61089 buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The TISP61089 is available in 8-pin plastic small-outline surface mount package and 8-pin plastic dual-in-line package.

#### absolute maximum ratings

| RATING  | SYMBOL            | VALUE                            | UNIT             |
|---|-------------------|----------------------------------|------------------|
| Repetitive peak off-state voltage, $I_G = 0$ , $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$   | $V_{\text{DRM}}$  | -100                             | V                |
| Repetitive peak gate-cathode voltage, $V_{KA} = 0$ , $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$   | $V_{\text{GKRM}}$ | -85                              | V                |
| Non-repetitive peak on-state pulse current (see Notes 1 and 2)<br>10/1000 $\mu\text{s}$ (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)<br>5/320 $\mu\text{s}$ (ITU-T recommendation K20 & K21, open-circuit voltage wave shape 10/700)<br>1.2/50 $\mu\text{s}$ (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4, Alternative)<br>2/10 $\mu\text{s}$ (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4) | $I_{\text{TSP}}$  | 30<br>40<br>100<br>120           | A                |
| Non-repetitive peak on-state current, 60 Hz (see Notes 1 and 2)<br>0.1 s<br>1 s<br>5 s<br>300 s<br>900 s  | $I_{\text{TSM}}$  | 11<br>4.5<br>2.4<br>0.95<br>0.93 | A                |
| Non-repetitive peak gate current, 1/2 $\mu\text{s}$ pulse, cathodes commoned (see Notes 1 and 2)  | $I_{\text{GSM}}$  | 40                               | A                |
| Operating free-air temperature range  | $T_A$             | -40 to +85                       | $^\circ\text{C}$ |
| Junction temperature  | $T_J$             | -40 to +150                      | $^\circ\text{C}$ |
| Storage temperature range   | $T_{\text{stg}}$  | -40 to +150                      | $^\circ\text{C}$ |

- NOTES: 1. Initially the protector must be in thermal equilibrium with  $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ . The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above  $85^\circ\text{C}$ , derate linearly to zero at  $150^\circ\text{C}$  lead temperature.

#### recommended operating conditions

|   | MIN | TYP | MAX | UNIT     |
|---|-----|-----|-----|----------|
| $C_G$ Gate decoupling capacitor   | 100 | 220 |     | nF       |
| $R_S$ TISP61089 series resistor for first-level and second-level surge survival | 40  |     |     | $\Omega$ |
| TISP61089 series resistor for first-level surge survival                        | 25  |     |     |          |

**TISP61089**  
**DUAL FORWARD-CONDUCTING P-GATE THYRISTORS**  
**PROGRAMMABLE OVERVOLTAGE PROTECTORS**

NOVEMBER 1995 - REVISED FEBRUARY 1998

**electrical characteristics,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)**

| PARAMETER  |                                     | TEST CONDITIONS  | MIN                      | TYP | MAX | UNIT          |
|------------|-------------------------------------|--|--------------------------|-----|-----|---------------|
| $I_D$      | Off-state current                   | $V_D = -85\text{ V}$ , $V_{GK} = 0$  | $T_J = 25^\circ\text{C}$ |     | -5  | $\mu\text{A}$ |
|            |                                     |  | $T_J = 85^\circ\text{C}$ |     | -50 | $\mu\text{A}$ |
| $V_{(BO)}$ | Breakover voltage                   | 2/10 $\mu\text{s}$ , $I_T = -56\text{ A}$ , $R_S = 45\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$   |                          | -57 |     | V             |
|            |                                     | 2/10 $\mu\text{s}$ , $I_T = -100\text{ A}$ , $R_S = 50\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$  |                          | -60 |     |               |
|            |                                     | 1.2/50 $\mu\text{s}$ , $I_T = -53\text{ A}$ , $R_S = 47\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$ |                          | -60 |     |               |
|            |                                     | 1.2/50 $\mu\text{s}$ , $I_T = -96\text{ A}$ , $R_S = 52\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$ |                          | -64 |     |               |
| $V_F$      | Forward voltage                     | $I_F = 5\text{ A}$ , $t_w = 200\ \mu\text{s}$  |                          |     | 3   | V             |
| $V_{FRM}$  | Peak forward recovery voltage       | 2/10 $\mu\text{s}$ , $I_F = 56\text{ A}$ , $R_S = 45\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$    |                          | 6   |     | V             |
|            |                                     | 2/10 $\mu\text{s}$ , $I_F = 100\text{ A}$ , $R_S = 50\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$   |                          | 8   |     |               |
|            |                                     | 1.2/50 $\mu\text{s}$ , $I_F = 53\text{ A}$ , $R_S = 47\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$  |                          | 8   |     |               |
|            |                                     | 1.2/50 $\mu\text{s}$ , $I_F = 96\text{ A}$ , $R_S = 52\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$  |                          | 12  |     |               |
| $I_H$      | Holding current                     | $I_T = -1\text{ A}$ , $di/dt = 1\text{ A/ms}$ , $V_{GG} = -48\text{ V}$  | -150                     |     |     | mA            |
| $I_{GAS}$  | Gate reverse current                | $V_{GG} = V_{GK} = -75\text{ V}$ , $V_{KA} = 0$  | $T_J = 25^\circ\text{C}$ |     | -5  | $\mu\text{A}$ |
|            |                                     |  | $T_J = 85^\circ\text{C}$ |     | -50 | $\mu\text{A}$ |
| $I_{GT}$   | Gate trigger current                | $I_T = 3\text{ A}$ , $t_{p(g)} \geq 20\ \mu\text{s}$ , $V_{GG} = -48\text{ V}$                                     |                          |     | 5   | mA            |
| $V_{GT}$   | Gate trigger voltage                | $I_T = 3\text{ A}$ , $t_{p(g)} \geq 20\ \mu\text{s}$ , $V_{GG} = -48\text{ V}$                                     |                          |     | 2.5 | V             |
| $Q_{GS}$   | Gate switching charge               | 1.2/50 $\mu\text{s}$ , $I_T = 53\text{ A}$ , $R_S = 47\ \Omega$ , $V_{GG} = -48\text{ V}$ , $C_G = 220\text{ nF}$  |                          | 0.1 |     | $\mu\text{C}$ |
| $C_{AK}$   | Anode-cathode off-state capacitance | $f = 1\text{ MHz}$ , $V_d = 1\text{ V}$ , $I_G = 0$ , (see Note 3)   | $V_D = -3\text{ V}$      |     | 100 | pF            |
|            |                                     |  | $V_D = -48\text{ V}$     |     | 50  | pF            |

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

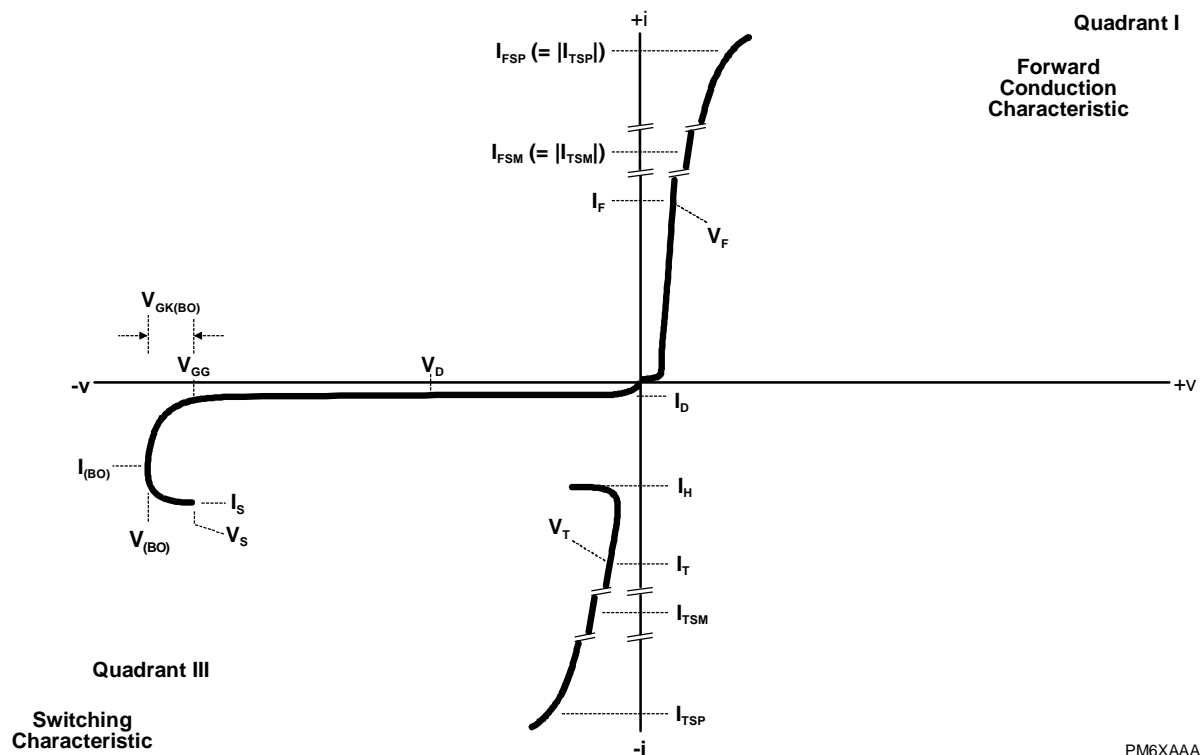
**thermal characteristics**

| PARAMETER       |   | TEST CONDITIONS  | MIN       | TYP | MAX | UNIT               |
|-----------------|---|--|-----------|-----|-----|--------------------|
| $R_{\theta JA}$ | Junction to free air thermal resistance | $P_{tot} = 0.8\text{ W}$ , $T_A = 25^\circ\text{C}$<br>5 cm <sup>2</sup> , FR4 PCB | D Package |     | 160 | $^\circ\text{C/W}$ |
|                 |   |  | P Package |     | 100 |                    |

**TISP61089**  
**DUAL FORWARD-CONDUCTING P-GATE THYRISTORS**  
**PROGRAMMABLE OVERVOLTAGE PROTECTORS**

NOVEMBER 1995 - REVISED FEBRUARY 1998

**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. VOLTAGE-CURRENT CHARACTERISTIC**

## THERMAL INFORMATION

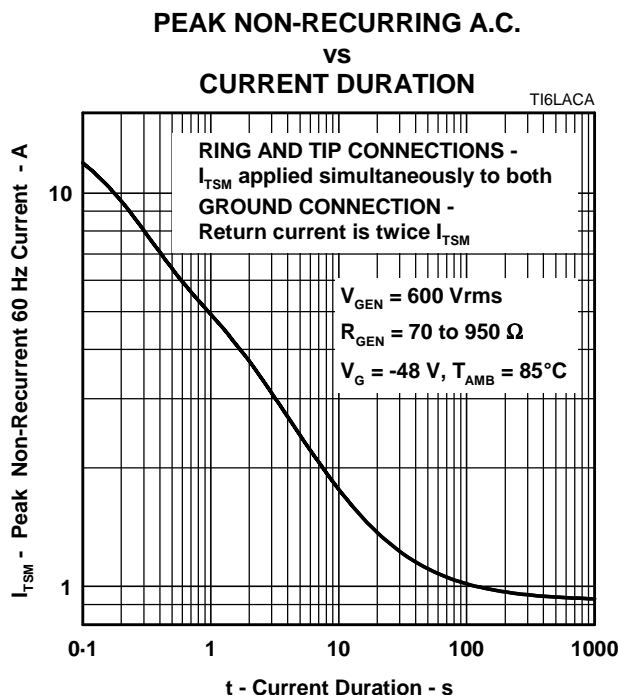


Figure 2. NON-REPETITIVE PEAK ON-STATE CURRENT AGAINST DURATION

## APPLICATIONS INFORMATION

### gated protectors

This section covers three topics. Firstly, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, an example application circuit is described.

#### purpose of gated protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

SLICs have become more sophisticated. To minimise power consumption, some designs automatically adjust the supply voltage,  $V_{BAT}$ , to a value that is just sufficient to drive the required line current. For short lines the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC supply, Figure 3. This gated (programmable) protection arrangement minimises the voltage stress on the SLIC, no matter what value of supply voltage.

# TISP61089 DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

NOVEMBER 1995 - REVISED FEBRUARY 1998

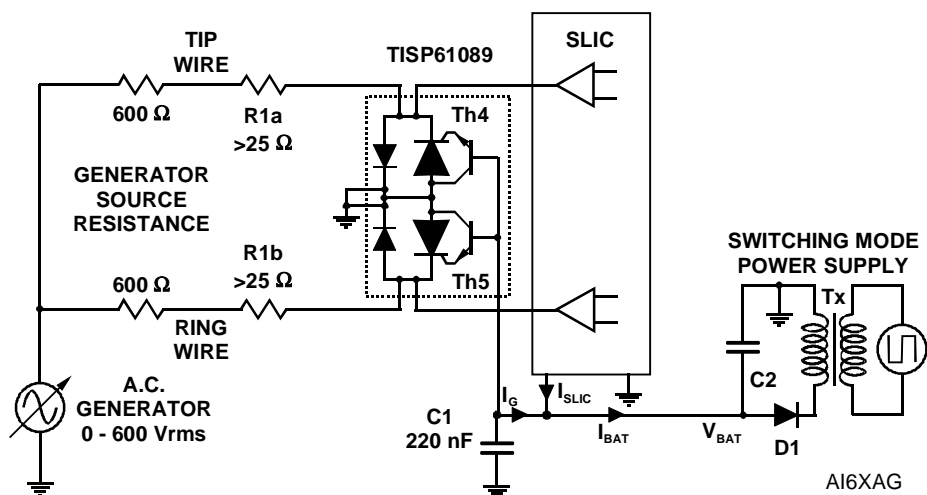


Figure 3. TISP61089 BUFFERED GATE PROTECTOR (SECTION 4.5.12 TESTING CONDITION)

## operation of gated protectors

Figures 4. and 5. show how the TISP61089 limits negative and positive overvoltages. Positive overvoltages (Figure 5) are clipped by the antiparallel diodes in the TISP61089 and the resulting current is diverted to ground. Negative overvoltages (Figure 4.) are initially clipped close to the SLIC negative supply rail value ( $V_{BAT}$ ). If sufficient current is available from the overvoltage, then the protector (Th5) will crowbar into a low voltage on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup. The protection voltage will be the sum of the gate supply ( $V_{BAT}$ ) and the peak gate-cathode voltage ( $V_{GK(BO)}$ ). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current ( $I_G$ ) is the same as the cathode current ( $I_K$ ). Rates of 70 A/μs can cause inductive voltages of 0.7 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimised by routing the SLIC connection through the protector as shown in Figure 3.

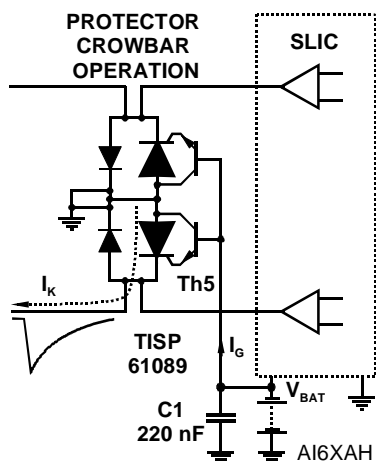


Figure 4. NEGATIVE OVERVOLTAGE CONDITION

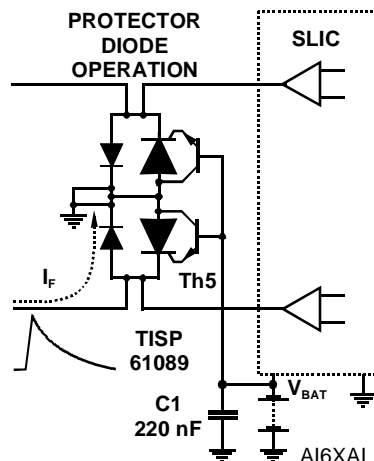
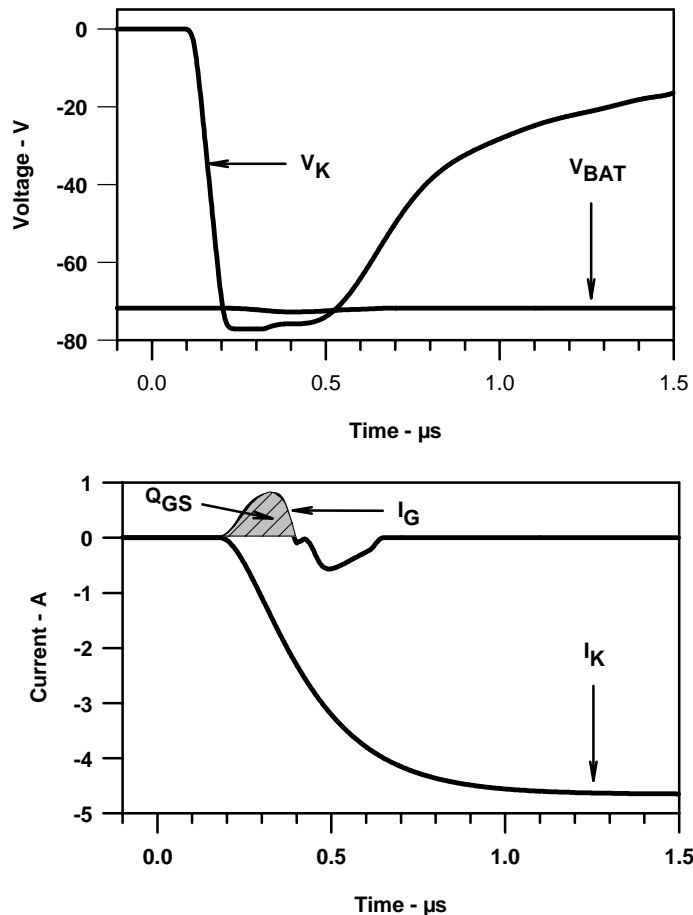


Figure 5. POSITIVE OVERVOLTAGE CONDITION

In Figure 6, the positive gate charge ( $Q_{GS}$ ) is about  $0.1 \mu\text{C}$  which, with the  $0.1 \mu\text{F}$  gate decoupling capacitor used, increased the gate supply by about  $1 \text{ V}$  ( $= Q_{GS}/C1$ ). This change is just visible on the  $-72 \text{ V}$  gate voltage,  $V_{BAT}$ . This increase does not directly add to the protection voltage as the supply voltage change reaches a maximum at  $0.4 \mu\text{s}$  when the gate current reverses polarity; whereas the protection voltage peaks at  $0.3 \mu\text{s}$ . In Figure 6, the peak clamping voltage ( $V_{(BO)}$ ) is  $-77.5 \text{ V}$ , an increase of  $5.5 \text{ V}$  on the nominal gate supply voltage. This  $5.5 \text{ V}$  increase is the sum of the supply rail increase at that time, ( $0.5 \text{ V}$ ), and the protection circuits cathode diode to supply rail breakover voltage ( $5 \text{ V}$ ). In practice, use of the recommended  $220 \text{ nF}$  gate decoupling capacitor would give a supply rail increase of  $0.25 \text{ V}$  and a  $V_{(BO)}$  value of about  $-77.25 \text{ V}$ .



**Figure 6. PROTECTOR FAST IMPULSE CLAMPING AND SWITCHING WAVEFORMS**

### application circuit

Figure 7 shows a typical TISP61089 SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the TISP61089 and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

# TISP61089 DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

NOVEMBER 1995 - REVISED FEBRUARY 1998

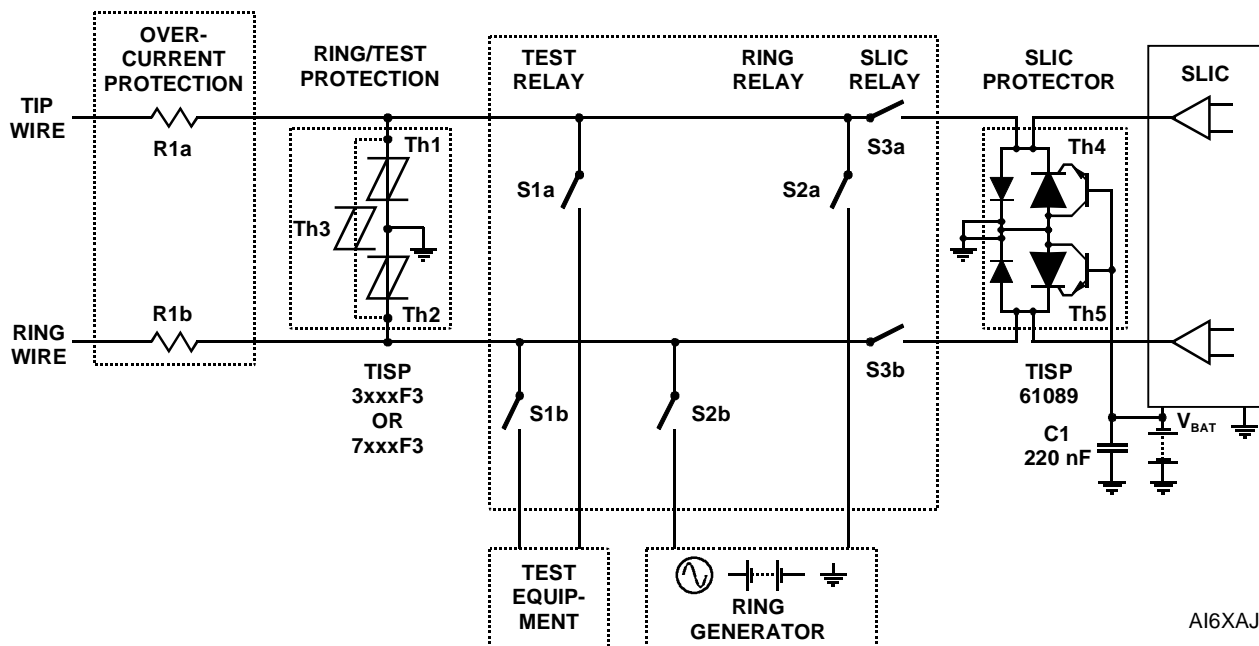


Figure 7. TYPICAL APPLICATION CIRCUIT

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISP61089 protector. The protector gate reference voltage comes from the SLIC negative supply ( $V_{BAT}$ ). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

## LSSGR 1089

GR-1089-CORE, "1089", covers electromagnetic compatibility and electrical safety generic criteria for US network telecommunication equipment. It is a module in Volume 3 of LSSGR (LATA (Local Access Transport Area) Switching Systems Generic Requirements, FR-NWT-000064). In 1089 surge and power fault immunity tests are done at two levels. After first-level testing the equipment shall not be damaged and shall continue to operate correctly. Under second level testing the equipment shall not become a safety hazard. The equipment is permitted to fail as a result of second-level testing. When the equipment is to be located on customer premises, second-level testing includes a wiring simulator test, which requires the equipment to reduce the power fault current below certain values.

The following clauses reference the 1089 section and calculate the protector stress levels. The TISP61089 is specified for use with a 40  $\Omega$  series resistor. This resistor value will ensure that the TISP61089 survives second level surge testing. Values down to 25  $\Omega$  may be used if some second level surge failure is acceptable. All the tabulated values are for a series resistance of 40  $\Omega$ . Peak current values for a 25  $\Omega$  series resistor are covered in the clause text.

The values of protector current are calculated from the open circuit generator voltage divided by the sum of the total circuit resistance. The total circuit resistance is the sum of the generator fictive source resistance and the TISP61089 series resistor value. Most generators have multiple outputs and each output connects to an individual line conductor. For those generators that have a single output, each conductor will have an effective generator fictive source resistance of  $n$  times the generator fictive source resistance, where  $n$  is the number of conductors simultaneously tested.



#### section 4.5.7 - first-level surge testing

The two most significant test wave shapes in this section are the high energy 10/1000 and the high current 2/10. As shown in table 1, the peak currents for these surges are 2x20 A and 2x56 A respectively. The protector must survive the 2x20 A 10/1000 surge and the TISP61089 will do this as its rating is 2x30 A. When both conductors are surged simultaneously the return (anode) current will be 40 A, again the TISP61089 will survive this as its rating for this condition will be 60 A. Similarly the TISP61089 will survive the 2x56 A 2/10 as its rating is 2x120 A.

**table 1. first-level surge currents**

| WAVE SHAPE                 | OPEN-CIRCUIT<br>VOLTAGE<br>V | SHORT-CIRCUIT<br>CURRENT<br>A | GENERATOR<br>FICTIVE<br>SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_T$<br>A |
|----------------------------|------------------------------|-------------------------------|--|---|------------|
| 2/10                       | 2500                         | 500                           | 5  | 45                                      | 2x56       |
| 1.2/50, 8/20<br>(See Text) | 2500                         | 360                           | 4 + 3  | 47                                      | 2x53       |
| 10/360                     | 1000                         | 100                           | 10   | 50                                      | 2x20       |
| 10/1000                    | 600                          | 100                           | 6  | 46                                      | 2x13       |
| 10/1000                    | 1000                         | 100                           | 10   | 50                                      | 2x20       |

The highest protection voltage will be for the 56 A 2/10 wave shape. Under this condition the average rate of current rise will be  $56/2 = 28 \text{ A}/\mu\text{s}$ . The value of diode and thyristor voltage under this condition is specified in the electrical characteristics.

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, adds the alternative of using the IEEE C62.41 1.2/50-8/20 combination wave generator for the 2/10 test. This generator usually has a single output and a fictive resistance of  $2 \Omega$ . The 2/10 generator has a fictive output resistance  $5 \Omega$ , (2500/500), and GR-1089-CORE compensates for this by adding an extra  $3 \Omega$  in the output of the 1.2/50-8/20 generator. In practice, the extra  $3 \Omega$  causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089 will survive the 2x53 A 1.2/50 as its rating is 2x100 A.

Using a  $25 \Omega$  series resistor will result in table 1.  $I_T$  column values of 2x83, 2x78, 2x29, 2x19 and 2x29. The TISP61089 will survive these peak current values as they are lower than the TISP61089 ratings.

#### section 4.5.8 - second-level surge testing

This is a 2/10 wave shape test. As shown in table 2, the peak current for this surge is 2x100 A. The TISP61089 will survive the 2x100 A 2/10 surge as its rating is 2x120 A.

Under this condition the average rate of current rise will be  $100/2 = 50 \text{ A}/\mu\text{s}$ . The value of diode and thyristor voltage under this condition is specified in the electrical characteristics.

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, adds the alternative of using the IEEE C62.41 1.2/50-8/20 combination wave generator for the 2/10 test. The 2/10 generator has a fictive output resistance  $10 \Omega$ , (5000/500), and GR-1089-CORE compensates for this by adding an extra  $8 \Omega$  in the output of the 1.2/50-8/20 generator. In practice, the extra  $8 \Omega$  causes the

**TISP61089**  
**DUAL FORWARD-CONDUCTING P-GATE THYRISTORS**  
**PROGRAMMABLE OVERVOLTAGE PROTECTORS**

NOVEMBER 1995 - REVISED FEBRUARY 1998

**table 2. second-level surge current**

| WAVE SHAPE                 | OPEN-CIRCUIT<br>VOLTAGE<br>V | SHORT-CIRCUIT<br>CURRENT<br>A | GENERATOR<br>FICTIVE<br>SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL<br>CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_T$<br>A |
|----------------------------|------------------------------|-------------------------------|--|--|------------|
| 2/10                       | 5000                         | 500                           | 10   | 50   | 2x100      |
| 1.2/50, 8/20<br>(See Text) | 5000                         | 420                           | 4 + 8/conductor  | 52   | 2x96       |

prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089 will survive the 2x96 A 1.2/50 as its rating is 2x100 A.

Using a 25  $\Omega$  series resistor will result in table 2.  $I_T$  column values of 2x143 and 2x135. The TISP61089 may fail at these peak current values as they are higher than the TISP61089 ratings.

**section 4.5.9 - Intra-building surge testing**

These tests use a 2/10 wave shape. As shown in table 3, the peak currents for this test are 2x27 A and 17 A. The TISP61089 can survive both these levels as its rating is 2x120 A.

**table 3. intra-building surge currents**

| WAVE SHAPE                 | OPEN-CIRCUIT<br>VOLTAGE<br>V | SHORT-CIRCUIT<br>CURRENT<br>A | GENERATOR<br>FICTIVE<br>SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_T$<br>A |
|----------------------------|------------------------------|-------------------------------|--|---|------------|
| 2/10                       | 1500                         | 100                           | 15   | 55                                      | 2x27       |
|                            | 800                          | 100                           | 8  | 48                                      | 17         |
| 1.2/50, 8/20<br>(See Text) | 1500                         | 94                            | 4 + 12/conduc-<br>tor                                    | 56                                      | 2x27       |
|                            | 800                          | 100                           | 2 + 6  | 48                                      | 17         |

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, the 2/10 alternative of using a CCITT Recommendation K.22 1.2/50-8/20 combination wave generator has been changed to an IEEE C62.41 1.2/50-8/20 generator. This generator usually has a single output and a fictive resistance of 2  $\Omega$ . The 2/10 generator has fictive output resistances of 15  $\Omega$  and 8  $\Omega$ . GR-1089-CORE compensates for this by adding an extra resistances of 12  $\Omega$  and 6  $\Omega$  in the output of the 1.2/50-8/20 generator. In practice, this extra resistance causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089 will survive the 2x27 A 1.2/50 as its rating is 2x100 A.

Using a 25  $\Omega$  series resistor will result in table 3.  $I_T$  column values of 2x38, 24, 2x37 and 24. The TISP61089 will survive these peak current values as they are lower than the TISP61089 ratings.

#### section 4.5.12 - first-level power fault testing

The most significant tests are a long duration (900 s) medium current test and a higher current tests of 60 one second power applications. As shown in table 4, the peak currents for these tests are 2x0.37 A and 2x1.3 A respectively. The TISP61089 will survive both these conditions as its ratings are 2x0.93 A and 2x4.5 A for these time periods

**table 4. first-level power fault currents**

| A.C.<br>DURATION<br>s | OPEN-CIRCUIT<br>RMS VOLTAGE<br>V | SHORT-CIRCUIT<br>RMS CURRENT<br>A | SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_{TRMS}$<br>A | $I_{TM}$<br>A |
|-----------------------|----------------------------------|-----------------------------------|----------------------------------|---|-----------------|---------------|
| 1                     | 200                              | 0.33                              | 600                              | 640                                     | 2x0.31          | 2x0.44        |
| 1                     | 400                              | 0.67                              | 600                              | 640                                     | 2x0.63          | 2x0.88        |
| 1                     | 600                              | 1                                 | 600                              | 640                                     | 2x0.94          | 2x1.3         |
| 1                     | 1000                             | 1                                 | 1000                             | 1040                                    | 2x0.96          | 2x1.3         |
| 900                   | 50                               | 0.33                              | 150                              | 190                                     | 2x0.26          | 2x0.37        |
| 900                   | 100                              | 0.17                              | 590                              | 630                                     | 2x0.16          | 2x0.22        |

Using a 25  $\Omega$  series resistor will result in table 4.  $I_{TM}$  column values of 2x0.45, 2x0.9, 2x1.4, 2x1.4, 2x0.4 and 2x0.23. The TISP61089 will survive these peak current values as they are lower than the TISP61089 ratings.

#### section 4.5.13 - second-level power fault testing

The two most significant tests are a long duration (900 s) medium current test and a higher current 5 s test. As shown in table 5, the peak currents for these tests are 2x17 A and 2x7.7 A respectively. For the TISP61089 to survive this test, the series current limiting element must operate within 0.1 s and 0.5 s respectively.

**table 5. second-level power fault currents**

| A.C.<br>DURATION<br>s | OPEN-CIRCUIT<br>RMS VOLTAGE<br>V | SHORT-CIRCUIT<br>CURRENT<br>A | SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL<br>CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_{TRMS}$<br>A | $I_{TM}$<br>A |
|-----------------------|----------------------------------|-------------------------------|----------------------------------|--|-----------------|---------------|
| 5                     | 600                              | 60                            | 10                               | 50   | 2x12            | 2x17          |
| 5                     | 600                              | 7                             | 86                               | 126  | 2x4.8           | 2x6.8         |
| 900                   | 120                              | 25                            | 5                                | 45   | 2x2.7           | 2x3.8         |
| 900                   | 277                              | 25                            | 11                               | 51   | 2x5.4           | 2x7.7         |
| 900                   | 100                              | 0.37                          | 273                              | 313  | 2x0.32          | 2x0.45        |
| 900                   | 300                              | 1.1                           | 273                              | 313  | 2x0.96          | 2x1.4         |
| 900                   | 600                              | 2.2                           | 273                              | 313  | 2x1.9           | 2x2.7         |

Using a 25  $\Omega$  series resistor will result in table 5.  $I_{TM}$  column values of 2x24, 2x7.7, 2x5.7, 2x11, 2x0.47, 2x1.4 and 2x2.9. The TISP61089 will probably fail for a peak current level of 2x24 A and the series current limiting

# TISP61089

## DUAL FORWARD-CONDUCTING P-GATE THYRISTORS

### PROGRAMMABLE OVERVOLTAGE PROTECTORS

NOVEMBER 1995 - REVISED FEBRUARY 1998

element must operate in under 0.1 s to prevent exceeding the TISP61089 package limit. For 2x7.7 A, the series current limiting element must operate within 0.4 s for TISP61089 survival.

#### section 4.5.15 - second-level power fault testing with wiring simulator

The purpose of this test is to ensure that the telephone cable does not become a hazard due to excessive current. A series fuse, type MDQ 1-6/10A, simulates the safe current levels of a telephone cable. If this fuse opens the equipment fails the test. For the equipment to pass, the equipment series overcurrent element must reduce the current to below the MDQ 1-6/10A fusing level to prevent the simulator operating. The a.c. test voltage can range from zero to 600 V, which gives a maximum conductor current of 10 A. Table 6 shows the simulator fusing times for three current levels.

**table 6. second-level power fault currents with MDQ 1-6/10A fuse**

| A.C.<br>DURATION<br>s | OPEN-CIRCUIT<br>RMS VOLTAGE<br>V | SHORT-<br>CIRCUIT<br>CURRENT<br>A | SOURCE<br>RESISTANCE<br>$\Omega$ | TOTAL<br>CIRCUIT<br>RESISTANCE<br>$\Omega$ | $I_{TRMS}$<br>A | $I_{TM}$<br>A | TIME<br>TO<br>OPEN<br>s |
|-----------------------|----------------------------------|-----------------------------------|----------------------------------|--|-----------------|---------------|-------------------------|
| 1000                  | 100                              | 5                                 | 20                               | 60   | 1.7             | 2.4           | $\infty$                |
| 1000                  | 300                              | 15                                | 20                               | 60   | 5.0             | 7.1           | 30                      |
| 1000                  | 600                              | 30                                | 20                               | 60   | 10              | 14            | 0.7                     |

Using a 25  $\Omega$  series resistor will result in table 6.  $I_{TM}$  column values of 2x3.1, 2x9.4 and 2x19. Simulator operating times will be  $\infty$ , 12 s and 0.4 s respectively

For the equipment to pass this test, the TISP61089 series current limiting element must operate before the MDQ 1-6/10A fusing times shown in table 7.

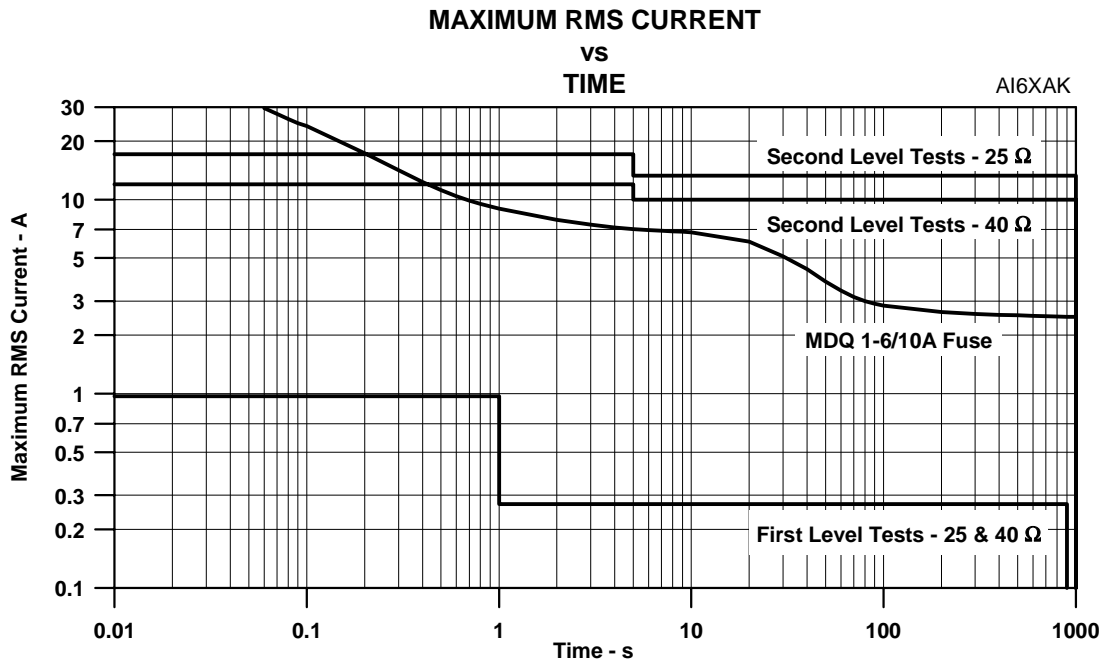
**table 7. operating times of MDQ 1-6/10A fuse**

| TIME TO<br>OPERATE<br>s | $I_{RMS}$<br>A |
|-------------------------|----------------|
| 0.2                     | 17             |
| 0.5                     | 12             |
| 1                       | 9              |
| 5                       | 7              |
| 10                      | 6.8            |
| 1000                    | 2.5            |

#### overcurrent protection

To meet '1089, the overcurrent protection must be coordinated with the requirements of sections 4.5.7, 4.5.8, 4.5.9, 4.5.12, 4.5.13, 4.5.15 and the TISP61089. The overcurrent protection must not fail in the first level tests of sections 4.5.7, 4.5.9 and 4.5.12. Recoverable overcurrent protectors (e.g. Positive Temperature Coefficient Resistors) may operate during first level testing, but normal equipment working must be restored after the test has ended. The test current levels and their duration are shown in Figure 8. First level tests have a high source resistance and the current levels are not strongly dependent on the TISP61089 series resistor value.

Second level tests have a low source resistance and the current levels are dependent on the TISP61089 series resistor value. The two stepped lines at the top of Figure 8 are for the 25  $\Omega$  and 40  $\Omega$  series resistor cases. If the full current-time durations occur the equipment will fail the wiring simulator test. The MDQ 1-6/10A fusing characteristic is also shown in Figure 8. The TISP61089 series overcurrent protection must operate before the MDQ 1-6/10A fuses, so this represents another boundary condition in the selection of the overcurrent protector.



**Figure 8. '1089 MAXIMUM TEST CURRENT LEVEL**

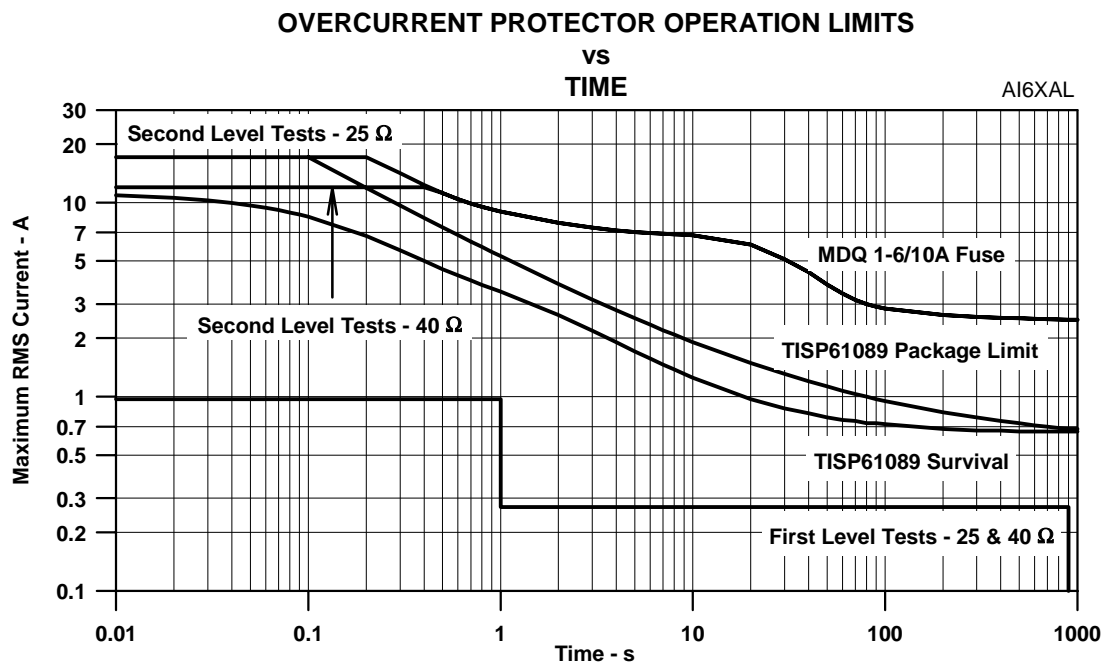
Figure 9 summarises these boundary conditions. The highest current levels that can flow are influenced by the TISP61089 series resistance. After one second the maximum current-time boundary becomes set by the MDQ 1-6/10A fusing characteristic. Fusible overcurrent protectors cannot operate at first level current levels.

Figure 9 shows two other curves. The lower one is the TISP61089 rated current. The overcurrent protector should not allow current-time durations greater than this otherwise the TISP61089 may fail. If second level failure is acceptable then the overcurrent protector *must* operate before the TISP61089 package limit is reached.

The TISP61089 a.c. ratings are worse case values when the device is mounted on the minimal sized PCB used for measuring thermal resistance. Typical PCBs would give a 25% increase in the rated currents for periods above 0.1 s.

**TISP61089**  
**DUAL FORWARD-CONDUCTING P-GATE THYRISTORS**  
**PROGRAMMABLE OVERVOLTAGE PROTECTORS**

NOVEMBER 1995 - REVISED FEBRUARY 1998



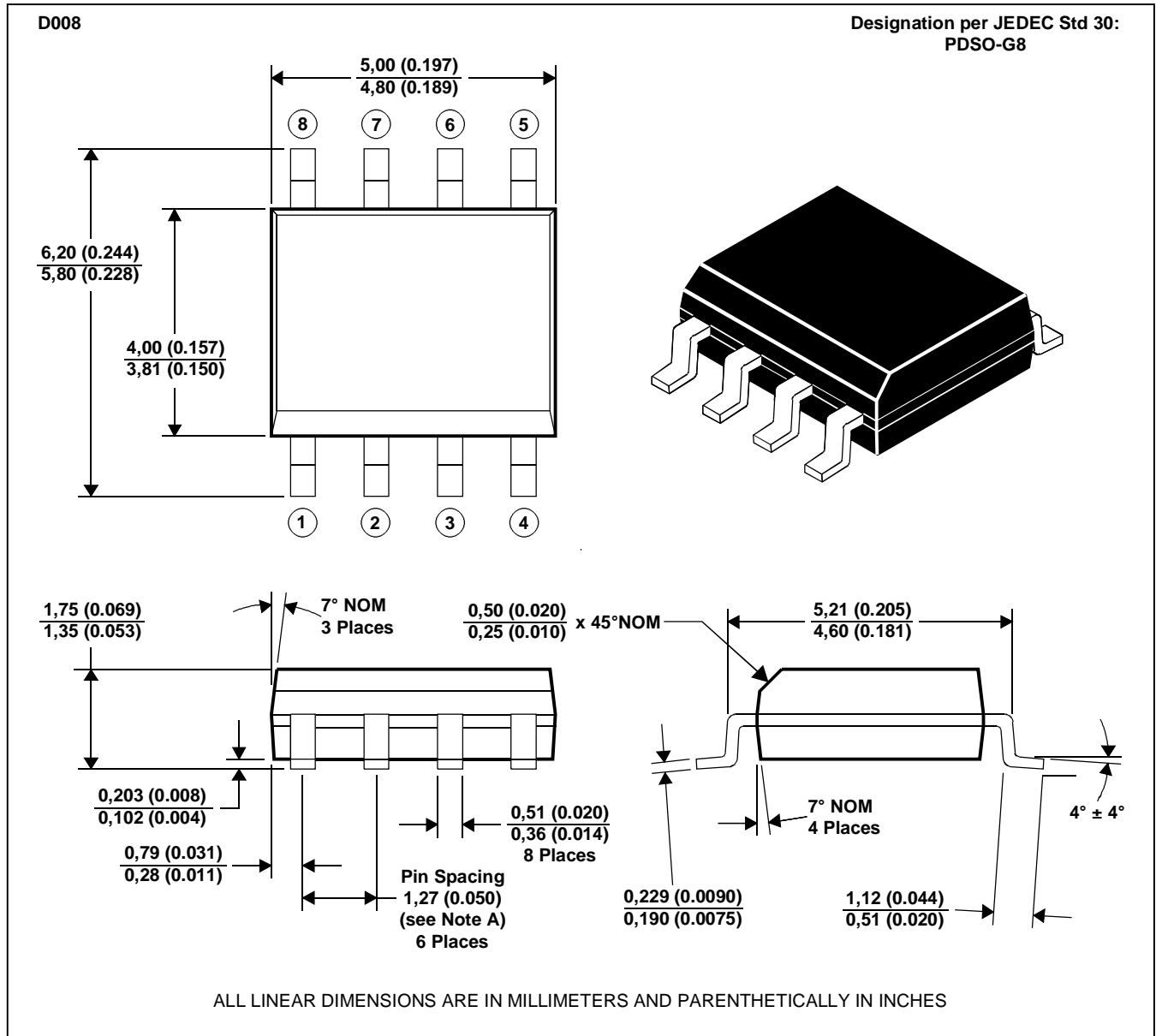
**Figure 9. OVERCURRENT PROTECTOR REQUIREMENTS**

## MECHANICAL DATA

### D008

#### plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.  
 B. Body dimensions do not include mold flash or protrusion.  
 C. Mold flash or protrusion shall not exceed 0,15 (0.006).  
 D. Lead tips to be planar within ±0,051 (0.002).

MDXXAA

**TISP61089**  
**DUAL FORWARD-CONDUCTING P-GATE THYRISTORS**  
**PROGRAMMABLE OVERVOLTAGE PROTECTORS**

NOVEMBER 1995 - REVISED FEBRUARY 1998

**MECHANICAL DATA**

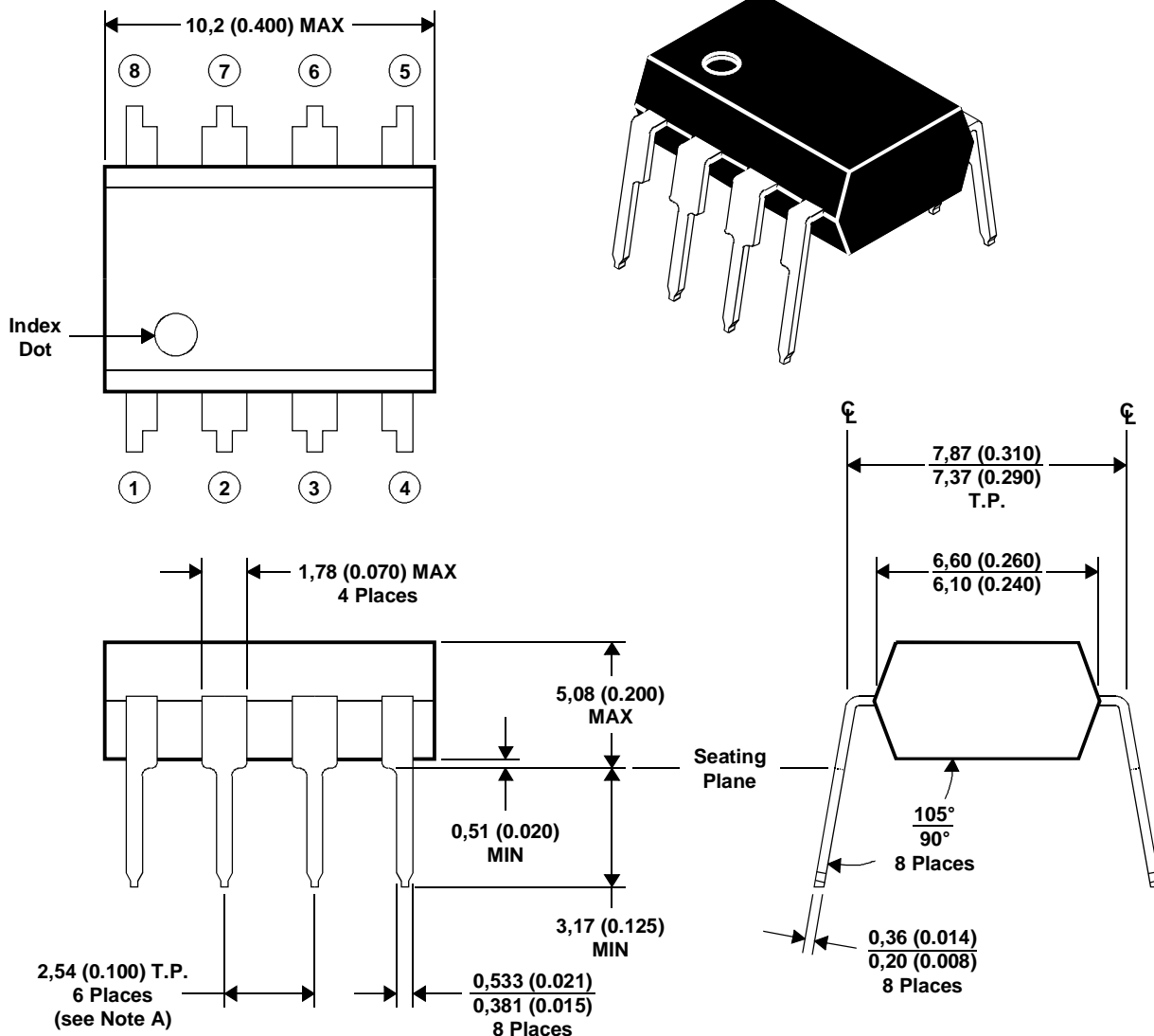
**P008**

**plastic dual-in-line package**

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centres. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

P008

Designation per JEDEC Std 30:  
PDIP-T8



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA



### **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1998, Texas Instruments Incorporated