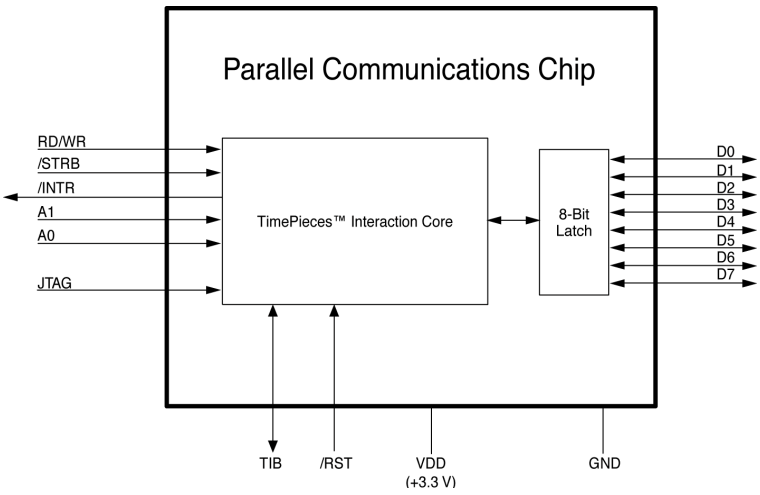
Parallel Communications Chip

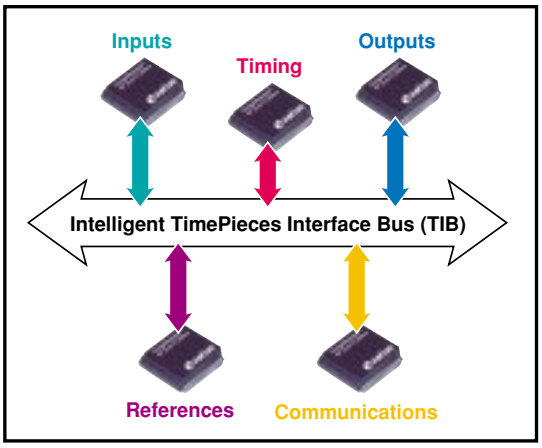
TimePieces™
CHIPSET SYNC SOLUTIONS

Ordering P/N: TP413179-000-0



Description

The Parallel Communications chip is an advanced management interface to communicate with a customer Host system. It's part of the patent-pending TimePieces (TP) product family. It's designed with an intelligent TIB (Timepieces Interface Bus), which enables a set of TP chips to be seamlessly interconnected, controlled and managed on distributed customer boards.



Features

- ✔ *Communications interface between a customer Host system and a TP system*
- ✔ *TIB-based management interface*
- ✔ *Configuration, fault and performance monitoring of a TP system by a customer Host system*
- ✔ *Scalable to design a clock system with other TimePieces chips*
- ✔ *Designed for GR-63 (NEBS) equipment*

Applications

- ✔ *Multiservice clock controller & interface*
- ✔ *Multiservice ATM/IP/SONET/SDH equipment*
- ✔ *Transport/Switch/Router equipment*
- ✔ *Core/Metro/Edge/Access network equipment*

Key Parallel Communications Technical Specifications	
Interface	
Customer Host system	8-bit memory mapped interface
Management Functionality	
Configuration	Customer Host system can configure a TP system
Monitoring	Customer Host system can monitor faults & performance of a TP system
Standards Compliance	Latest GR-253/378/1244, ANSI T1.102/403 ITU-T
Size	
Footprint	Standard 68-pin PLCC
Height	0.44" (11.176 mm)
Power Supply	
Input voltage (DC)	3.3 V (nominal)
Consumption	130 mA
Environmental	
Operating temperature	0 to 70° C
Storage temperature	-40° to 100° C
Humidity	0 to 95% (no condensation)

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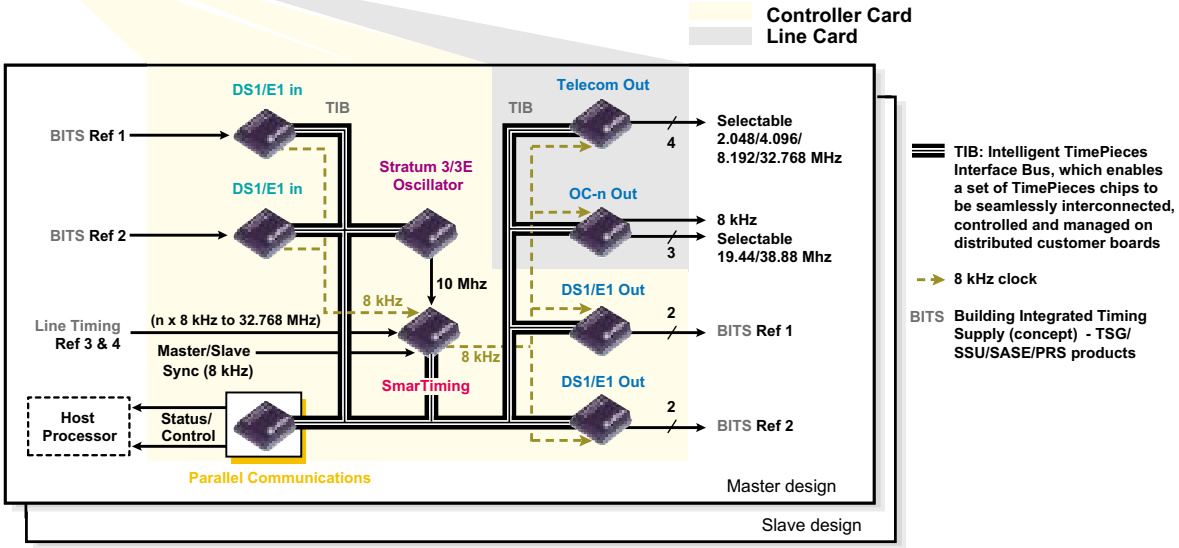
Typical Application

Clock Controllers & Line Card Timing Interfaces

Multiservice
network element



The above configuration provides a fully operating Clock system with default settings to meet the standards specifications defined in GR-378/1244/253, ANSI T1.101/102/105 series/403, ITU-T G.703/704/812/813/823/824/825 and ETSI ETS 300 462 series. Connection to the Host processor is not required unless changes to default settings or monitoring is required.

Key Clock System Features & Capabilities	
Input	
BITS (2x)	Selectable DS1/E1 (redundant) with SSM (Sync Status Message) data
Line timing (2x)	Selectable n x 8 kHz up to 32.768 MHz
Sync (1x)	8 kHz (Master/Slave protection mode for redundant design - 2 Clock/SmarTiming chips)
Auto selection/reverting	Locking/reverting to the best qualified input reference
Output	
BITS (4x)	Selectable DS1/E1 (redundant) with SSM data
Telecom (4x)	Selectable 2.048/4.096/8.192/32.768 MHz
OC-n (4x)	Selectable 1x 8 KHz and 3x 19.44/38.88 MHz
Clock Holdover	
Oscillator	Stratum 3 or 3E
Hitless Clock Switching	
Master/Slave clock switchover	Phase transient build-out during clock switchover
Jitter/Wander/Transient/Phase Filtering & Noise Transfer	See performance specifications of the SmarTiming chip
Real-Time Performance Monitoring	
Input	Up to 5 inputs, including Master/Slave Sync, settable or default priority selection
Reference qualification	Based on 1) frequency offsets; 2) stability offsets caused by jitter/wander (MTIE/TDEV thresholds); 3) DS1/E1 SSM; 4) telecom signal errors
Historical data	Frequency, phase, MTIE, TDEV data for performance and root-cause analysis
Retrieving Data	Through the TIB (TimePieces Interface Bus)
Communications/Management	
Parallel	8 bit memory mapped interface
TIB	TimePieces Interface Bus
Standards Compliance	
Equipment (TimePieces inside)	Latest GR-253/378/1244, ANSI T1.101/102/105/403, ITU-T G.703/704/812/813/823/824/825, ETSI ETS 300 462 series

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