TMC2301

Image Resampling Sequencer
15, 18, 20 MHz

Features

- Rotation, warping, panning, zooming, and compression of images in real time
- 20 MHz clock rate
- 4096 x 4096 image field addressing capability
- User-selectable nearest-neighbor, bilinear interpolation, and cubic convolution resampling algorithms
- Static convolutional filtering of up to 16 x 16 pixel windows
- Single-pass or two-pass convolution operations
- Low power consumption CMOS process
- Single 5V power supply
- Available in a 68-pin grid array and low-cost plastic leaded chip carrier (J-bend)

Applications

- Video special-effects generators
- Image recognition systems, robotics
- Artificial intelligence
- High-precision image registration (LANDSAT processing)
- High-speed data encoding/decoding
- General purpose image processing
- Image data compression

Description

The TMC2301 is a VLSI circuit which supports image resampling, rotation, rescaling and filtering by generating input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with external multiplier-accumulator control signals. The TMC2301 can process data fields of up to 4096 x 4096 multibit words at a clock rate of up to 20 MHz. An Image Resampling

Sequencer (IRS) based system can nearest-neighbor resample a 512 x 512 image in 15 milliseconds, translating, zooming, rotating, or warping it, depending on the transform parameter set loaded. A complete bilinear interpolation of the same image can be completed in 60 milliseconds. Image resampling speed is independent of the angle of rotation, degree of warp, or amount of zoom specified.
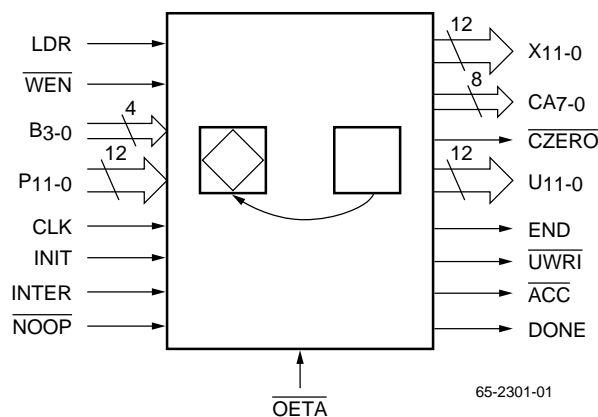
A high performance, TMC2301-based system can execute bilinear and cubic convolution algorithms that rotate images accurately and in real time. Keystone or other perspective correction, image plane distortion, and numerous other second order polynomial transformations can be programmed and executed under direct user control. Direct access to the interpolation coefficient lookup table allows dynamic modification of the algorithm.

Following an initialization with the transform parameters and control bits defining the operation to be executed, the IRS assumes control of the input and output data fields and executes unattended. All inputs except INTER and all outputs are registered on the rising edge of clock. All outputs are three-state controlled except $\overline{ACC}$, $\overline{CZERO}$, END, and DONE.

Fabricated in a 1 micron CMOS process, the TMC2301 operates at clock rates of up to 20 MHz over the full commercial (0 to 70°C) temperature and supply voltage ranges. All signals are TTL compatible.

Logic Symbol

65-2301-01

Block Diagram

65-2301-02
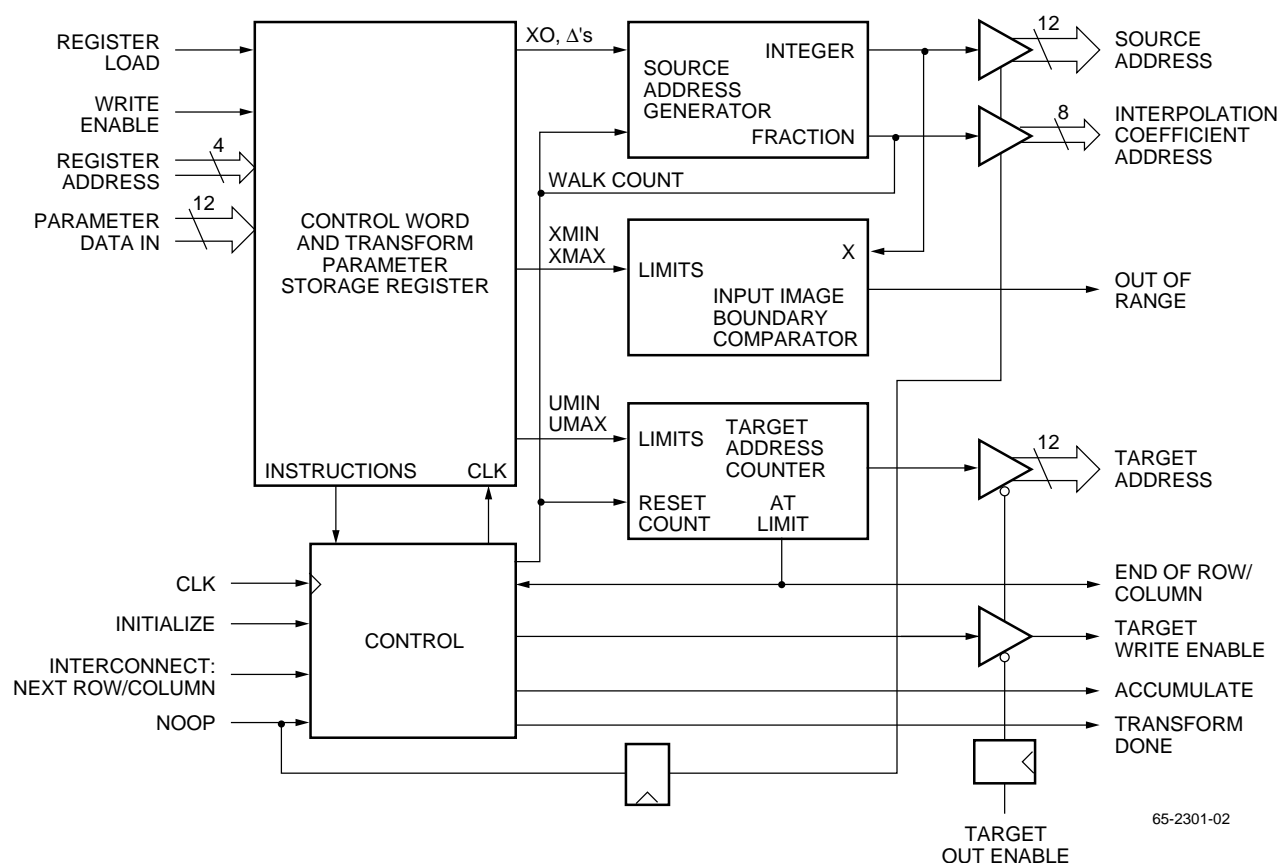
Functional Description

General Information

The IRS is a versatile self-sequencing address generator designed primarily to filter a two-dimensional image or to remap and resample it from one set of Cartesian coordinates (x, y) into a new transformed set (u, v). Most applications use two identical devices in tandem, one generating the row coordinates (X and U), the other generating the column coordinates (Y and V). The algorithm performed by the TMC2301 consists of two steps: a coordinate system transformation, followed by pixel interpolation. Interpolation is necessary when the transformed pixel positions (U, V) do not coincide with the original pixel positions (X, Y). The new pixel intensity values are obtained by interpolating the original pixels in the neighborhood of the transformed pixel positions. See Figure 1.

The IRS executes a general second order coordinate transformation of the form:

$$X(u, v) = Au^2 + Bu + Cuv + Dv^2 + Ev + F$$
$$Y(u, v) = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$$

where A through N are user-defined parameters. It steps sequentially through the pixels of a user-defined rectangle in the new set of coordinates, computing the "old" address (X, Y) corresponding to each "new" location (U, V).

The TMC2301 uses the external multiplier-accumulator, connected to the system clock, to calculate the interpolated pixel value by summing the products of the original pixel values stored in the source buffer RAM and the appropriate weights from the polynomial transform lookup table. The new interpolated image value is then stored in the corresponding (U, V) memory location. Finally, the new image address is incremented by one pixel in the "U" direction or reset to the start of the next line (with "V" incremented) proceeding line-by-line through the entire destination image.

The TMC2301 can support any nearest neighbor, bilinear, or cubic resampling, according to the user's requirements. The bilinear and cubic kernels require a coefficient lookup table and multiplier-accumulator. Both one-pass and two-pass algorithms are supported. Sophisticated "walkaround" algorithms implementing static filters are also easily realized utilizing convolutional kernels of up to 16 x 16 pixels. For each output point in a typical static single-pass filter, the IRS will generate a series of addresses, "walking" around that point in two dimensions. At the end of each walk, it will advance one pixel along the output scan line, then begin the walk for the next pixel.

Original (Source) Image   **New (Target) Image**
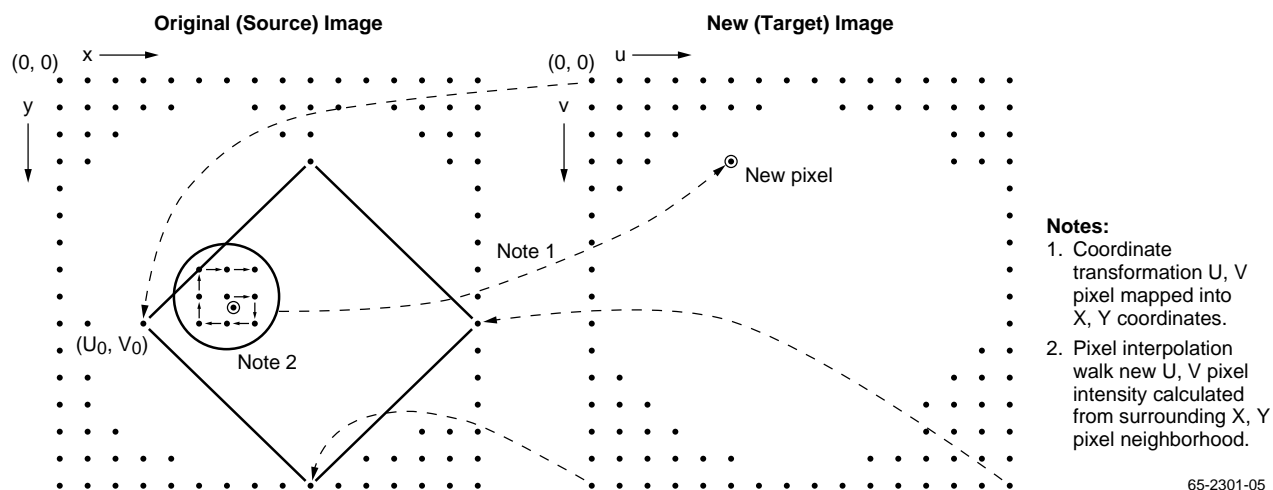
Figure 1. Image Resampling Geometry Showing Image Rotation and Expansion

A basic TMC2301-based system is shown in Figure 2. In this typical system, two Image Resampling Sequencers process the image. The only other external parts needed are a multiplier-accumulator, external interpolation coefficient lookup table RAM, and the user-specified Source and Destination Image Memory.
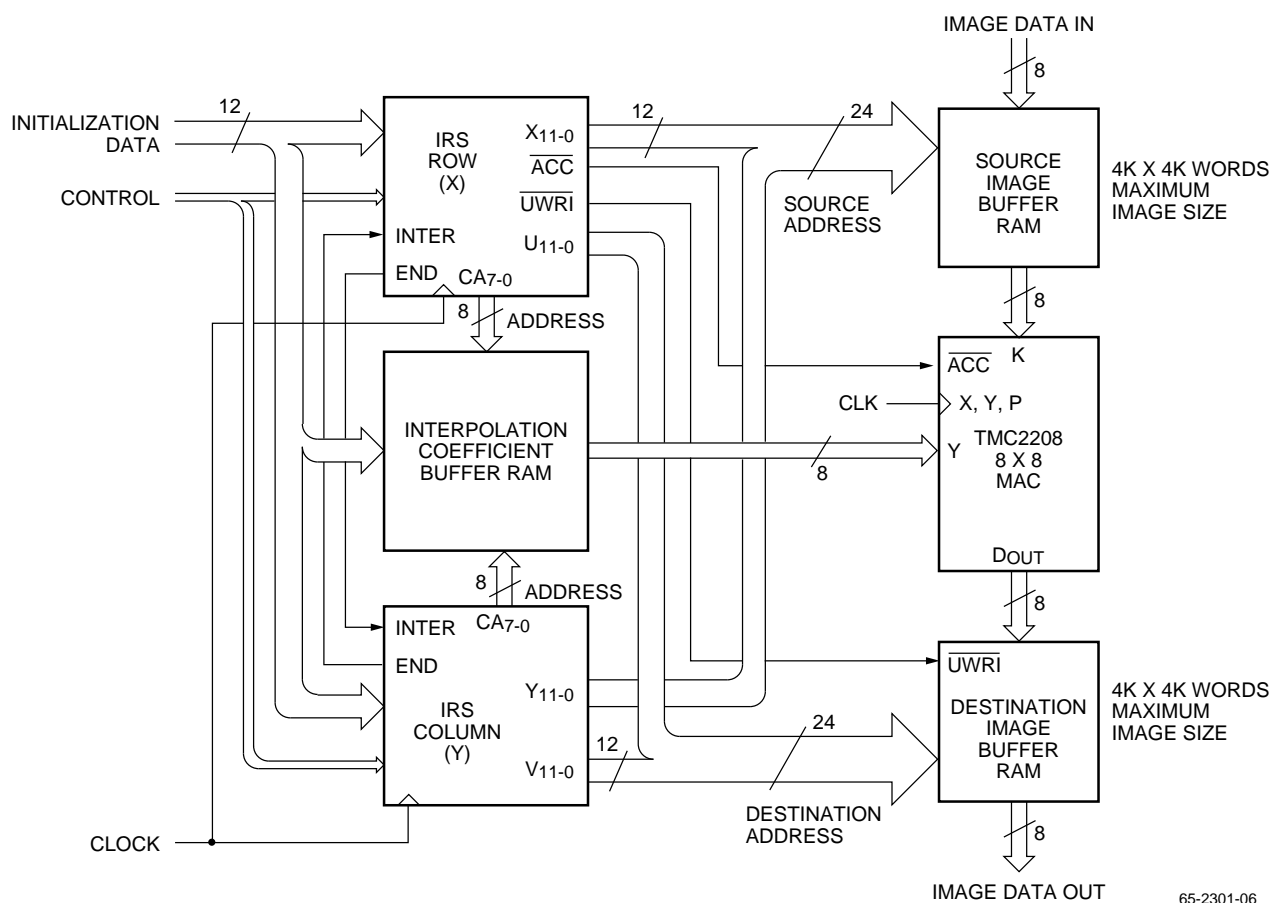
**Figure 2. Basic 2-D Image Convolver Using TMC2301 Image Resampling Sequencer
Utilizing Typical 8-Bit Data Path**

Pin Assignments

68 Pin Grid Array

65-2301-03

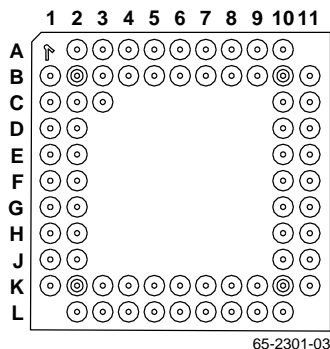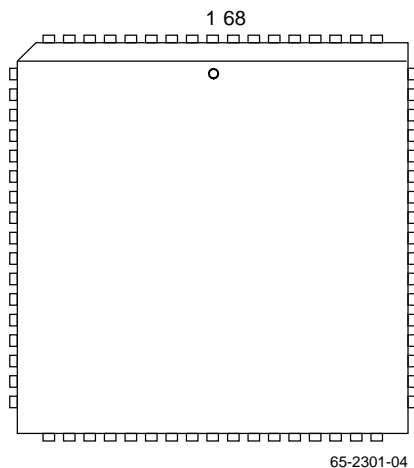| Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	$\overline{INIT}$	K2	U_{10}	K10	X_1	B10	P_6
B1	$\overline{OETA}$	L2	U_{11}	K11	X_2	A10	P_5
C2	INTER	K3	$\overline{UWRI}$	J10	X_3	B9	P_4
C1	END	L3	$\overline{ACC}$	J11	X_4	A9	P_3
D2	DONE	K4	$\overline{CZERO}$	H10	X_5	B8	P_2
D1	U_0	L4	CA_0	H11	X_6	A8	P_1
E2	U_1	K5	CA_1	G10	X_7	B7	P_0
E1	U_2	L5	V_{DD}	G11	X_8	A7	CLK
F2	GND	K6	GND	F10	GND	B6	GND
F1	U_3	L6	CA_2	F11	X_9	A6	V_{DD}
G2	U_4	K7	CA_3	E10	X_{10}	B5	$\overline{NOOP}$
G1	U_5	L7	CA_4	E11	X_{11}	A5	LDR
H2	U_6	K8	CA_5	D10	P_{11}	B4	B_0
H1	U_7	L8	CA_6	D11	P_{10}	A4	B_1
J2	U_8	K9	CA_7	C10	P_9	B3	B_2
J1	U_9	L9	X_0	C11	P_8	A3	B_3
K1	GND	L10	GND	B11	P_7	A2	$\overline{WEN}$

68 Pin PLCC

65-2301-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	GND	35	GND	52	GND
2	CA_2	19	X_9	36	V_{DD}	53	U_3
3	CA_3	20	X_{10}	37	$\overline{NOOP}$	54	U_4
4	CA_4	21	X_{11}	38	LDR	55	U_5
5	CA_5	22	P_{11}	39	B_0	56	U_6
6	CA_6	23	P_{10}	40	B_1	57	U_7
7	CA_7	24	P_9	41	B_2	58	U_8
8	X_0	25	P_8	42	B_3	59	U_9
9	GND	26	P_7	43	$\overline{WEN}$	60	GND
10	X_1	27	P_6	44	$\overline{INIT}$	61	U_{10}
11	X_2	28	P_5	45	$\overline{OETA}$	62	U_{11}
12	X_3	29	P_4	46	INTER	63	$\overline{UWRI}$
13	X_4	30	P_3	47	END	64	$\overline{ACC}$
14	X_5	31	P_2	48	DONE	65	$\overline{CZERO}$
15	X_6	32	P_1	49	U_0	66	CA_0
16	X_7	33	P_0	50	U_1	67	CA_1
17	X_8	34	CLK	51	U_2	68	V_{DD}

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	PGA	PLCC	
Power			
GND	F2, F10, K1, K6, L10, B6	1, 9, 18, 35, 52, 60	**Supply Voltage.** The TMC2301 operates from a single +5V supply. All pins must be connected.
V_{DD}	L5, A6	36, 68	**Ground.** The TMC2301 operates from a single +5V supply. All pins must be connected.
Clock			
CLK	A7	34	**System Clock.** The TMC2301 has a angle clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
Inputs			
B_{3-0}	A3, B3, A4, B4	42-39	**Parameter Register Address.** The write addresses for the individual coordinate transform parameters are presented at the registered 4-bit B input port. B_3 is the Most Significant Bit.
P_{11-0}	D10, D11, C10, C11, B11, B10, A10, B9, A9, B8, A8, B7	22-33	**Parameter Register Data.** The coordinate transformation parameters are loaded through the registered 12-bit P input port. P_{11} is the Most Significant Bit.
Outputs			
CA_{7-0}	K9, L8, K8, L7, K7, L6, K5, L4	7-2, 67, 66	**Coefficient Address.** The current interpolation kernel coefficient lookup table address is indicated by the registered 8-bit CA_{7-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. CA_7 is the Most Significant Bit.
U_{11-0}	L2, K2, J1, J2, H1, H2, G1, G2, F1, E1, E2, D1	62, 61, 59-53, 51-49	**Target Address.** The U (or V) target address of the image being generated is indicated by the registered 12-bit U_{11-0} output bus. This output is forced to the high impedance state when $\overline{OETA}$ is HIGH. U_{11} is the Most Significant Bit.
X_{11-0}	E11, E10, F11, G11, G10, H11, H10, J11, J10, K11, K10, L9	21-19, 17-10, 8	**Source Address.** The current X (or Y) source pixel address of the image being resampled is indicated by the registered 12-bit X_{11-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. X_{11} is the Most Significant Bit.
Controls			
$\overline{ACC}$	L3	64	**Accumulate.** The accumulation register of the external multiplier-accumulator is initialized by the registered $\overline{ACC}$ output. $\overline{ACC}$ goes LOW for one cycle at the start of each interpolation "walk," effectively clearing the storage register by loading in only the new first product. See Figure 9.
INIT	B2	44	**Initialize.** The control logic is cleared and initialized for the start of a new image transformation when the registered INIT input is HIGH for a minimum of two clock cycles. Normal operation begins after INIT goes LOW.
INTER	C2	46	**Interconnect.** In the common two-device system configuration, the Interconnect inputs are connected to the END flag outputs. The END flag from the row (X) sequencer thus indicates an "end of line" to the column (Y) device, while the column sequencer in turn sends a "bottom of frame" signal to the row device, forcing a reset of the address counter.

Pin Descriptions (continued)

	Pin Number		
Pin Name	**PGA**	**PLCC**	**Pin Function Description**
LDR	A5	38	**Load Parameter Data Registers.** The data held in all transformation parameter preload registers are latched into the working registers when the registered input LDR is HIGH. When LDR is LOW, the working parameters remain unchanged. See Figure 4.
$\overline{\text{NOOP}}$	B5	37	**No Operation.** The Clock is overridden when the registered input NOOP is LOW, holding each address generator in their current state. Also, the output buffers for the address busses X_{11-0} and CA_{7-0} are forced to the high impedance state. This allows the user access to all external memory. When $\overline{\text{NOOP}}$ goes HIGH, normal operation resumes on the next clock cycle.
$\overline{\text{OETA}}$	B1	45	**Target Memory Output Enable.** The target memory outputs $\overline{\text{UWRI}}$ and address bus U_{11-0} are in the high-impedance state when the registered Output Enable input is HIGH. When $\overline{\text{OETA}}$ is LOW, they are enabled on the next clock cycle.
$\overline{\text{UWRI}}$	K3	63	**Target Memory Write Enable.** After the end of each interpolation "walk," the Target Memory (U or V) Write Enable goes LOW for one clock cycle. See Figure 9. This registered output is forced to the high impedance state when $\overline{\text{OETA}}$ is HIGH.
$\overline{\text{WEN}}$	A2	43	**Parameter Write Enable.** The registered Write Enable input allows the transformation parameters to be written into the preload register indicated by the address at the B input port when LOW. See Figure 4.
Flags			
$\overline{\text{CZERO}}$	K4	65	**Coefficient Zero.** The registered $\overline{\text{CZERO}}$ flag of a horizontal dimension TMC2301 goes HIGH if $X < 0$, $XMIN \leq X \leq XMAX$, or $X \geq 4096$ (1000 hex). It goes LOW if $0 \leq X \leq XMIN$ or $XMAX < X < 4096$. The logical AND of the $\overline{\text{CZERO}}$ flags of a two-dimensional pair of TMC2301s will go LOW when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), denoting an invalid address. The external data path can be wired to substitute a selected background value whenever this AND = 0.
DONE	D2	48	**End of Transform.** In the standard two-device system, a row sequencer DONE flag HIGH after the last walk at the end of the last row of an image (during $\overline{\text{UWRI}}$ LOW) indicates the end of the transform. This registered output is usually ignored on the column device. See the Transformation Control Parameters, AUTOINIT.
END	C1	47	**End of Row/Page.** The registered END flag goes HIGH during the last pixel of the last walk in a row in the case of the row chip, and the last pixel of the last walk in a column in the column chip, in the two-device architecture. This output is used as the end-of-line and end-of-frame indicator in conjunction with the INTER inputs of both TMC2301s.

Transformation Control Parameters

The TMC2301 is a self-sequencing device which requires no cycle-to-cycle intervention from the host system. To program the device, the user loads the 16 operating parameters, which define the transformation to be performed, which sections of the original and resampled image spaces are to be utilized, and various control words. Filtering operations are further defined by the values the user loads into the external coefficient memory. The transform parameters are described below. See also Tables 1 through 3.

XMIN, XMAX, YMIN, YMAX	These four parameters outline the "source" rectangular region of the original image. Whenever the IRS pair generates an (X, Y) address within this boundary the $\overline{\text{CZERO}}$ flags will denote a valid memory read. In the most common case, XMIN < XMAX, YMIN < YMAX, 000h < X < FFFh, and 000h < Y< FFFh. In this case, addresses out of bounds cause one or both $\overline{\text{CZERO}}$s to go LOW. Refer to Application Note TP-38 for further information on other boundary violation cases. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.
UMIN, UMAX, VMIN, VMAX	These four parameters outline the "target" region of the (u, v) plane, into which the resampled image will be written. The IRS will generate, line by line, a scan that fills only this portion of the plane, permitting the user to assemble a mosaic of multiple rectangular subimages. Care must be taken to ensure that UMAX > UMIN and VMAX > VMIN. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.
(X_0, Y_0)	These are the coordinates of the first pixel to be read from the original image. In many applications, this point will be one of the four corners of the original image to be resampled. The pixels near (X_0, Y_0) in the original image will be used to compute the upper left pixel of the transformed image. In non-inverting, non-reversing applications (X_0, Y_0) will be the upper left corner of the original subimage. Each coordinate is expressed in 13-bit integer plus 5-bit fraction, two's complement notation.

dX/dU_0	Is the initial horizontal partial first derivative indicating the displacement along the X axis which corresponds to each one pixel movement along the U axis. Usually, $0 < dX/dU_0 < 1$ corresponds to magnification, whereas $dX/dU_0 > 1$ represents reduction and $dX/dU_0 < 0$ denotes reflection about a vertical axis. The first derivatives are expressed in 8-bit integer, 12-bit fraction two's complement notation.
dX/dV_0	Is the initial horizontal-vertical partial first derivative. It indicates the displacement along the X axis corresponding to each one pixel movement along the V axis. The coefficients dX/dV_0 and dX/dU_0 define image rotation and shear.
dY/dU_0	Is the initial vertical-horizontal partial first derivative. It indicates the displacement along the Y axis corresponding to each one pixel movement along the U axis.
dY/dV_0	Is the initial vertical partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel step along the V axis. Since dX/dV_0 and dY/dV_0 are separate parameters, vertical magnification and reflection need not match their horizontal counterparts.

Note:

1. For each incremental move along the U axis, the starting point of the new "walk around spiral" is indexed to the ENDING point of the previous walk around spiral, rather than to its center. Therefore, the terms dX/dU_0 and dY/dU_0 must be adjusted accordingly. Since each new line is referenced back to the previous line's initial spiral starting point, no similar dX/dV_0 or dY/dV_0 correction is needed.

d^2X/dU^2	Is the second order horizontal derivative. It indicates the rate of change of the horizontal-horizontal first derivative with each step along a line in the output image space. All six second-order derivatives are 4-bit integer, 20-bit fractional two's complement parameters.
d^2X/dV^2	Is the second order horizontal-vertical-vertical derivative. It indicates the rate of change of the horizontal-vertical first derivative with each step down a column in the output image space.

d^2Y/dU^2	Is the second order vertical-horizontal-horizontal derivative. It indicates the rate of change of the the vertical-horizontal first derivative with each step along a line of the output image space.
d^2Y/dV^2	Is the second order vertical derivative. It indicates the rate of change of the vertical-vertical first derivative with each step down a column of the output image space.
$d^2X/dUdV$	Is the mixed second order derivative indicating the rate of change of the first order horizontal derivative as one proceeds downwards through the output image space. This is also the rate of change of the first order horizontal-vertical derivative during horizontal sweeps in the output image space.
$d^2Y/dUdV$	Is the mixed second order derivative indicating the rate of change of the first order vertical derivative as one moves horizontally across the output space, or, equivalently, the rate of change of the first order vertical-horizontal derivative as one moves vertically in the output image space
Row/Column Select	Sets the mode to either Row (0) or Column (1) operation.
Mode	This 2-bit control word defines three unique instructions: | Code	Instruction
00, 01	single-pass operation
10	pass 1 of two-pass operation
11	pass 2 of two pass operation	

In single-pass operation, the device walks through the entire (k + 1) x (k + 1) kernel for each output pixel, where k is the value written into the Kernel section (see below) of the parameter register. Two-pass operation, which requires a dimensionally separable kernel, is executed first for a (k + 1) element kernel in one direction, then for a (k + 1) element kernel in the other direction. For kernel sizes exceeding 2 x 2, the two-pass algorithm is obviously beneficial, requiring 2n samples per output point instead of n x n. In this case, the intermediate image data stored in the destination image memory following the first pass is used as the source image data on the second pass. The user may design a system to

switch source and destination memory bank addresses in place, or could utilize a second TMC2301 pair in a pipelined architecture. This would require a third image buffer for the final destination image. Both devices of a system pair are usually set to the same mode.

Kernel	The effective kernel width (height) exceeds this 4-bit unsigned number by 1, thereby providing kernels of 1 x 1 to 16 x 16 source pixels per output, for either resampling or filtering. Simple static filters can be implemented with kernels of up to 16 x 16 pixels (Kernel = 15), while resampling interpolation kernels are limited to 4 x 4 pixels (Kernel = 3), due to the four bits of fractional X (or Y) address generated by the TMC2301. See the Applications Discussion. Again, both devices in a pair are generally initialized with equal Kernel values.
Field of View (FOV)	As the device walks through its kernel coefficients, each corresponding step in (x, y) space is normally one pixel length or height; this is a field of view of 1. However, the user can subsample the original space before filtering or resampling, by applying the coefficient kernel over a view field of up to 7 units. At a field of view of F, the pixels selected for each kernel operation are F pixels apart. This is useful in oversampled pictures, whose intensity changes only slowly from pixel to pixel.
Autoload (ALR)	When set to 1 (HIGH), the LDR control is automatically asserted when INIT is strobed, loading the coefficient set currently stored in the preload registers.
Autoinit (AIN)	At the end of an image, if the AIN bit is 1 (HIGH) the DONE flag goes HIGH for one clock cycle and a new transform begins. If 0 (LOW), $\overline{UWRI}$ and the DONE flag remain HIGH during the sequence until the user strobes the INIT control to begin a new image transformation.
Pipe (PIPE)	Adjusts the timing of the target memory write controls, to compensate for buffered source image RAM. If the PIPE bit is 1 (HIGH), outputs $\overline{ACC}$ and $\overline{UWRI}$ will be delayed one clock cycle relative to the generation of the target address (U or V). See Figure 9.

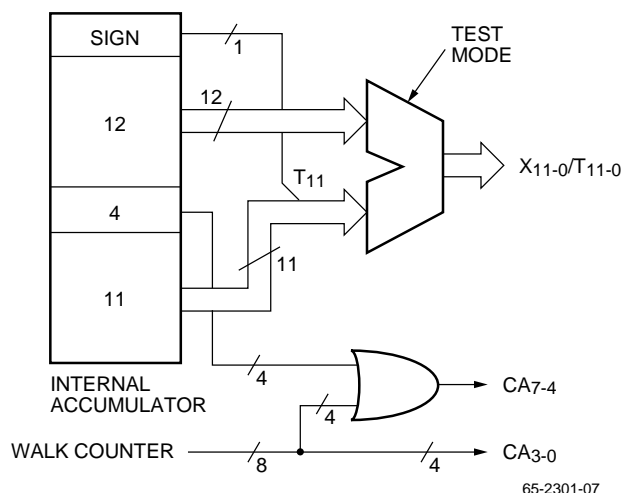|	
Test Mode (TM)	This mode is available for user inspection of the coefficient data. The source image and coefficient addresses are calculated by an internal 28-bit accumulator. When TM is 1 (HIGH), the sign bit, normally discarded, and the lower 11 bits of internal data are substituted for the upper 12 bits appearing at the source address port (X) during a standard transform cycle. This allows user verification of algorithm mathematics during debug. Since the TM bit is registered and cannot be changed during a single clock cycle, two distinct clock cycles are required to access both the MSW and LSW of the internal accumulator. See Figure 3.

Figure 3. Test Mode Data Routing

Table 1. Parameter Registers – Row Sequencer

Addr	Name	Description
0000	XMIN	Left side of Source Window
0001	XMAX	Right side of Source Window
0010	X_0 (LSW)	Source starting point – X coordinate
0011	X_0 (MSW)	Source starting point – X coordinate
0011	Controls	Mode Select Bits
0100	dX/dU_0 (LSW)	Row/Row first differential
0101	dX/dU_0 (MSW)	Row/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dX/dV_0 (LSW)	Row/Column first differential
0111	dX/dV_0 (MSW)	Row/Column first differential
0111	Kernel	Resampling/Filtering Kernel
1000	$d^2X/dUdV$ (LSW)	Mixed second differential
1001	$d^2X/dUdV$ (MSW)	Mixed second differential
1010	d^2X/dU^2 (LSW)	Row second differential
1011	d^2X/dU^2 (MSW)	Row second differential
1100	d^2X/dV^2 (LSW)	Row/Column second differential
1101	d^2X/dV^2 (MSW)	Row/Column second differential
1110	UMIN	Left edge of Final Image
1111	UMAX	Right edge of Final Image

Table 2. Parameter Registers – Column Sequencer

Addr	Name	Description
0000	YMIN	Top of Source Window
0001	YMAX	Bottom of Source Window
0010	Y_0 (LSW)	Source starting point – Y coordinate
0011	Y_0 (MSW)	Source starting point – Y coordinate
0011	Controls	Mode Select Bits
0100	dY/dU_0 (LSW)	Column/Row first differential
0101	dY/dU_0 (MSW)	Column/Row first differential
0101	TM, FOV	Test Mode, field of View
0110	dY/dV_0 (LSW)	Column/Column first differential
0111	dY/dV_0 (MSW)	Column/Column first differential
0111	Kernel	Resampling/Filtering Kernel Sure
1000	$d^2Y/dUdV$ (LSW)	Mixed second differential
1001	$d^2Y/dUdV$ (MSW)	Mixed second differential
1010	d^2Y/dU^2 (LSW)	Column/Row second differential
1011	d^2Y/dU^2 (MSW)	Column/Row second differential
1100	$d^2Y/dV2$ (LSW)	Column second differential
1101	d^2Y/dV^2 (MSW)	Column second differential
1110	VMIN	Top edge of Final Image
1111	VMAX	Bottom edge of Final Image

Table 3. Parameter Registers Binary Format (Row or Column Sequencer)

Address	Format												Limits	
	MSB											LSB	Dec	Hex
0000*	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
0001*	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
0010	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	$4096\text{-}2^{-5}$	0FFF.F8
0011							-2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	-4096	F000.00
0011 (Control)	ALR	AIN	PIPE	R/C	M_1	M_0								
0100	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128\text{-}2^{-12}$	007F.FFF
0101					-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	-128	FF80.000
0101* (TM, FOV)	TM	2^2	2^1	2^0										
0110	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128\text{-}2^{-12}$	007F.FFF
0111					-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	-128	FF80.000
0111* (Kernel)	2^3	2^2	2^1	2^0									15 0	f 0
1000	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8\text{-}2^{-20}$ -8	0007.FFFFF
1001	-2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}		
1010	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8\text{-}2^{-20}$ -8	0007.FFFFF
1011	-2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}		
1100	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8\text{-}2^{-20}$ -8	0007.FFFFF
1101	-2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}		
1110*	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FF 000
1111*	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FF 000

Notes:

1. * unsigned binary notation
2. A "–" indicates MSB is sign bit

Internal Bit Mapping (For parametric inputs, integers in table are bits of P, the input point)

	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
XOUT [11:0]		11	10	9	8	7	6	5	4	3	2	1	0				
CADN [7:4]														7	6	5	4
XMAX, XMIN		11	10	9	8	7	6	5	4	3	2	1	0				
XO	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1
DX/DU, DX/DV						7	6	5	4	3	2	1	0	11	10	9	8
$D^2X/DUDV$, D^2X/DU^2, D^2X/DV^2										11	10	9	8	7	6	5	4

	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}
XOUT [11:0]																
CADN [7:4]																
XMAX, XMIN																
XO	0															
DX/DU, DX/DV	7	6	5	4	3	2	1	0								
$D^2X/DUDV$, D^2X/DU^2, D^2X/DV^2	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0

Operation of the Transformation Parameter Registers

Numerous applications require the ability to update the coordinate transformation parameters "on the fly." Because the parameters are double-buffered, the user can load any or all of them into the preload registers without upsetting the operation in progress. Then LDR (load data registers) will update all transform parameters to the new values simultaneously. This feature is particularly valuable for "pin cushion" and "fish eye" transformations, or polar-to-rectangular conversions which cannot be performed with constant second derivatives. The Autoload function updates the preread registers at the beginning of a new image automatically. See the Transformation Control Parameters section. Note also that data can be loaded in to the registers while $\overline{NOOP}$ is active (LOW).
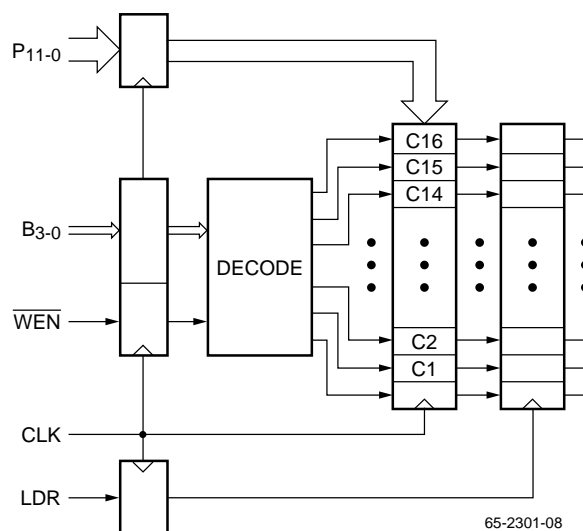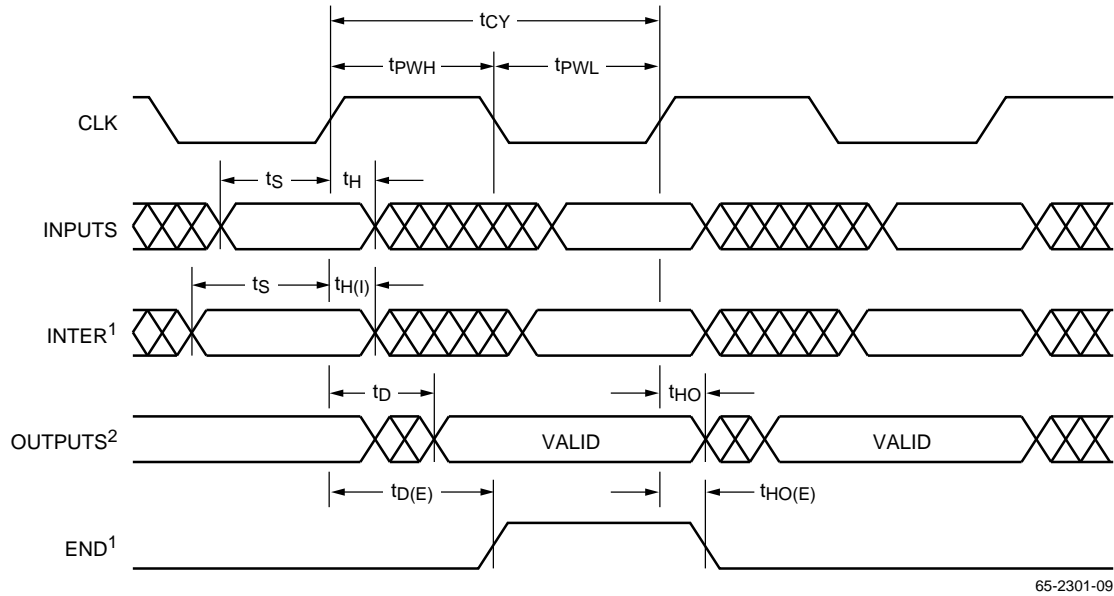
Figure 4. Operation of LDR Control for Parameter Update

65-2301-08

Timing Diagram

65-2301-09

Notes:
1. t_S and $t_{D(E)}$ are guaranteed to allow full speed operation in the standard two-device architecture. See text.
2. All outputs except END. See text.
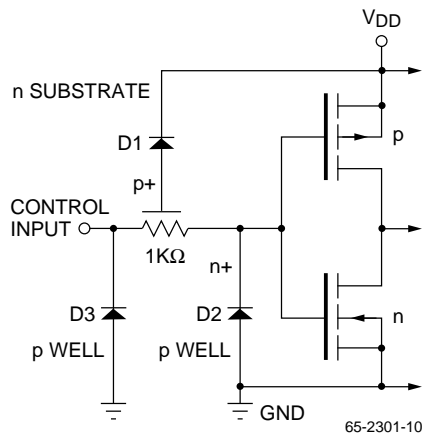
Equivalent Circuits and Transition Levels
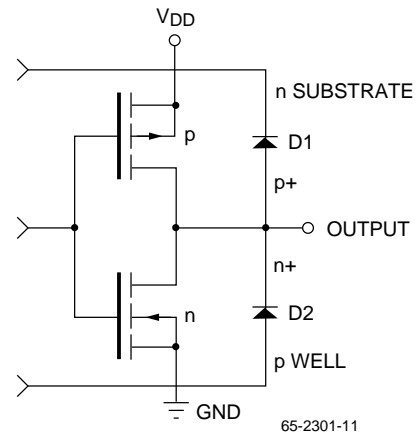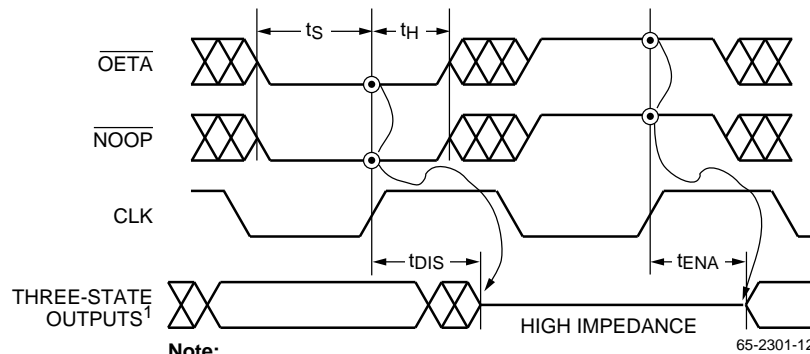

65-2301-10

Figure 5. Equivalent Input Circuit

65-2301-11

Figure 6. Equivalent Output Circuit

65-2301-12

Note:
1. All outputs except $\overline{CZERO}$, $\overline{ACC}$, END and DONE.

Figure 7. Transition Level for Three-State Output

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Output				
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-1.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Temperature				
Operating, Case	-60		130	°C
Operating, Junction			175	°C
Lead Soldering (10 seconds)			300	°C
Storage	-65		150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			8.0	mA
I_{OH}	Output Current, Logic HIGH			-4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
T_C	Case Temperature				°C

DC Characteristics   within specified operating conditions[1]

Parameter		Conditions	Min	Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 15MHz		75	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-10	10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Min, V_{IN} = V_{DD}	-10	10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Min, V_{IN} = 0V	-40	40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Min, V_{IN} = V_{DD}	-40	40	μA
I_{OS}	Short-Circuit Output Current[2]	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Guaranteed but not tested.

AC Characteristics   within specified operating conditions

Parameter		Conditions	-2		-1				Unit
			Min	Max	Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{DD} = Min	50		55		66		ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	20		22		25		ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	25		28		33		ns
t_S	Input Setup Time[1]		15		18		20		ns
t_H	Input Hold Time		1		2		2		ns
$t_{H(I)}$	Input Hold Time, INTER		8		10		10		ns
t_D	Output Delay[2]	V_{DD} = Min, C_{LOAD} = 40pF		25		27		35	ns
$t_{D(E)}$	Output Delay, END[1]	V_{DD} = Min, C_{LOAD} = 10pF		35		37		45	ns
t_{HO}	Output Hold Time[2]	V_{DD} = Max, C_{LOAD} = 40pF	5		5		5		ns
$t_{HO(E)}$	Output Hold Time, END	V_{DD} = Max, C_{LOAD} = 10pF	10		10		10		ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		25		27		35	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF	25		27		35		ns

Notes:
1. $t_S + t_{D(E)}$ = t_{CY} max.
2. Excluding output pin END.

Applications Discussion

Basic Operation

Each TMC2301 pair contains address controllers which execute patterns much like the following FORTRAN 3-level nested DO loop:

1. The inner loop is a clockwise outgoing spiral "walk" through the N-element coefficient kernel.

2. The middle loop is a left-to-right "scan" along each row of the output image space.

3. Finally, the outer loop is a top-to-bottom "scan" down each column of the output image space.

A typical one pass image transformation proceeds as follows:

1. The device pair outputs the addresses (X_0, Y_0), which is the first point in the source image, and (CAX, CAY), the interpolation lookup table address for the first pixel in the kernel. The output $\overline{ACC}$ goes LOW, causing the external accumulator to load the first product without summation, clearing the accumulator.

2. For the next N cycles, the IRS walks through an outward clockwise spiral in (x, y) space, accumulating pixel-interpolation coefficient products. The spiral sequence is depicted in Figure 8.

3. After the completion of the first spiral walk, the IRS outputs the target address of the first pixel, (UMIN, VMIN) and the control $\overline{UWRI}$, along with the initial (X, Y) values of the next spiral walk. $\overline{ACC}$ and $\overline{UWRI}$ can be delayed by one clock cycle by setting the control bit PIPE to 1 (HIGH) simplifying the task of interfacing the TMC2301 to buffered source image memory.

4. After the last cycle of the next spiral, $\overline{UWRI}$ again goes LOW for one clock, and the target address outputs are updated, pointing to the location of the pixel calculation just completed, (UMIN + 1, VMIN).

5. The third spiral walk begins with $\overline{ACC}$ going LOW, and ends with (UMIN + 2, VMIN) output and UWRI going LOW.
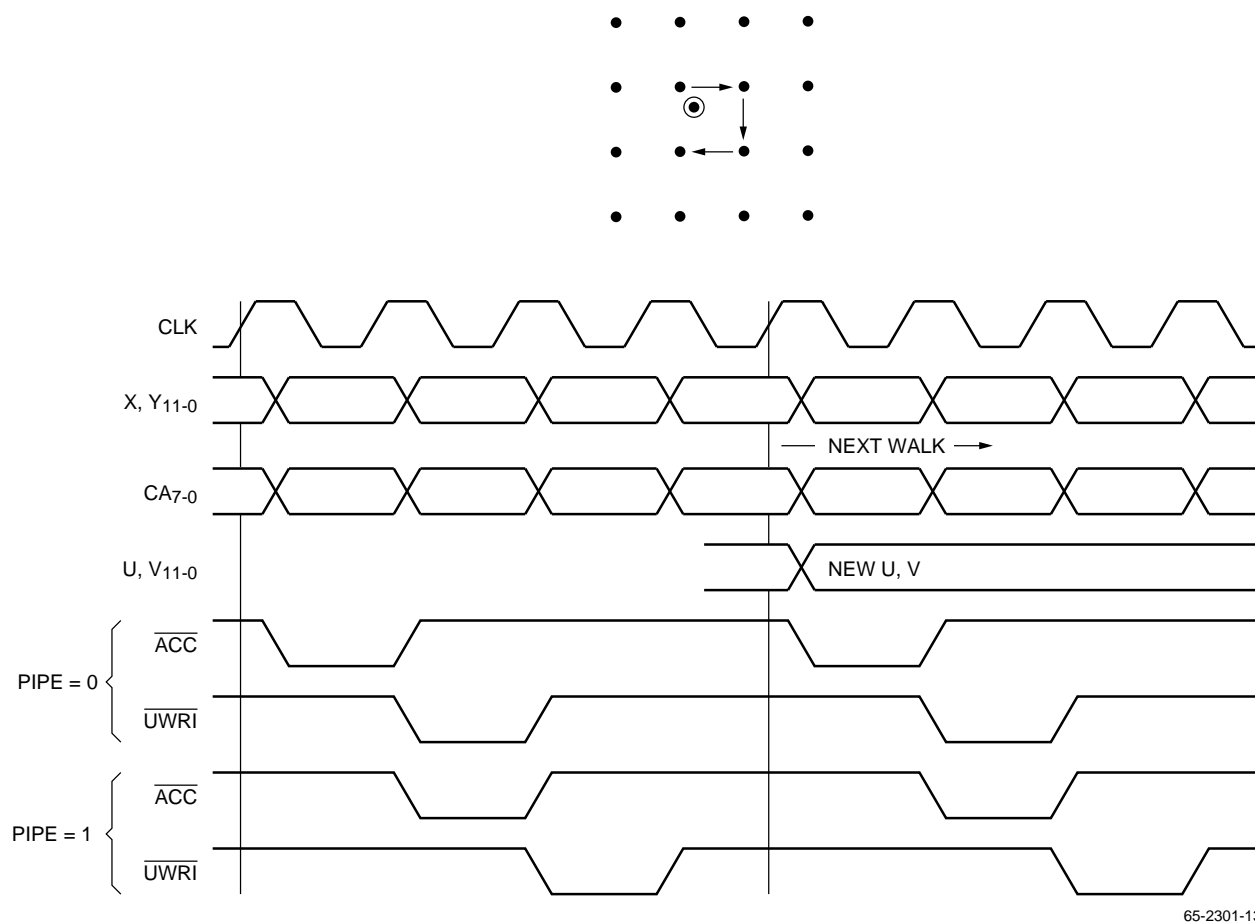
Notes:
1. Assumes that $\overline{OETA}$ is LOW and $\overline{NOOP}$ is HIGH.
2. Timing parameters are not shown on this diagram.

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Figure 8. Timing Diagram and Pixel Map Showing Outward Clockwise Spiral Walk Generated by TMC2301 (2x2 Kernel Shown)

6. The procedure continues until (UMAX + 1, VMIN) is reached, at which point the device resets to U (position within row) and increments V (number of row). Thus, the next (U, V) set after (UMAX + 1, VMIN) will be (UMIN, VMIN + 1), followed by (UMIN + 1, VMIN + 1), etc.

7. Upon completion of the walk corresponding to (UMAX + 1, VMAX + 1), the TMC2301 will generate a DONE flag with the final $\overline{UWRI}$, and begin a new sequence.

On any given clock cycle, the actual (X, Y) and (U, V) outputs of the IRS are given by the following equations:

$$x = X_0 + dX/dU_0 * m + dX/dV_0 * n + d^2X/dUdV * m * n$$
$$+ d^2X/dU^2 * (m2 - m)/2 + d^2X/dV^2 * (n^2 - n)/2$$
$$+ FOV * CAX(w) + FOV * m * CAX(Ker)$$

$$y = Y_0 + dY/dU_0 * m + dX/dV_0 * n + d^2Y/dUdV * m * n$$
$$+ d^2Y/dU^2 * (m2 - m)/2 + d^2Y/dV^2 * (n^2 - n)/2$$
$$+ FOV * CAY(w) + FOV * m * CAY(Ker)$$

$$u = UMIN + m$$

$$v = VMIN + n$$

where FOV is the 4-bit field of view parameter, normally set to 1 so that the spiral walk proceeds in single-pixel steps. Setting FOV to 4 would expand the spiral walk, allowing the user to trade two bits of image size for two bits of additional interpixel positioning resolution. CAX(w) and CAY(w) are the current value of the coefficient address outputs and CAX(KER) and CAY(KER) are the terminal values of each pixel walk. The CA(KER) terms arise because the IRS computes each new walk's starting paint from the previous spiral walk's end point rather than its starting point.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation values used to calculate the value of the new pixel. These values are selected by the user allowing maximum filtering flexibility. In simple filtering applications, all 8 bits of coefficient address are available to access up to 256 interpolation coefficients, for kernels of 16 x 16 pixels. This address is generated by the internal walk counter of the TMC2301. In most applications, the same Kernel parameter value is selected in both IRS devices; thus, the Coefficient Address outputs CA_{7-0} for the X and Y devices are identical, and the user needs only one of the 8-bit buses for memory access.

Applications executing a coordinate transformation, however will almost always generate non-integer source pixel addresses; that is the U (or V) locations will not map to the X (or Y) addresses exactly and fractional address components

are generated. The user then must account for this spatial offset in both dimensions by storing the appropriate corrected interpolation kernel values in the lookup table. The 8-bit address bus is broken up into two parts: the fractional portion (upper 4 bits), and the walk counter (lower 4 bits). Thus, in resampling applications, the maximum kernel size is 4 x 4 pixels, or 16 locations. As in the filtering example, assuming that the user has selected the same kernel size for both IRS devices, the 4 bits of least-significant address generated by both devices will be identical and redundant. The four most significant address bits, however, will reflect the current fractional offsets of the resampled pixel from the nearest X (Y) location, to a spatial resolution of 4 bits in the X (or Y) directions. Utilization of the 12 bits (total) of lookup table address is left to the user to be arranged as desired for memory access. See Figure 3.

Application Examples

One of the more common applications for the TMC2301 is simple static filtering In this case the source and target memories locations are identical and no coordinate transformation is performed. The (X, Y) and (U, V) outputs listed in Table 4 show the address sequencing generated by the TMC2301 to execute the walk of a 5 x 5 pixel interpolation kernel. The normalized coefficients shown implement a first-order Butterworth Low Pass Filter with cutoff radius of $1/\sqrt{2}$. Note that the (U, V) output address is updated following the completion of the walk for that location.
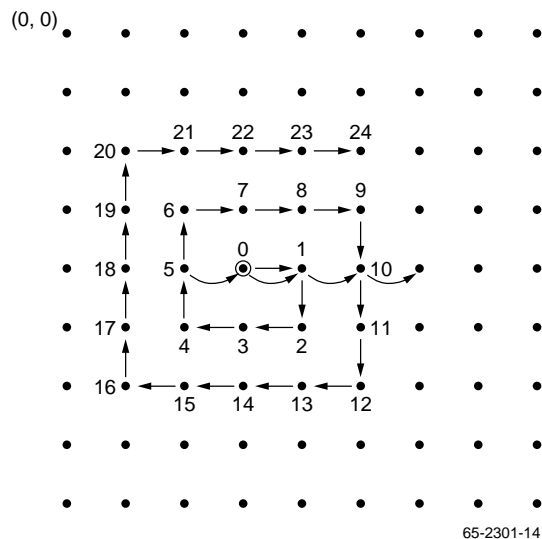

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Figure 9. Pixel Map Showing Walk Sequence for 5x5 Static Filter

Table 4. IRS Outputs for Static Filter Illustrated in Figure 10

| Cycle	X	Y	Index (CA)	Coefficient	U	V
1	3	4	0	0.2176	2	4
2	4	4	1	0.0725	2	4
3	4	5	2	0.0435	2	4
4	3	5	3	0.0725	2	4
5	2	5	4	0.0435	2	4
6	2	4	5	0.0725	2	4
7	2	3	6	0.0435	2	4
3	3	3	7	0.0725	2	4
9	4	3	8	0.0435	2	4
10	5	3	9	0.0198	2	4
11	5	4	10	0.0272	2	4
12	5	5	11	0.0198	2	4
13	5	6	12	0.0128	2	4
14	4	6	13	0.0198	2	4
15	3	6	14	0.0272	2	4
16	2	6	15	0.0198	2	4
17	1	6	16	0.0128	2	4
18	1	5	17	0.0198	2	4
19	1	4	18	0.0272	2	4
20	1	3	19	0.0198	2	4
21	2	2	20	0.0128	2	4
22	3	2	21	0.0198	2	4
23	4	2	22	0.0272	2	4
24	5	2	23	0.0198	2	4
25	4	2	24	0.0128	2	4
26		4	0	0.2175	3	4

Figure 10 illustrates the sequence for a bilinear resampling of a 63° rotation. The starting point is translated +1 in the Y-direction. A common rotation matrix might be:

$$dX/dU_0 = \cos(a) = .6 \qquad dY/dU_0 = \sin(a) = .8$$
$$dX/dV_0 = -\sin(a) = -.8 \qquad dY/dV_0 = \cos(a) = .6$$

However, we have included a linear compression factor of 5:1, and must accommodate the fact that each time u is incremented, the start of the new walk is referenced to the END of the previous walk. Given these corrections, the rotation matrix becomes:

$$dX/dU_0 = 5\cos(a) = 3 \qquad dY/dU_0 = 5\sin(a) - FOV = 3$$
$$dX/dV_0 = 5\sin(a) = -4 \qquad dY/dV_0 = 5\cos(a) = 3$$
$$Kernel = 1$$
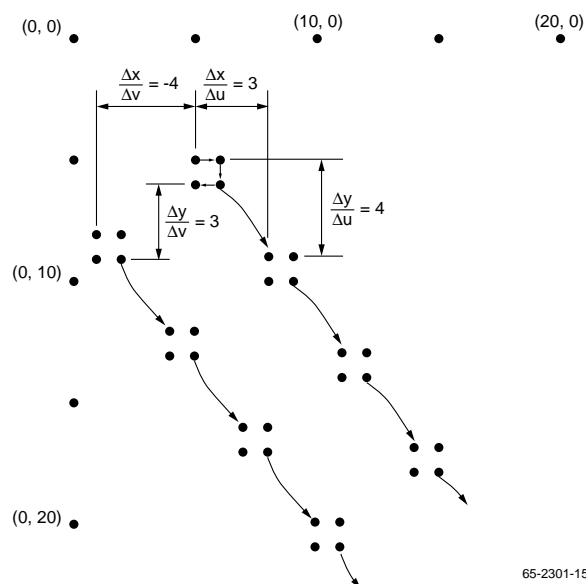
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Figure 10. Pixel Map Showing parameters for 63° Rotation and 5:1 Compression Listed in Table 5

Table 5. IRS Outputs for Operation Illustrated in Figure 11

Cycle	X	Y	Index	U	V
1	5	5	0	4	5
2	6	5	1	4	5
3	6	6	2	4	5
4	5	6	3	4	5
5	8	9	0	5	5
6	9	9	1	5	5
7	9	10	2	5	5
8	8	10	3	5	5
9	11	13	0	6	5
10	12	13	1	6	5
11	12	14	2	6	5
12	11	14	3	6	5
13	14	17	0	7	5
14	15	17	1	7	5
15	15	18	2	7	5
16	14	18	3	7	5
17	1	8	0	8	5
18	2	8	1	8	5
19	2	9	2	8	5
20	1	9	3	8	5
21	4	12	0	5	6
22	5	12	1	5	6
23	5	13	2	5	6
24	4	13	3	5	6
25	7	16	0	6	6
26	8	16	1	6	6
27	8	17	2	6	6
28	7	17	3	6	6
29	10	20	0	7	6
30	11	20	1	7	6
31	11	21	2	7	6
32	10	21	3	7	6
33	0	5	0	8	6

Figure 11 may help clarify the relationships among (X_0, Y_0), (XMIN, YMIN), (XMAX, YMAX), (UMIN, VMIN), and (UMAX, VMAX). With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the transformed image is located at (UMAX + 1, VMAX + 1); the location of the corresponding corner of the original image depends on the values of the derivatives. Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. This feature permits one to construct a mosaic of several abutting subimages in the (x, y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper right and lower right corners of the resampled image lie outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums.
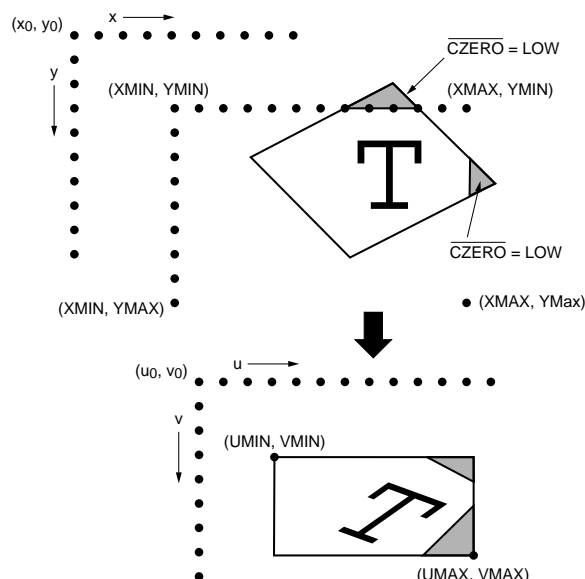
Note: Assume 000h < X < FFFh, 000h < Y < FFFh   65-2301-15

Figure 11. Pixel Maps Demonstrating Source and Destination Image Boundaries and Image Clipping (Note Shaded Area)

Application Note

Nearest Neighbor Operation—Additional Timing Details

Example A, PIPE = 0
Inspecting Figure 13:
PIPE = 0, KER = 0 (near neighbor), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX = 5,
DX/DU = 1, DY/DV = 1, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Table entries are events after listed clock rising edge.
END, DONE flags = 0, except where shown as 1.
UWRI goes low and remains low with CLK #2.

				END			
CLK	X	U	V	R	C	DON	Comments
0			0	0			First clock after INIT falling edge
1			0	0			
2	0		0	0			First valid X addresses = XO
3	1	0	0	0	0		Second X; first valid U, V = UMN, VMN
4	2	1	0	0	0		
5	3	2	0	1	0		END ROW flag 3 cycles before last X
6	4	3	0	0	0		
7	5	4	0	0	0		
8	6	5	0	0	0		Last X of first row
9	0	6	0	0	0		Last U, V or first row; first X of 2nd row
10	1	0	1	0	0		First U, V of second row
11	2	1	1	0	0		
12	3	2	1	1	0		END ROW flag 4 cycles before last U, V
13	4	3	1	0	0		
14	5	4	1	0	0		
15	6	5	1	0	0		Last X of second row
16	0	6	1	0	0		Last U, V of second row U = UMX + 1
35	5	4	4	0	1		END COL goes high before last X
36	6	5	4	0	1		Last X of V = VMX –1 row
37	0	6	4	0	1		First X of Last (V = VMX) row
38	1	0	5	0	1		First U, V = UMN, VMX of last now
39	2	1	5	0	1		
40	3	2	5	1	1		Last END ROW flag of frame
41	4	3	5	0	1		END COL goes low when DONE goes high
42	5	4	5	0	0	1	DONE immediately before last X
43	6	5	5	0	0		Last X of frame
44	0	6	5	0	0		Last U, V = UMX + 1, VMX
45	1	0	0	0	0		First U, V = UMN, VMN of new frame
46	2	1	0	0	0		
47	3	2	0	1	0		First END ROW flag of new frame

Example B, PIPE = 1
Now, referring to Figure 14:
PIPE = 1, KER = 0 (near neighbor), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX=5,
DX/DU = 1, DY/DV = 1, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Table entries are events after listed clock rising edges.
END, DONE, flags = 0, except where shown as 1.
UWRI goes low with CLK #3, stays low. Otherwise, the timing is the same as Figure 13, i.e., pipeline delays UWRI and ACC by one clock cycle.

Bilinear Interpolation

Example C, PIPE = 0
From Figure 15, we can see the following:
PIPE = 0, KER = 1 (bilinear), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX=5,
DX/DU = 1, DY/DV = 1, YO = 0, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Table entries are events after listed clock rising edges.
END, DONE flags = 0, except where shown as 1.

				END				
CLK	X	U	V	ROW	UWR	ACC	DON	Comments
0					1	0		1st CLK after INIT falling edge
1					0	0		
2	0				1	0		1st valid X address = XO: start 1st ACCum
3	1				0	1		
4	1				1	1		
5	0				1	1		End 1st 2x2 kernel; end 1st ACCum
6	1	0	0		1	0		1st valid u, v = UMN, VMN; 2nd ACCum start
7	2	0	0		0	1		
8	2	0	0		1	1		
9	1	0	0		1	1		
10	2	1	0		1	0		2nd valid u, v = UMN + 1, VMN
11	3	1	0		0	1		
12	3	1	0		1	1		
13	2	1	0		1	1		
14	3	2	0		1	0		3rd valid u, v = UMN + 2, VMN
15	4	2	0		0	1		
16	4	2	0		1	1		
17	3	2	0		1	1		End 4th 2x2 kernel
160	5	3	5	1	1	1		
161	4	3	5	1	1	1		
162	5	4	5	1	1	0		Begin next-to-last x-walk
163	6	5	4	1	0	1		
164	6	5	4		1	1		

CLK	X	U	V	END ROW	UWR	ACC	DON	Comments
165	5	4	5		1	1		
166	6	5	5		1	0		Begin last x-walk
167	7	5	5		0	1		
168	7	5	5		1	1	1	
169	6	5	5		1	1		Last x of frame
170	0	6	5		1	0		
171	1	6	5		0	1		
172	1	6	5		1	1		
173	0	6	5		1	1		Last u, v = UMX + 1, VMX
174	1	0	0		1	0		First u, v of new frame
175	2	0	0		0	1		
176	2	0	0		1	1		
177	1	0	0		1	1		

Performing Larger Interpolation Kernels

With PIPE = 0, AUTOINIT = 1, and the following definitions:

T_{xdone} = Clock cycle of final X address of a transform.
T_{xend} = Clock cycle of final X address along a row.
KER = (K + 1)(K + 1), where K is the value in the "kernel size" parameter register.

The following relationships hold true:

First X address   valid 3 rising clock edges after INlTs failing edge.

END FLAG   goes HIGH for KER cycles at clock cycle $T_{xend} - 1 - 2*KER$. Otherwise stated, END is active for one walkaround starting two walkarounds and one cycle prior to the final source address of a row.

DONE FLAG   goes HIGH for one cycle at clock cycle $T_{xdone} - 1$. Otherwise stated, DONE is active for one clock cycle one cycle prior to the last source address of the final walkaround.

Example D, KER = 0 (nearest neighbor), UMIN = 0, UMAX = 3, UMIN = 0, VMAX = 2
If first CLOCK edge after INIT goes low is 0, then:
First x, y out (= XO, YO) appears after CLOCK edge 2.
First u, v out (= 0, 0) appears after CLOCK edge 3.
END is high after CLOCK edge 13 only.
DONE is high after CLOCK edge 16.
Last x out appears after CLOCK edge 16.
Last u, v out (= 4, 2) appears after CLOCK edge 17.

Example E, KER = 1, (1 pass bilinear), UMIN = 0, UMAX = 4, VMIN = 1, VMAX = 3
If first CLOCK edge after INIT goes low is 0, then:
First x, y out (= XO, YO) appears after CLOCK edge 2.
First u, v out (= 0, 1) appears after CLOCK edge 6 and remains through edges 7, 8 and 9.
END is high after CLOCK edge 92, goes low after 96.
DONE is high after CLOCK edge 100 only.
Last x out appears CLOCK edge 101.
Last u, v out (= 5, 3) appears after CLOCK edge 102 and remains through edges 103, 104 and 105.
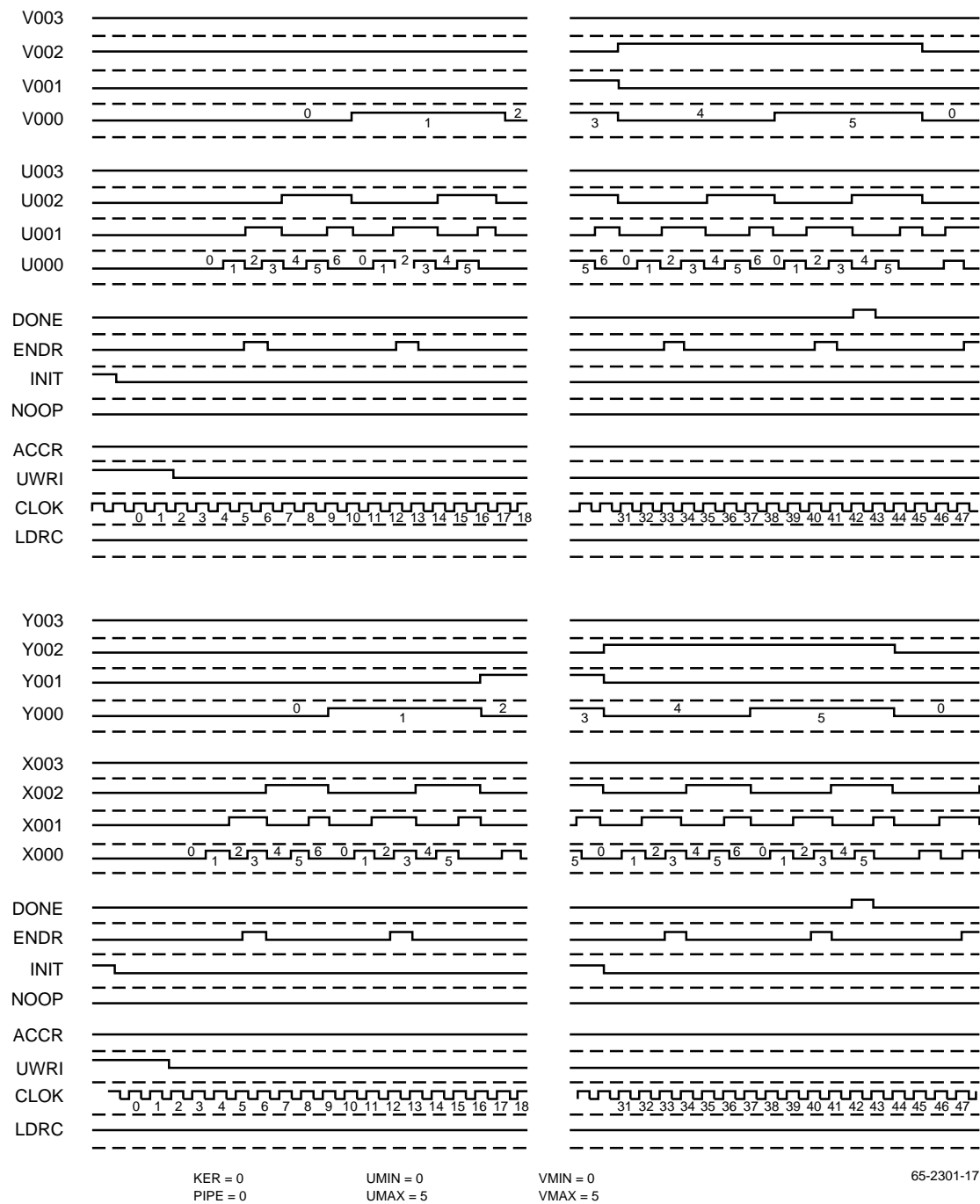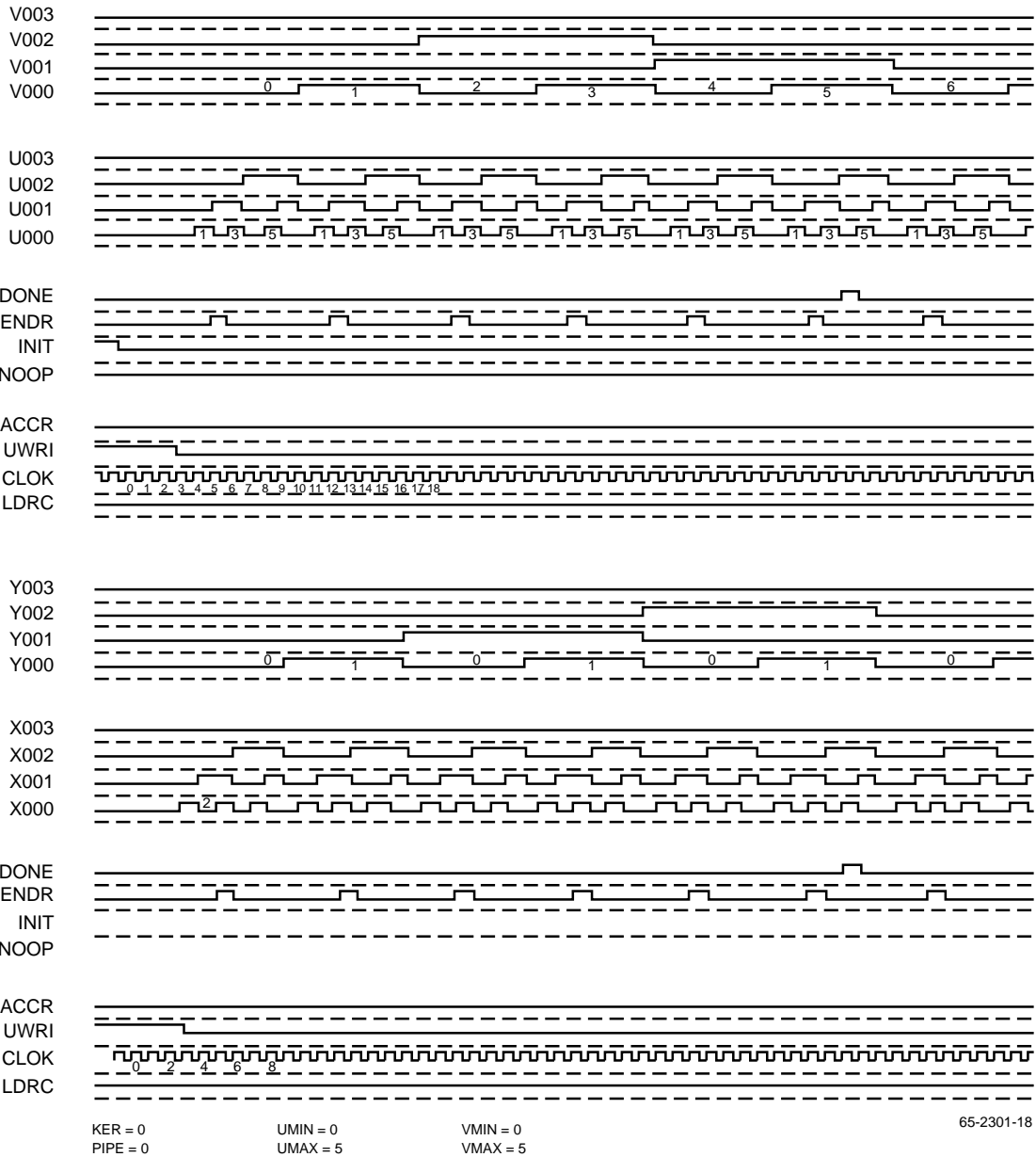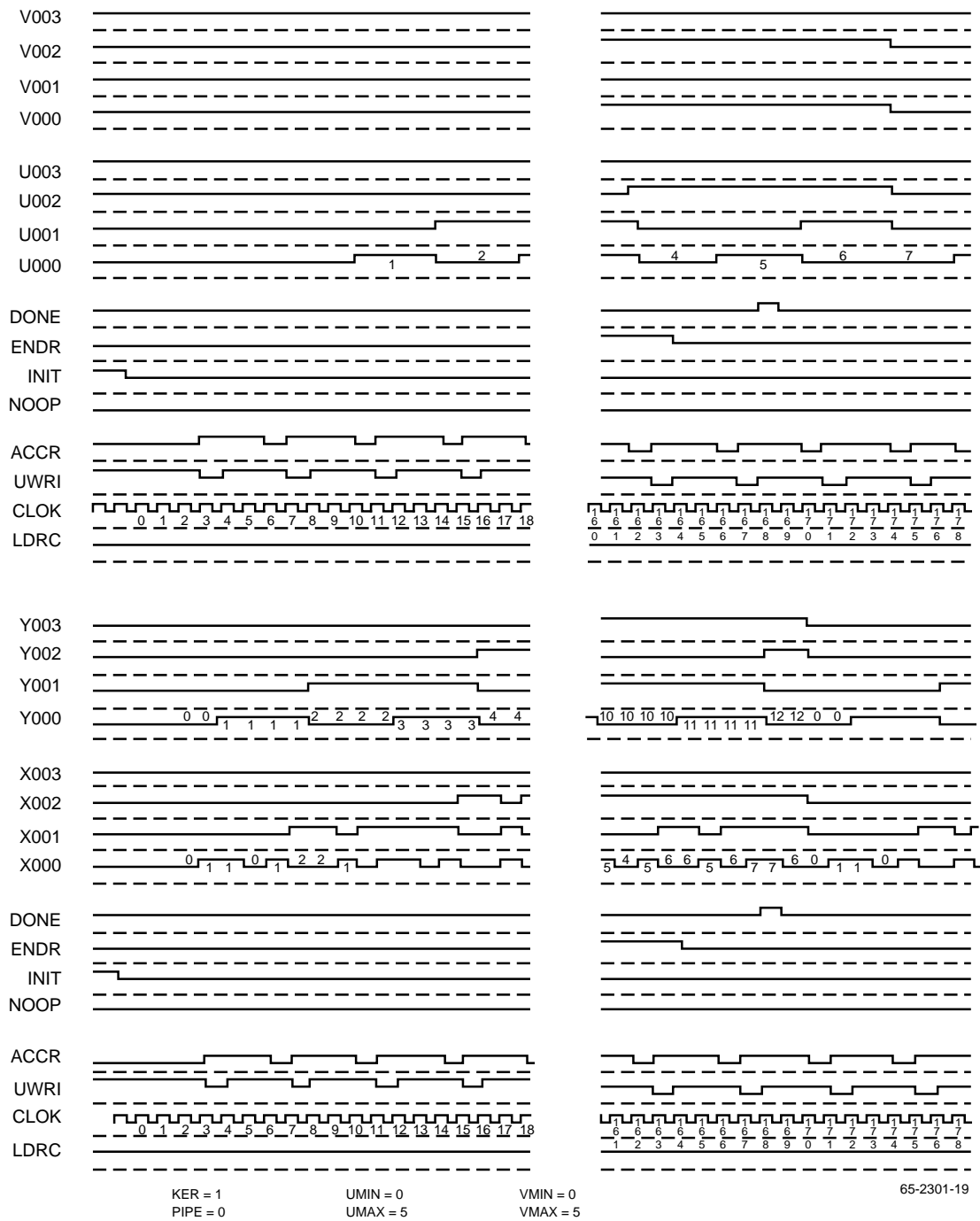
Figure 12.

KER = 0   UMIN = 0   VMIN = 0   65-2301-17
PIPE = 0   UMAX = 5   VMAX = 5

Figure 13.

Figure 14

Mechanical Dimensions

68 Lead Pin Grid Array

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.040	.060	1.02	1.52	
A2	.115	.190	2.92	4.83	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.
5. Optional index pin.
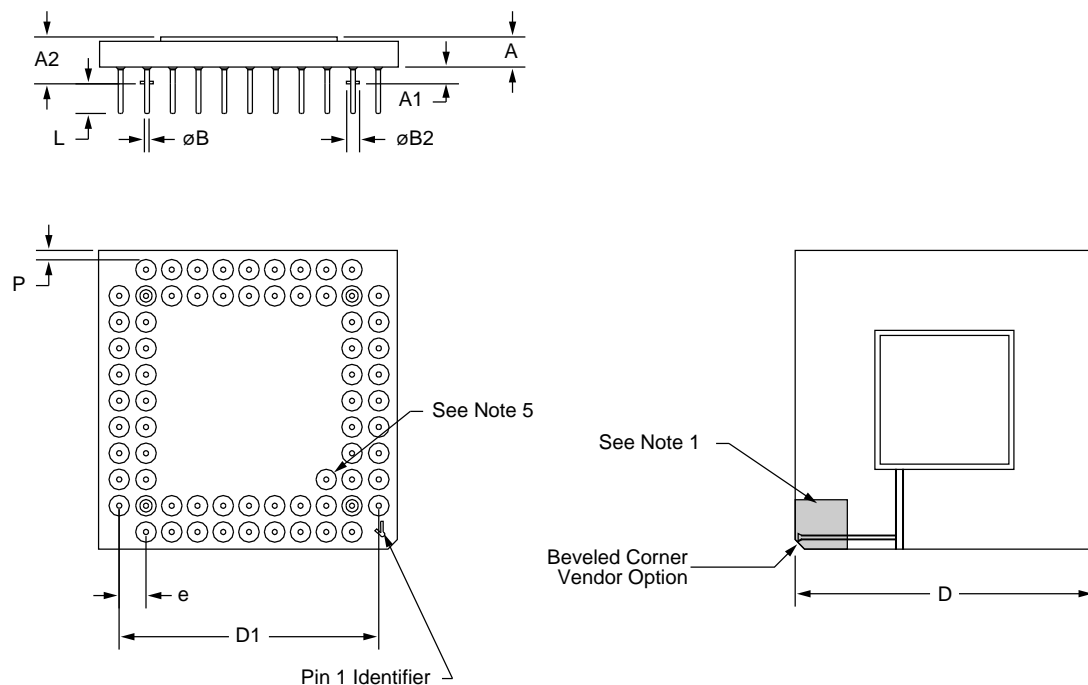
Mechanical Dimensions (continued)

68 Lead Plastic Leaded Chip Carrier

Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982

2. Corner and edge chamfer (J) = 45°

3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)
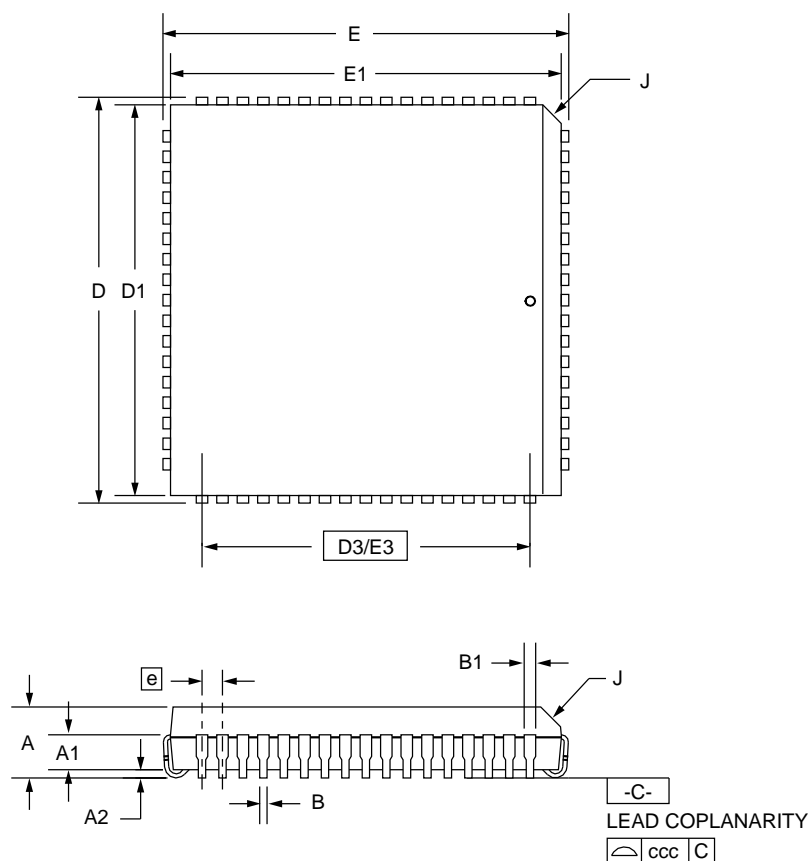
Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2301G8C	STD–T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301G8C
TMC2301G8C1	STD–T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301G8C1
TMC2301G8C2	STD–T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301G8C2
TMC2301H8C	STD–T_A =0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C
TMC2301H8C1	STD–T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C1
TMC2301H8C2	STD–T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C2
TMC2301R1C	STD-T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C
TMC2301R1C1	STD T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C1
TMC2301R1C2	STD-T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C2