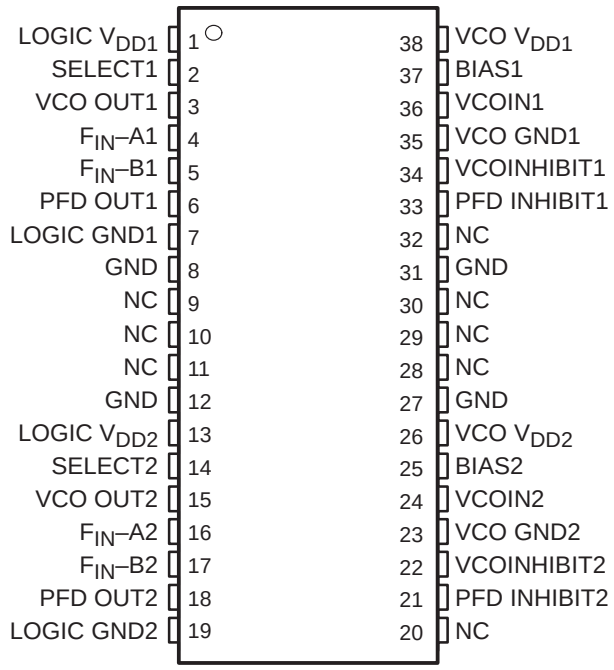
- **Dual TLC2932 by Multichip Module (MCM) Technology**
- **Voltage-Controlled Oscillator (VCO) Section:**
  - **Complete Oscillator Using Only One External Bias Resistor (R_{BIAS})**
  - **Recommended Lock Frequency Range:**
    22 MHz to 50 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1 Output)
    11 MHz to 25 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1/2 Output)
  - **Output Frequency . . . ×1 and ×1/2 Selectable**
- **Includes a High-Speed Edge-Triggered Phase Frequency Detector (PFD) With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**

DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

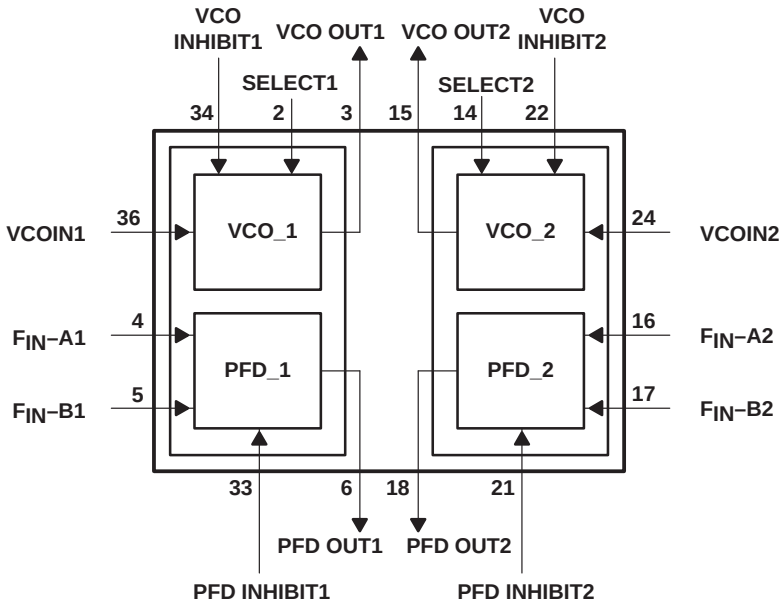
The TLC2942 is a multichip module product that uses two TLC2932 chips. The TLC2932 chip is composed of a voltage-controlled oscillator and an edge-triggered phase frequency detector. The oscillation frequency range of each VCO is set by an external bias resistor (R_{BIAS}) and each VCO output can be a ×1 or ×1/2 output frequency. Each high speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. The VCO and the PFD have inhibit functions that can be used as a power-down mode. The high-speed and stable oscillation capability of the TLC2932 makes the TLC2942 suitable for use in dual high-performance phase-locked loop (PLL) systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (DB)
–20°C to 75°C	TLC2942IDB

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BIAS1	37	I	VCO1 bias supply. An external resistor ($R_{BIAS}1$) between VCO V_{DD1} and BIAS1 supplies bias for adjusting the oscillation frequency range.
BIAS2	25	I	VCO2 bias supply. An external resistor (R_{BIAS2}) between VCO V_{DD2} and BIAS2 supplies bias for adjusting the oscillation frequency range.
F_{IN}–A1	4	I	Input reference frequency 1. The frequency f(REF IN)1 is applied to F_{IN}-A1.
F_{IN}–A2	16	I	Input reference frequency 2. The frequency f(REF IN)2 is applied to F_{IN}-A2.
F_{IN}–B1	5	I	Input for VCO1 external counter output frequency f(F_{IN}-B)1. F_{IN}-B1 is nominally provided from the external counter (see Figure 28).
F_{IN}–B2	17	I	Input for VCO2 external counter output frequency f(F_{IN}-B)2. F_{IN}-B2 is nominally provided from the external counter (see Figure 28).
GND	8, 12, 27,31		Ground
LOGIC V_{DD1}	1		Logic1 supply voltage. LOGIC V_{DD1} supplies voltage to internal logic 1. LOGIC V_{DD1} should be separate from the other supply lines to reduce cross-coupling between power supplies.
LOGIC V_{DD2}	13		Logic2 supply voltage. LOGIC V_{DD2} supplies voltage to internal logic 2. LOGIC V_{DD2} should be separate from the other supply lines to reduce cross-coupling between power supplies.
LOGIC GND1	7		Ground for the internal logic 1
LOGIC GND2	19		Ground for the internal logic 2
NC	9, 10, 11, 20, 28, 29, 30, 32		No internal connection
PFD INHIBIT1	33	I	PFD inhibit 1 control. When PFD INHIBIT1 is high, PFD OUT1 is in the high-impedance state (see Table 4).
PFD INHIBIT2	21	I	PFD inhibit 2 control. When PFD INHIBIT2 is high, PFD OUT2 is in the high-impedance state (see Table 5).
PFD OUT1	6	O	PFD1 output. When the PFD INHIBIT1 is high, PFD OUT1 is in the high-impedance state.
PFD OUT2	18	O	PFD2 output. When the PFD INHIBIT2 is high, PFD OUT2 is in the high-impedance state.
SELECT1	2	I	VCO1 output frequency select. When SELECT1 is high, the VCO1 output frequency is $\times$1/2 and when SELECT1 is low, the output frequency is $\times$1 (see Table 1).
SELECT2	14	I	VCO2 output frequency select. When SELECT2 is high, the VCO2 output frequency is $\times$1/2 and when SELECT2 is low, the output frequency is $\times$1 (see Table 1).
VCO GND1	35		Ground for VCO1
VCO GND2	23		Ground for VCO2
VCOINHIBIT1	34	I	VCO1 inhibit control. When VCOINHIBIT1 is high, VCO OUT1 is low (see Table 2).
VCOINHIBIT2	22	O	VCO2 inhibit control. When VCOINHIBIT2 is high, VCO OUT2 is low (see Table 3).
VCO OUT1	3	O	VCO1 output. When VCOINHIBIT1 is high, VCO OUT1 is low.
VCO OUT2	15		VCO2 output. When VCOINHIBIT2 is high, VCO OUT2 is low.
VCO V_{DD1}	38		VCO1 supply voltage. VCO V_{DD1} supplies voltage for VCO1. VCO V_{DD1} should be separated from LOGIC V_{DD1} and LOGIC V_{DD2} and VCO $V_{DD}2$ to reduce cross-coupling between power supplies.
VCO V_{DD2}	26		VCO2 supply voltage. VCO V_{DD2} supplies voltage for VCO2. VCO V_{DD2} should be separated from LOGIC V_{DD1} and LOGIC V_{DD2} and VCO $V_{DD}1$ to reduce cross-coupling between power supplies.
VCOIN1	36	I	VCO1 control voltage input. Nominally the external loop filter output1 connects to VCOIN1 to control VCO1 oscillation frequency.
VCOIN2	24	I	VCO2 control voltage input. Nominally the external loop filter output2 connects to VCOIN2 to control VCO2 oscillation frequency.

detailed description

multichip module

The TLC2942 is a multichip module (MCM) product that uses two TLC2932 chips. A newly developed lead frame for TLC2942IBD is specially shaped and cut in the package to electrically isolate one chip from another. The two chips are completely independent from each other to perform the best stable oscillation and locking. If asynchronous locking operation is required for these two PLL blocks, each TLC2942 VCO and PFD can achieve the same stability as the single chip TLC2932IPW.

Three NC terminals are on both sides of the package between chip1 and chip2 due to the lead frame shape. To avoid performance degradation, special attention is needed for each PLL block PCB layout especially for supply voltage lines and GND patterns.

voltage-controlled oscillator (VCO)

VCO1 and VCO2 have the same typical characteristics. Each VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between each VCO V_{DD} and BIAS terminals. The oscillation frequency and range depends on this register value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 kΩ with V_{DD} = 3 V and nominally 2.2 kΩ with V_{DD} = 5 V. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

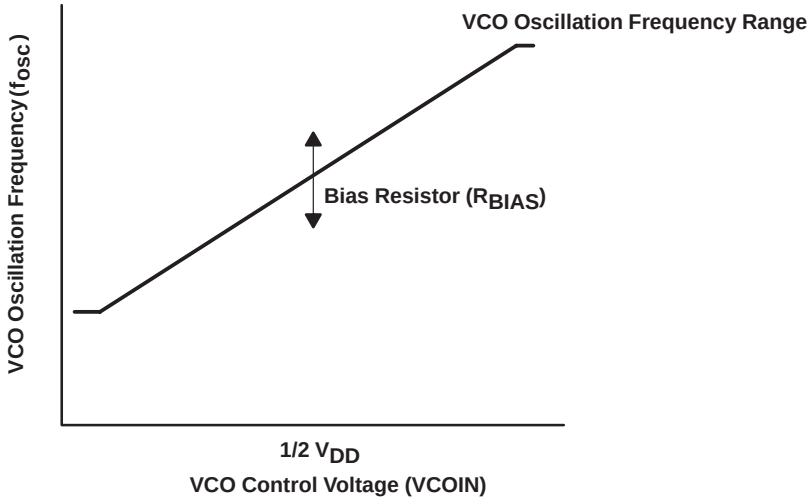


Figure 1. VCO1 and VCO2 Oscillation Frequency

VCO output frequency 1/2 divider

SELECT1 and SELECT2 select between f_{osc} and 1/2 f_{osc} for the VCO output frequencies as shown in Table 1.

Table 1. SELECT1 and SELECT2 Function Table

SELECT1	VCO1 OUTPUT FREQUENCY	SELECT2	VCO2 OUTPUT FREQUENCY
Low	f_{osc1}	Low	f_{osc2}
High	1/2 f_{osc1}	High	1/2 f_{osc2}

VCO inhibit function

Each VCO has an externally controlled inhibit function that inhibits the VCO output. The VCO oscillation is stopped during a high level on VCOINHIBIT, so the high level can also be used as the power-down mode. The VCO output maintains a low level during the power-down mode (see Table 2 and Table 3).

Table 2. VCO1 Inhibit Function

VCOINHIBIT1	VCO1 OSCILLATOR	VCO OUT1	VCO1 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power Down

Table 3. VCO2 Inhibit Function

VCOINHIBIT2	VCO2 OSCILLATOR	VCO OUT2	VCO2 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to F_{IN}–A and F_{IN}–B as shown in Figure 2. Nominally the reference is supplied to F_{IN}–A, and the frequency from the external counter output is fed to F_{IN}–B.

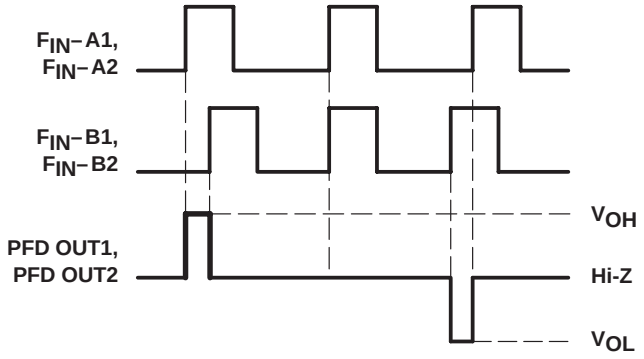


Figure 2. PFD Function Timing Chart

PFD output control

A high level on PFD INHIBIT places the PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 4 and Table 5. A high level on PFD INHIBIT also can be used as the power-down mode for the PFD.

Table 4. PFD1 Inhibit Function

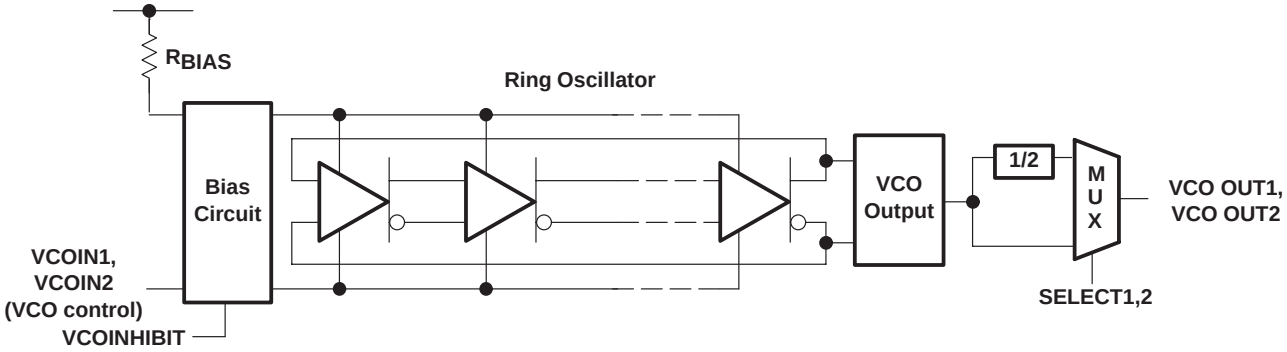
PFD INHIBIT1	DETECTION	PFD OUT1	PFD1 I_{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power Down

Table 5. PFD2 Inhibit Function Table

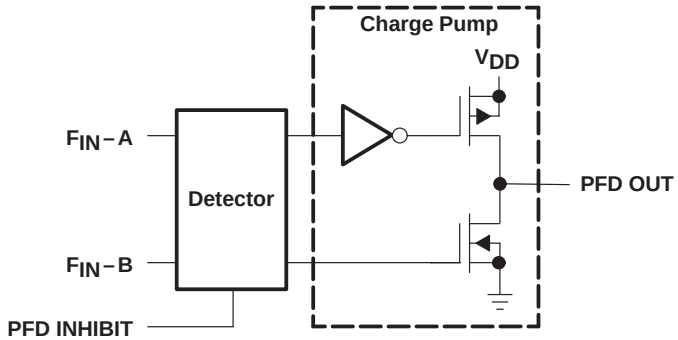
PFD INHIBIT2	DETECTION	PFD OUT2	PFD2 I_{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power Down

schematics

VCO block schematic (VCO1, VCO2)



PFD block schematic (PFD1, PFD2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1) . . . . . 7 V
Input voltage range (each input), V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Input current (each input), I_I . . . . . ±20 mA
Output current (each output), I_O . . . . . ±20 mA
Continuous total power dissipation, at (or below) T_A = 25°C (see Note 2) . . . . . 1160 mW
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 9.3 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_I, (all inputs except VCOIN1, VCOIN2)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at each VCOIN1, VCOIN2		0.9		V_{DD}	V
Lock frequency, (each VCO) (×1 output)	V_{DD} = 3 V	14		21	MHz
	V_{DD} = 5 V	22		50	
Lock frequency, (each VCO) (×1/2 output)	V_{DD} = 3 V	7		10.5	MHz
	V_{DD} = 5 V	11		25	
Bias resistor, (each BIAS), R_{BIAS1}, R_{BIAS2}	V_{DD} = 3 V	2.2	3.3	4.3	kΩ
	V_{DD} = 5 V	1.5	2.2	3.3	
Operating temperature, T_A		–20		75	°C

NOTE 3: It is recommended that LOGIC V_{DD1} and VCO V_{DD1} or LOGIC V_{DD2} and VCO V_{DD2} should be at the same voltage and separated from each other.

VCO1, VCO2 electrical characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.3	V
V_{IT}	Input threshold voltage	SELECT1, SELECT2, VCOINHIBIT2, VCOINHIBIT1		0.9	1.5	2.1	V
I_I	Input current	SELECT1, SELECT2, VCOINHIBIT2, VCOINHIBIT1	$V_I = V_{DD}$ or GND			±1	µA
$Z_{i(VCOIN)}$	Input impedance	VCOIN2, VCOIN1	VCOIN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit) (each chip)		See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current (each chip)		See Note 5		5	15	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCOINHIBIT = V_{DD}, and the PFD is inhibited.
5. The current into VCO V_{DD} and LOGIC V_{DD} when VCOIN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCOINHIBIT = GND, and the PFD is inhibited.

PFD1, PFD2 electrical characteristic, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance output current		PFD INHIBIT = high, $V_O = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2		2.7			V
V_{IL}	Low-level input voltage	F_{IN}–A1, F_{IN}–B1, FIN–A2, F_{IN}–B2				0.5	V
V_{IT}	Input threshold voltage	PFD INHIBIT2, PFD INHIBIT1		0.9	1.5	2.1	V
C_i	Input capacitance	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2			5		pF
Z_i	Input impedance	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2			10		MΩ
$I_{DD(Z)}$	High-impedance state PFD supply current		See Note 6		0.1	1	µA
$I_{DD(PFD)}$	PFD supply current		See Note 7		0.1	1.5	mA

NOTES: 6. The current into LOGIC V_{DD}, when F_{IN}–A and F_{IN}–B = GND, PFD INHIBIT= V_{DD}, no load, and VCO OUT is inhibited.
7. The current into LOGIC V_{DD} when F_{IN}–A and F_{IN}–B = 1 MHz with $V_{I(PP)}$ = 3 V rectangular wave, PFD INHIBIT = GND, no load, and VCO OUT is inhibited.

VCO1, VCO2 operating characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS1}, R_{BIAS2} = 3.3 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation	See Note 8			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		7	14	ns
		C_L = 50 pF, See Figure 3		14		
t_f	Fall time	C_L = 15 pF, See Figure 3		6	12	ns
		C_L = 50 pF, See Figure 3		10		
	Duty cycle at VCO OUT	R_{BIAS1}, R_{BIAS2} = 3.3 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS1}, R_{BIAS2} = 3.3 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}, T_A = –20°C to 75°C		0.04		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS1}, R_{BIAS2} = 3.3 kΩ, VCOIN1, VCOIN2 = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.02		%/mV
	Jitter absolute (see Note 9)	R_{BIAS1} = 3.3 kΩ		100		ps

NOTES: 8. The time period to stabilize the VCO oscillation frequency after VCOINHIBIT is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD1, PFD2 operating characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}	PFD output disable time from high level			23	50	
t_{PZL}	PFD output enable time to low level			11	30	ns
t_{PZH}	PFD output enable time to high level			10	30	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns

VCO1, VCO2 electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –2 mA	4			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
V_{IT}	Input threshold voltage	SELECT1, SELECT2, VCOINHIBIT1, VCOINHIBIT2		1.5	2.5	3.5	V
I_I	Input current	SELECT1, SELECT2, VCOINHIBIT1, VCOINHIBIT2	V_I = V_{DD} or GND			±1	µA
$Z_{i(VCOIN)}$	Input impedance	VCOIN1, VCOIN2	VCOIN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit) (each chip)		See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current (each chip)		See Note 10		15	35	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCOINHIBIT = V_{DD}, and the PFD is inhibited.
10. The current into VCO V_{DD} and LOGIC V_{DD} when VCOIN = 1/2 V_{DD}, R_{BIAS} = 2.2 kΩ, VCOINHIBIT = GND, and the PFD is inhibited.

PFD1, PFD2 electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance output current		PFD INHIBIT1, PFD INHIBIT2 = high, V_O = V_{DD} or GND			±1	µA
V_{IH}	High-level input voltage	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2		4.5			V
V_{IL}	Low-level input voltage	F_{IN}–A1, F_{IN}–B1, FIN–A2, F_{IN}–B2				1	V
V_{IT}	Input threshold voltage	PFD INHIBIT2, PFD INHIBIT1		1.5	2.5	3.5	V
C_i	Input capacitance	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2			5		pF
Z_i	Input impedance	F_{IN}–A1, F_{IN}–B1, F_{IN}–A2, F_{IN}–B2			10		MΩ
$I_{DD(Z)}$	High-impedance state PFD supply current		See Note 6		0.1	1	µA
$I_{DD(PFD)}$	PFD supply current (each chip)		See Note 11		0.15	3	mA

NOTES: 6. The current into LOGIC V_{DD}, when F_{IN}–A and F_{IN}–B = GND, PFD INHIBIT= V_{DD}, no load, and VCO OUT is inhibited.
11. The current into LOGIC V_{DD} when F_{IN}–A and F_{IN}–B = 1 MHz with $V_{I(PP)}$ = 5-V rectangular wave, PFD INHIBIT = GND, no load, and
VCO OUT is inhibited.

VCO1, VCO2 operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS1}, R_{BIAS2} = 2.2 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}	32	41	50	MHz
$t_{s(fosc)}$	Time to stable oscillation	See Note 8			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		5.5	10	ns
		C_L = 50 pF, See Figure 3		8		
t_f	Fall time	C_L = 15 pF, See Figure 3		5	10	ns
		C_L = 50 pF, See Figure 3		6		
	Duty cycle at VCO OUT	R_{BIAS1}, R_{BIAS2} = 2.2 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS1}, R_{BIAS2} = 2.2 kΩ, VCOIN1, VCOIN2 = 1/2 V_{DD}, T_{ope} = –20°C to 75°C		0.06		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS1}, R_{BIAS2} = 2.2 kΩ, VCOIN1, VCOIN2 = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.006		%/mV
	Jitter absolute (see Note 9)	R_{BIAS1} = 3.3 kΩ		100		ps

NOTES: 8. The time period to stabilize the VCO oscillation frequency after VCOINHIBIT is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD1, PFD2 operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	
t_{PZL}	PFD output enable time to low level			7.3	20	ns
t_{PZH}	PFD output enable time to high level			6.5	20	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns

PARAMETER MEASUREMENT INFORMATION

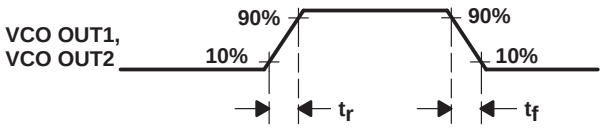
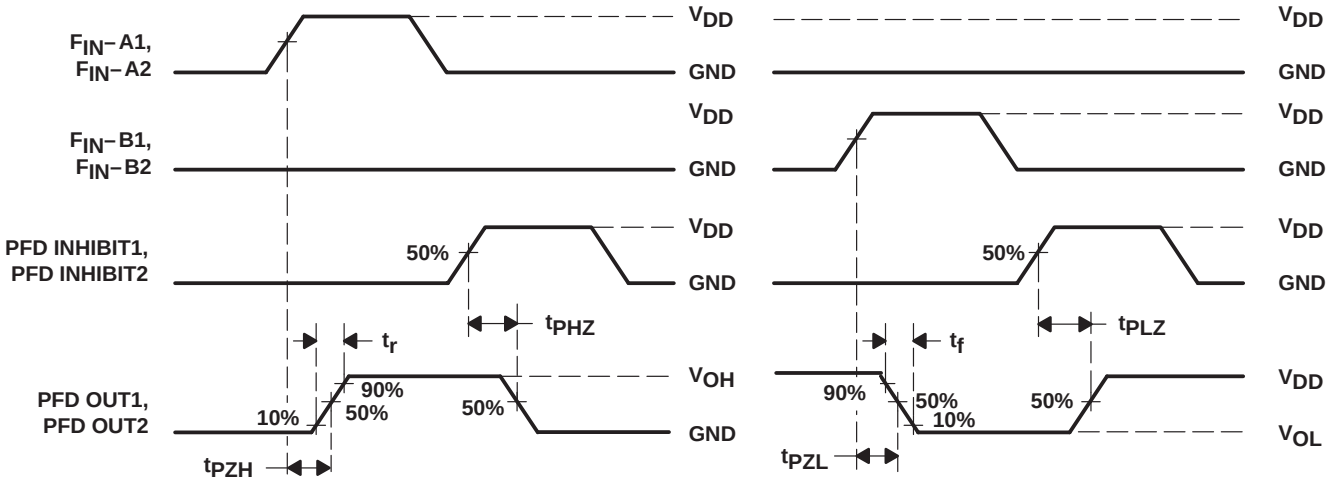


Figure 3. VCO Output Voltage Waveform



(a) OUTPUT PULLDOWN (see Figure 5 and Table 6)

(b) OUTPUT PULLUP (see Figure 5 and Table 6)

† F_{IN}–A and F_{IN}–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 6. PFD1 and PDF2 Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

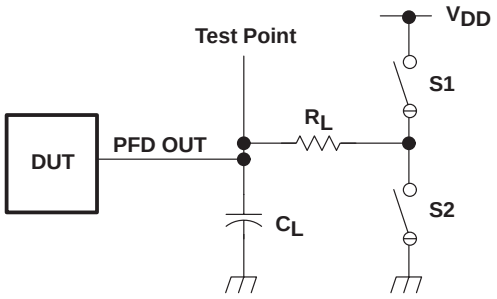


Figure 5. PFD1 and PFD2 Output Test Conditions

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

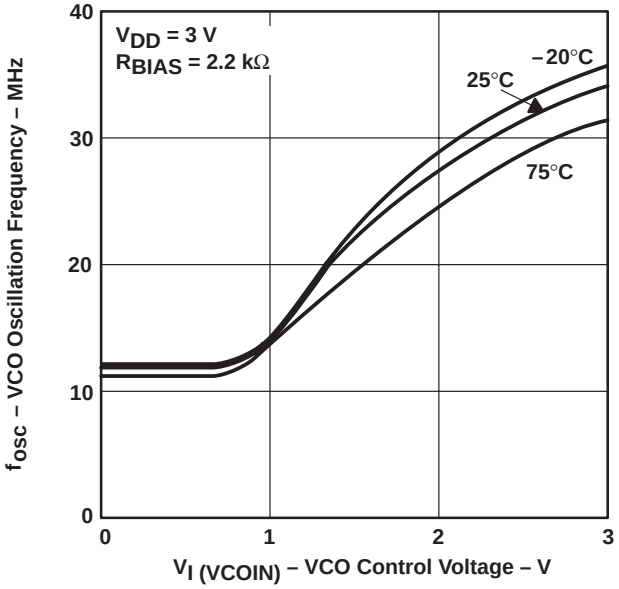


Figure 6

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

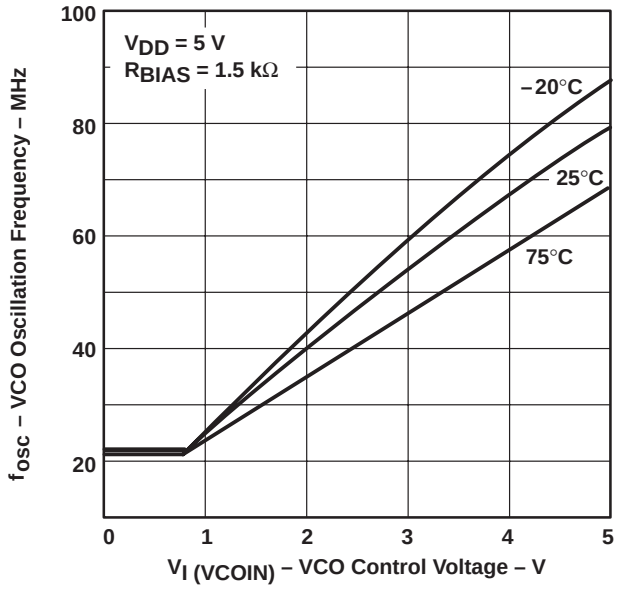


Figure 7

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

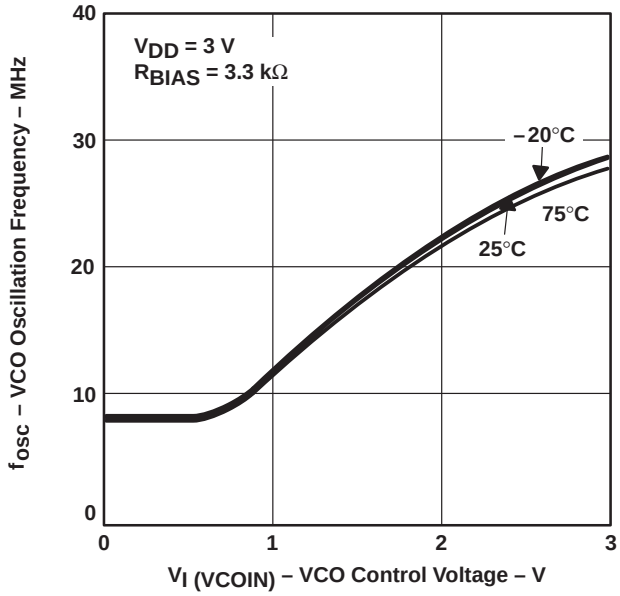


Figure 8

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

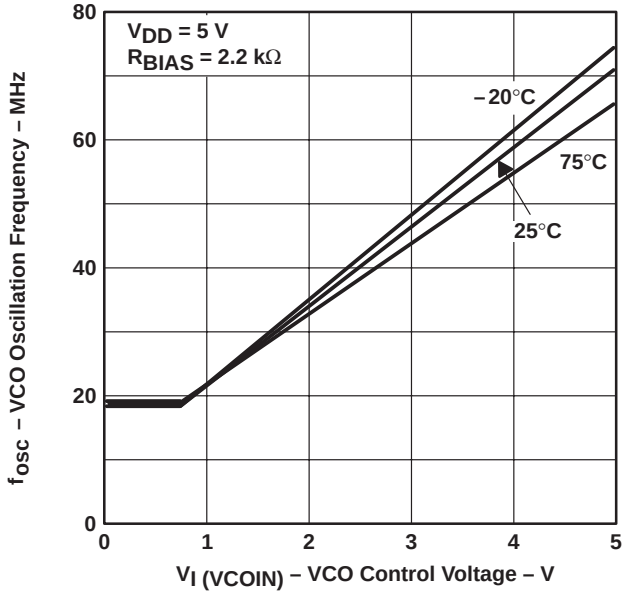


Figure 9

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

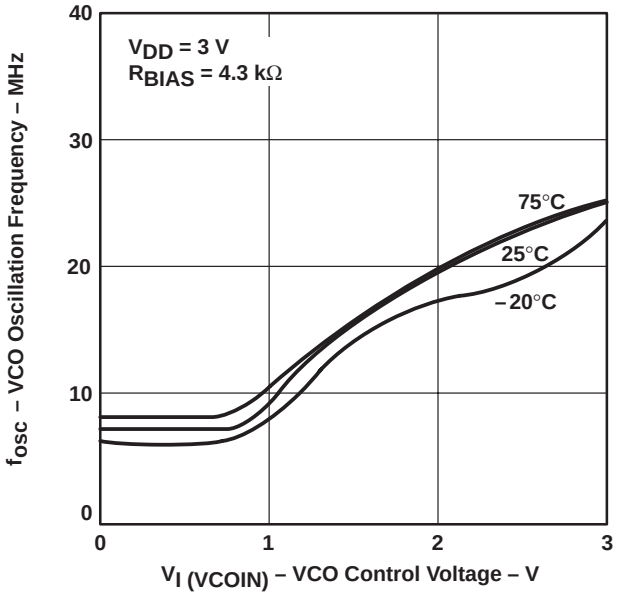


Figure 10

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

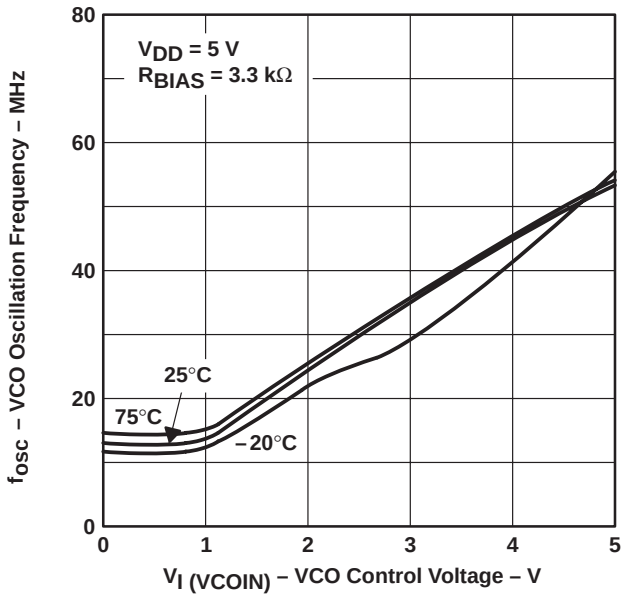


Figure 11

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

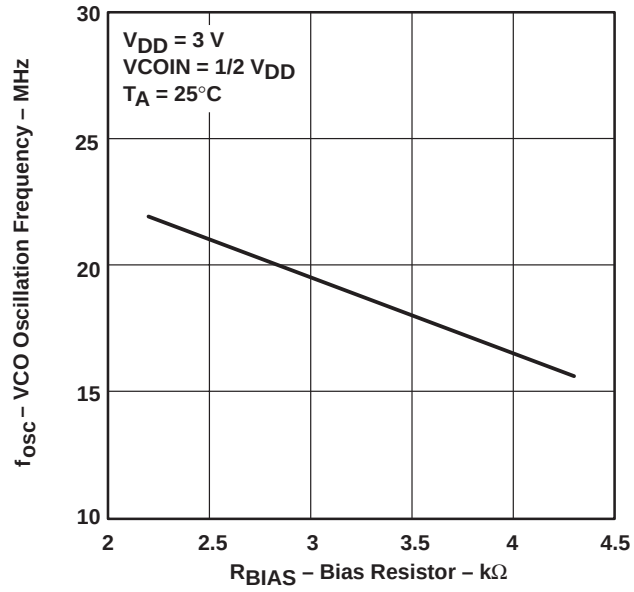


Figure 12

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

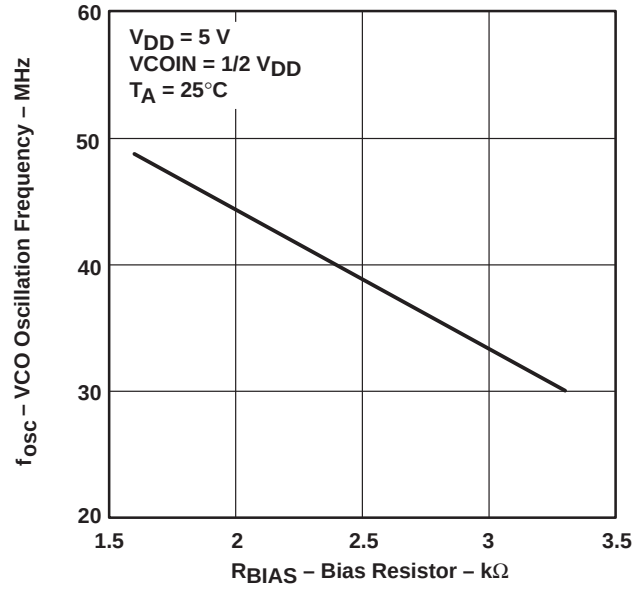


Figure 13

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

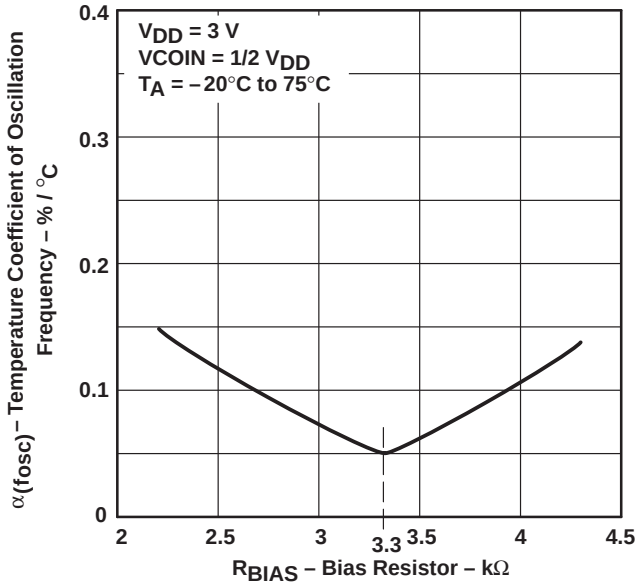


Figure 14

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

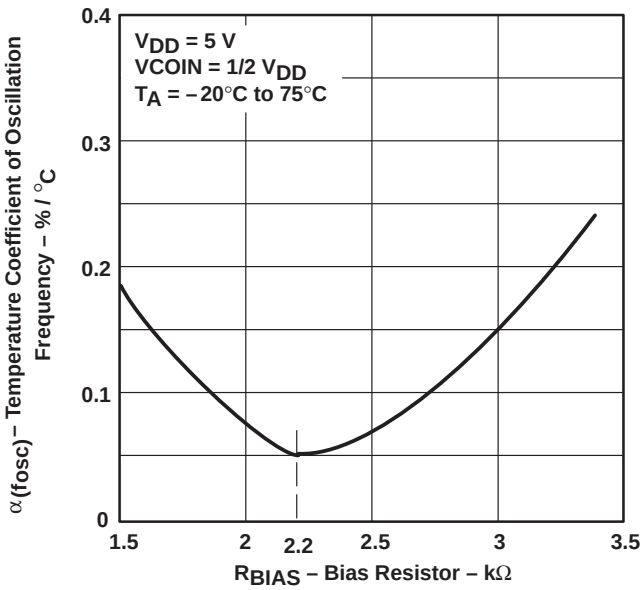


Figure 15

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

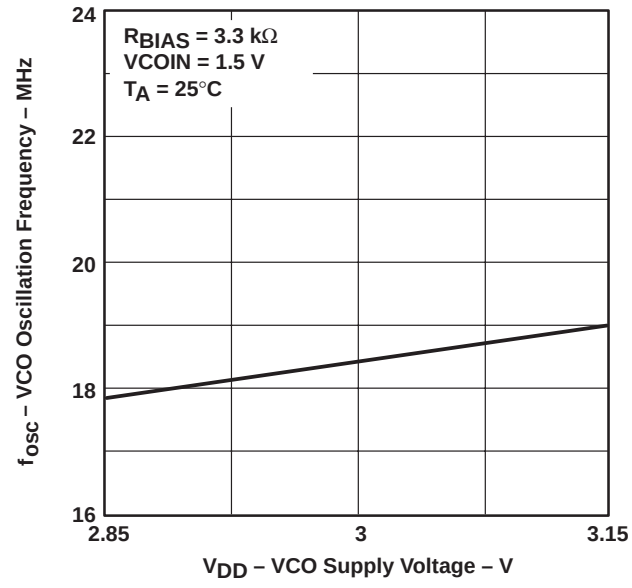


Figure 16

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

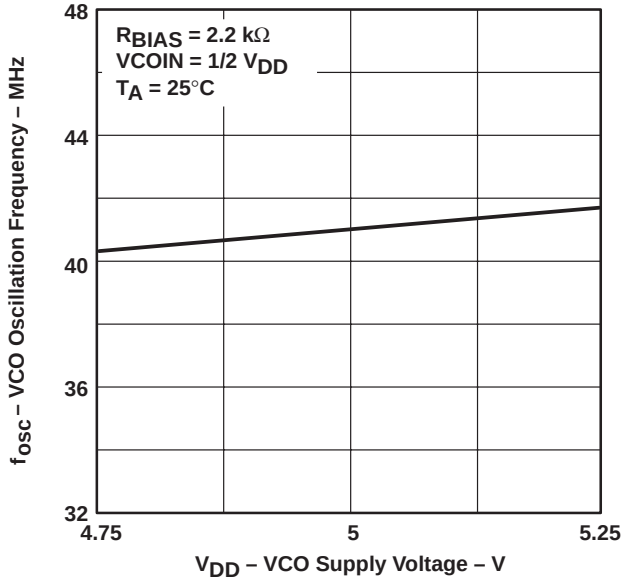


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

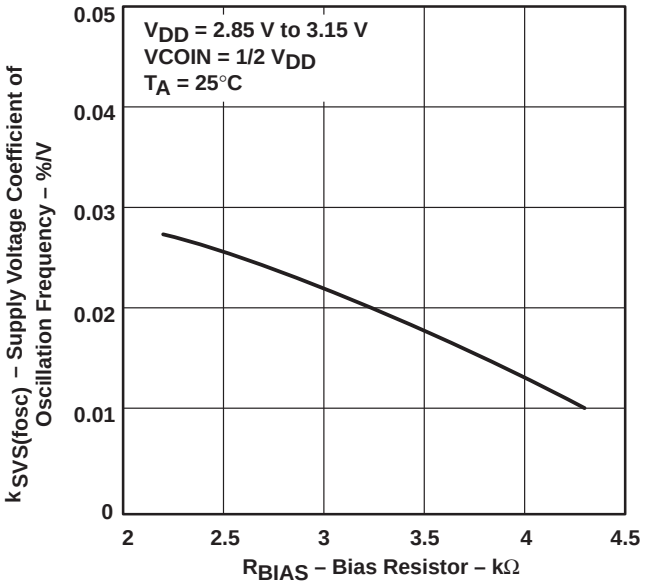


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

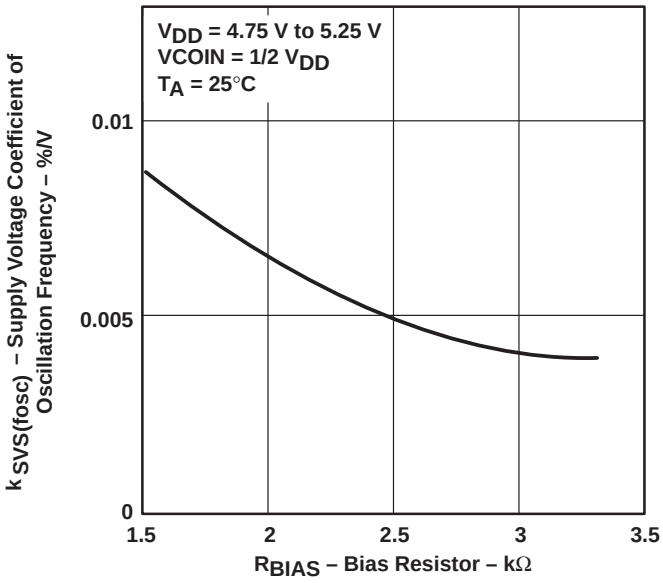


Figure 19

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

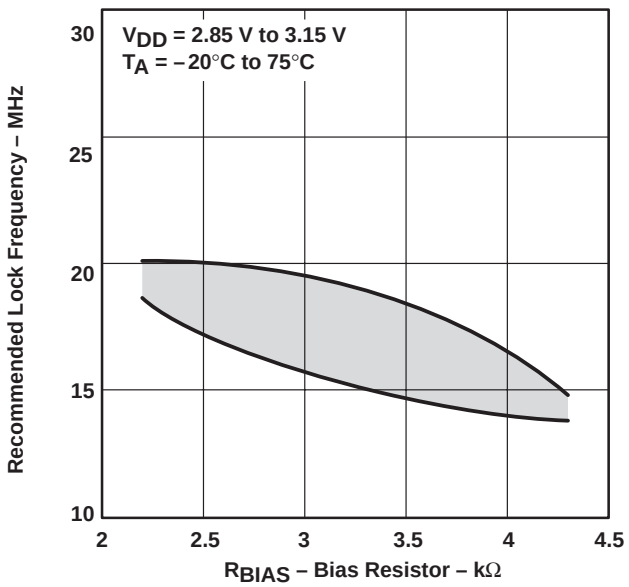


Figure 20

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

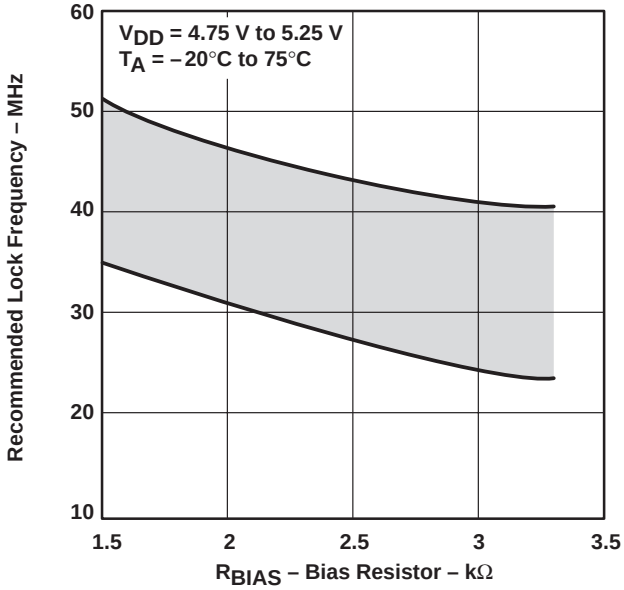


Figure 21

TYPICAL CHARACTERISTICS

**RECOMMENDED LOCK FREQUENCY
(×1/2 OUTPUT)
vs
BIAS RESISTOR**

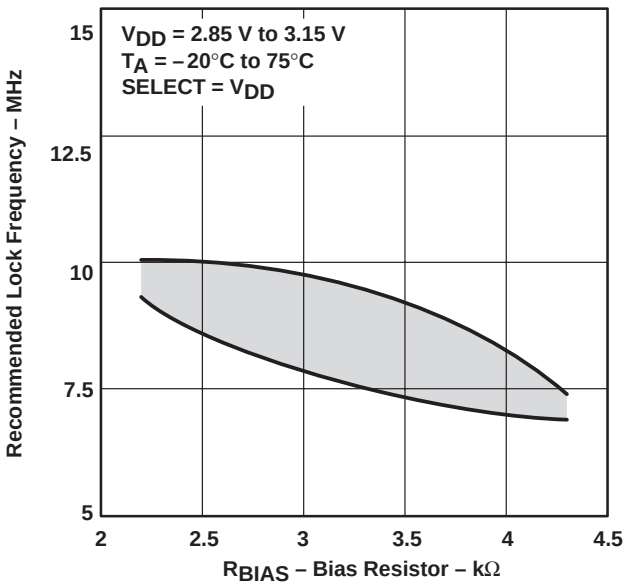


Figure 22

**RECOMMENDED LOCK FREQUENCY
(×1/2 OUTPUT)
vs
BIAS RESISTOR**

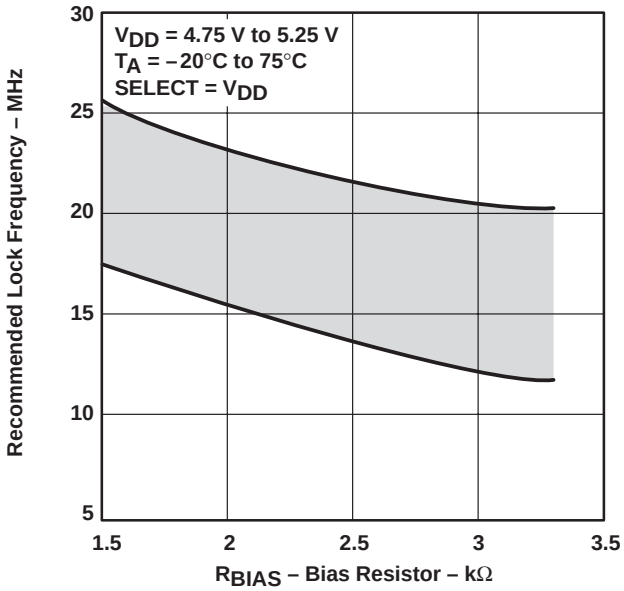


Figure 23

APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 24. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 24(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 24(c).

The parameters for the block diagram with the units are as follows:

K_V : VCO gain (rad/s/V)
K_p : PFD gain (V/rad)
K_f : LPF gain (V/V)
K_N : countdown divider gain (1/N)

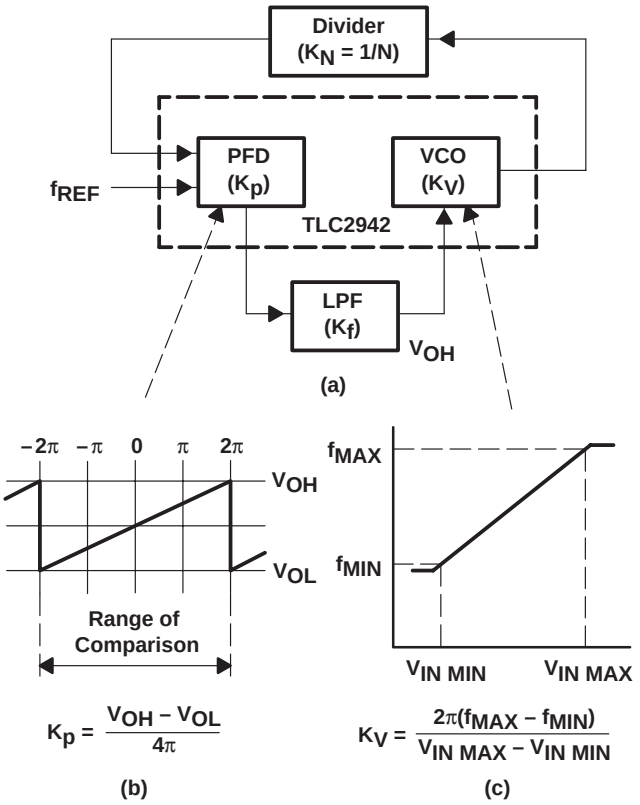


Figure 24. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCOIN terminal. However, for optimum temperature performance, a resistor value of 3.3 kΩ with a 3-V supply, or a resistor value of 2.5 kΩ for a 5-V supply is recommended. For the most accurate results, a metal-film resistor is the better choice, but a carbon-compositiion resistor can be used with excellent results also. A 0.22-μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 25 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right) \left(K_V\right) \left(K_f\,(\infty)\right) \quad (1)$$

Where

$K_f\,(\infty)$ = the filter transfer function value at $\omega = \infty$

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and they should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 25. When the active filter of Figure 25(c) is used, the reference should be applied to F_{IN}-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one-tenth the value of C1.

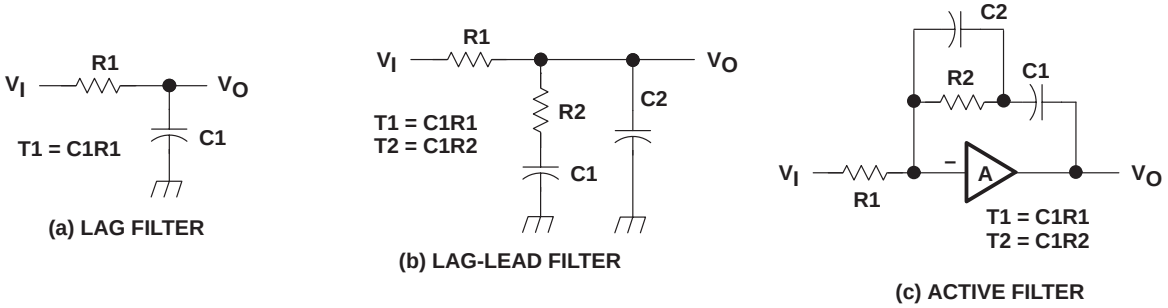


Figure 25. LPF Examples for PLL

the passive filter

The transfer function for the low-pass filter shown in Figure 25(b) is:

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T2}{1 + s \cdot (T1 + T2)} \tag{2}$$

Where

$$T1 = R1 \cdot C1 \text{ and } T2 = R2 \cdot C1$$

Using this filter makes the closed loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 26.

the active filter

When using the active filter shown in Figure 25(c), the phase detector inputs must be reversed since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the F_{IN}-B terminal and the output of the VCO divider should be applied to the input reference terminal, F_{IN}-A.

The transfer function for the active filter shown in Figure 25(c) is:

$$F(s) = \frac{1 + s \cdot R2 \cdot C1}{s \cdot R1 \cdot C1} \tag{3}$$

Using this filter makes the closed loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 27.

APPLICATION INFORMATION

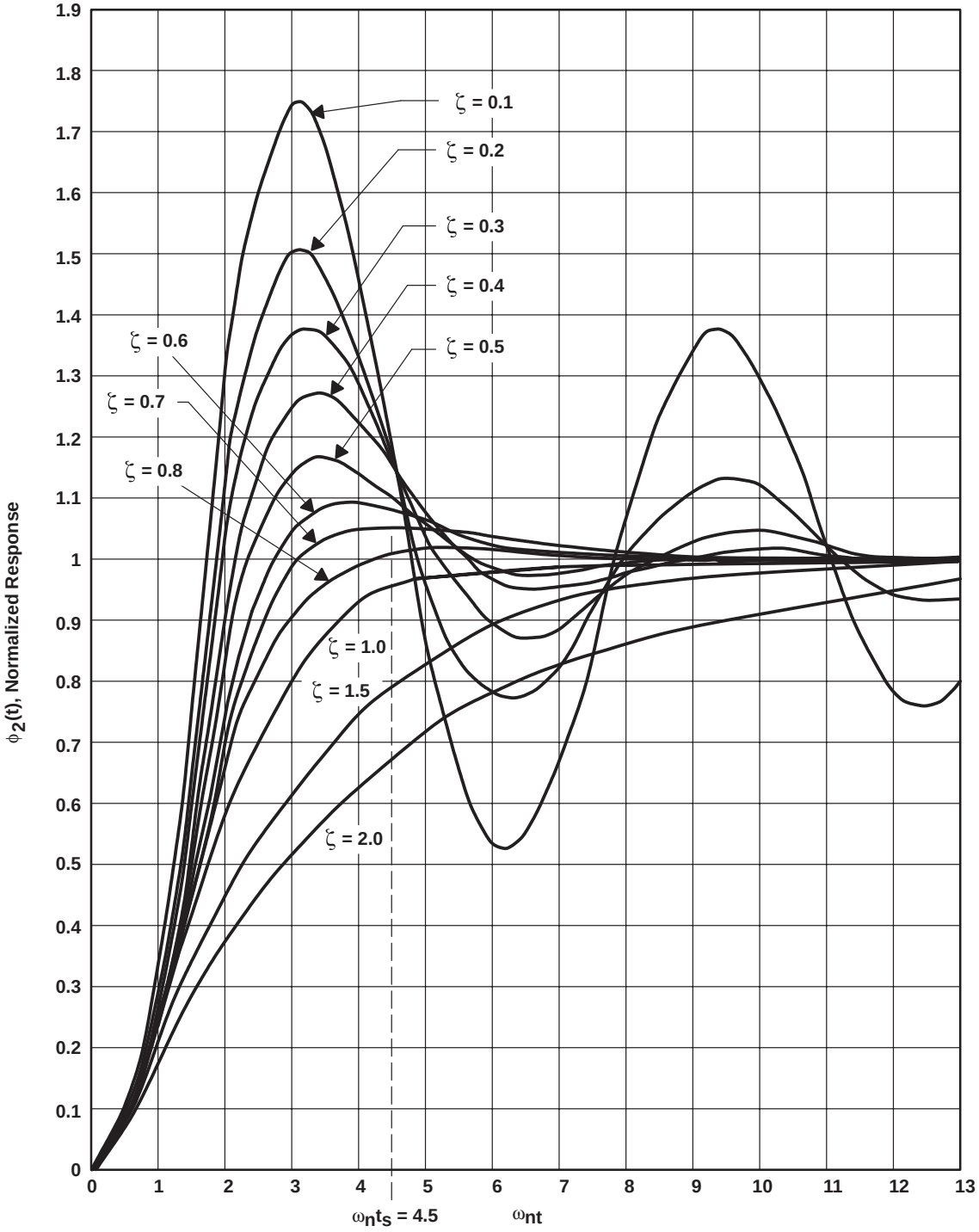


Figure 26. Type 1 Second-Order Step Response

APPLICATION INFORMATION

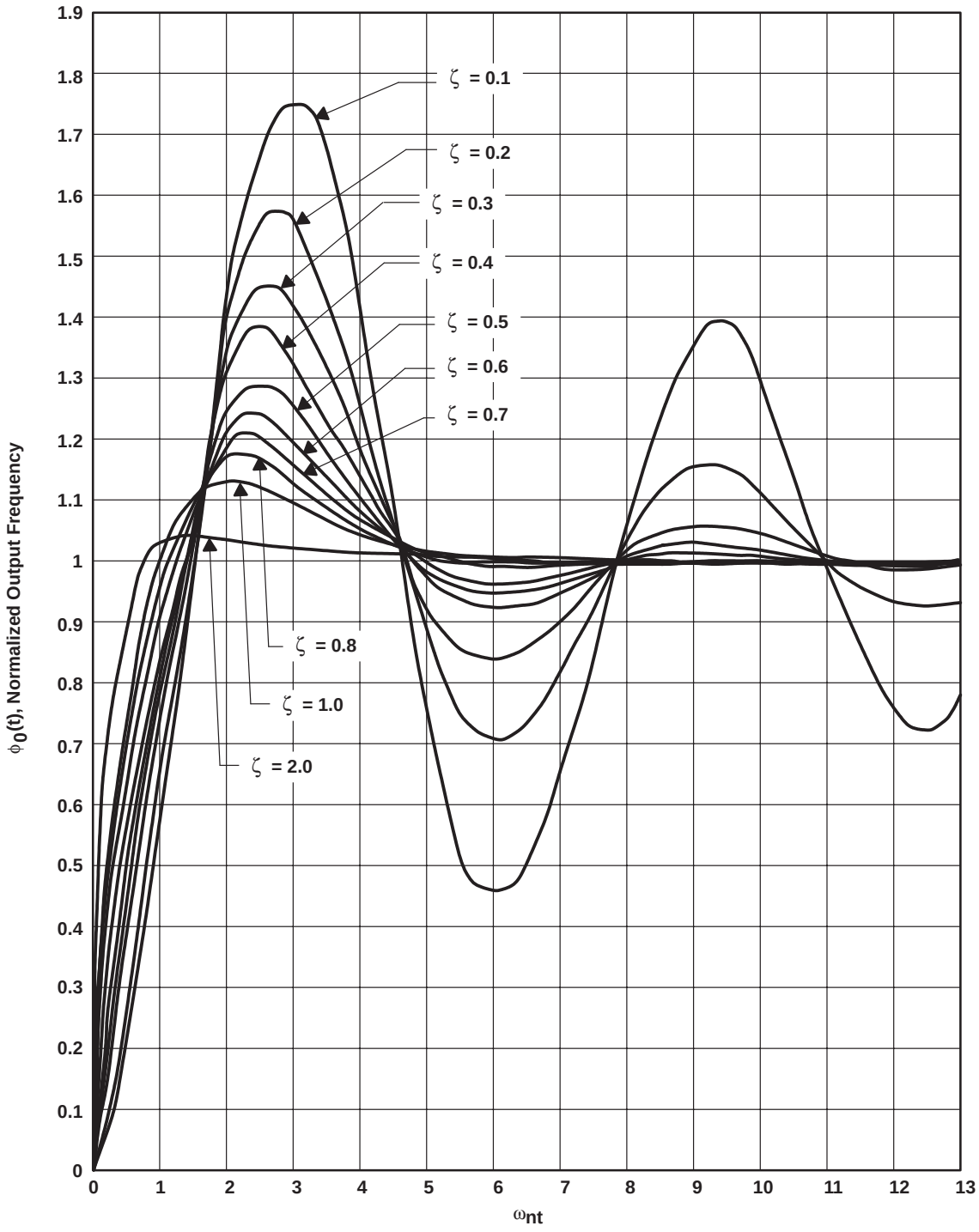


Figure 27. Type 2 Second-Order Step Response

APPLICATION INFORMATION

basic design example

The following design example presupposes that the input reference frequency and the required frequency of the VCO are within the respective ranges of the device.

Assume the loop has to have a 100-μs settling time (t_s) with a countdown divider N value = 8. Using the Type 1, second-order response curves of Figure 26, a value of 4.5 radians is selected for $\omega_n t_s$ with a damping factor of 0.7. This selection gives a good combination for settling time, accuracy, and loop gain margin. The initial parameters are summarized in Table 7. The loop constants, K_V and K_p, are calculated from the data sheet specifications and Table 8 shows these values.

The natural loop frequency is calculated as follows:

Since

$$\omega_n t_s = 4.5 \tag{4}$$

Then

$$\omega_n = \frac{4.5}{100\ \mu s} = 45\ \text{k-radians/sec}$$

Table 7. Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Divider value	N	8	
Lockup time	t	100	μs
Radian value to selected lockup time	$\omega_n t$	4.5	rad
Damping factor	ζ	0.7	

Table 8. Device Specifications

PARAMETER	SYMBOL	VALUE	UNITS
VCO gain	K_V	76.6	Mrad/V/s
f_{MAX}		70	MHz
f_{MIN}		20	MHz
$V_{IN\ MAX}$		5	V
$V_{IN\ MIN}$		0.9	V
PFD gain	K_p	0.342357	V/rad

Using the low-pass filter in Figure 25(b) and divider N value, the transfer function for phase and frequency are shown in equations 5 and 6. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, transfer function of Figure 24 (a) for phase is:

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \cdot K_V}{N \cdot (T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \tag{5}$$

APPLICATION INFORMATION

and the transfer function for frequency is:

$$\frac{F_{OUT(s)}}{F_{REF(s)}} = \frac{K_p \cdot K_V}{(T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (6)$$

The standard two-pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2$ and comparing the coefficients of the denominator of equation 5 and 6 with the standard two-pole denominator gives the following results:

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \quad (7)$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \cdot K_V}{N \cdot \omega_n{}^2}$$

and by using this value for T1 + T2 in equation 7 the damping factor is:

$$\zeta = \frac{\omega_n}{2} \cdot \left(T2 + \frac{N}{K_p \cdot K_V} \right) \quad (8)$$

solving for T2:

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \cdot K_V} \quad (9)$$

then by substituting for T2 in equation 7 and solving for T1 as given in equation 10:

$$T1 = \frac{K_V \cdot K_p}{N \cdot \omega_n{}^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \quad (10)$$

From the circuit constants and the initial design parameters then:

$$R1 = \left[\frac{K_p \cdot K_v}{\omega_n{}^2 \cdot N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1} \quad (11)$$

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1} \quad (12)$$

APPLICATION INFORMATION

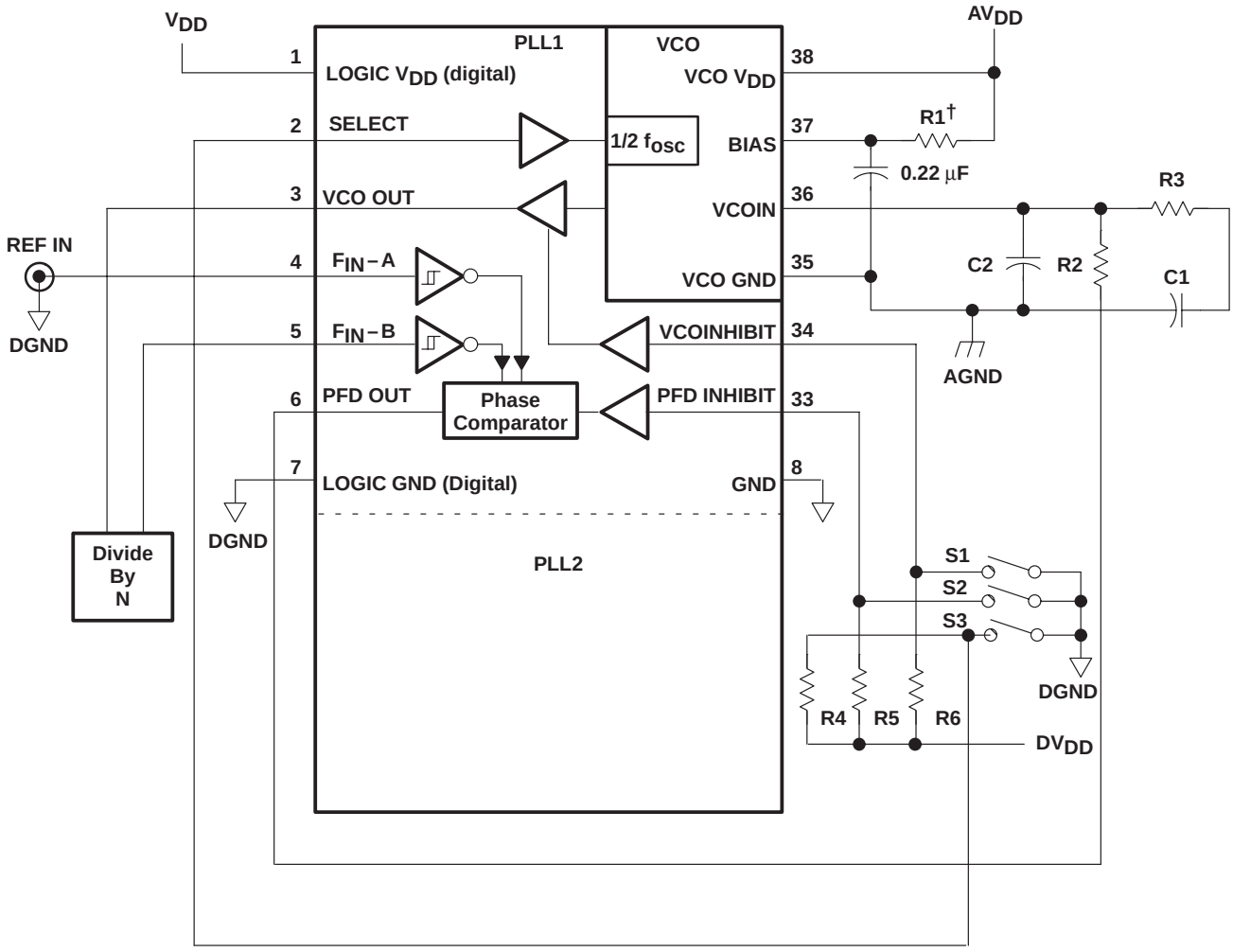
The capacitor, C1, is usually chosen between 1 μF and 0.1 μF to allow for reasonable resistor values and physical capacitor size. In this example, C1 is chosen to be 0.1 μF and the corresponding R1 and R2 calculated values are listed in Table 9.

Table 9. Calculated Values

PARAMETER	SYMBOL	VALUE	UNITS
Natural angular frequency	ω_n	45000	rad/sec
$K = (K_V \bullet K_p)/N$		3.277	Mrad/sec
Lag-lead filter Calculated value Nearest standard value	R1	15870 16000	Ω
Calculated value Nearest standard value	R2	308 300	Ω
Selected value	C1	0.1	μF

APPLICATION INFORMATION

The evaluation and operation schematic for the TLC2942I is shown in Figure 28.



† R_{BIAS} resistor

Figure 28. Evaluation and Operation Schematic

APPLICATION INFORMATION

PCB layout considerations

The TLC2942I contains high frequency analog oscillators; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

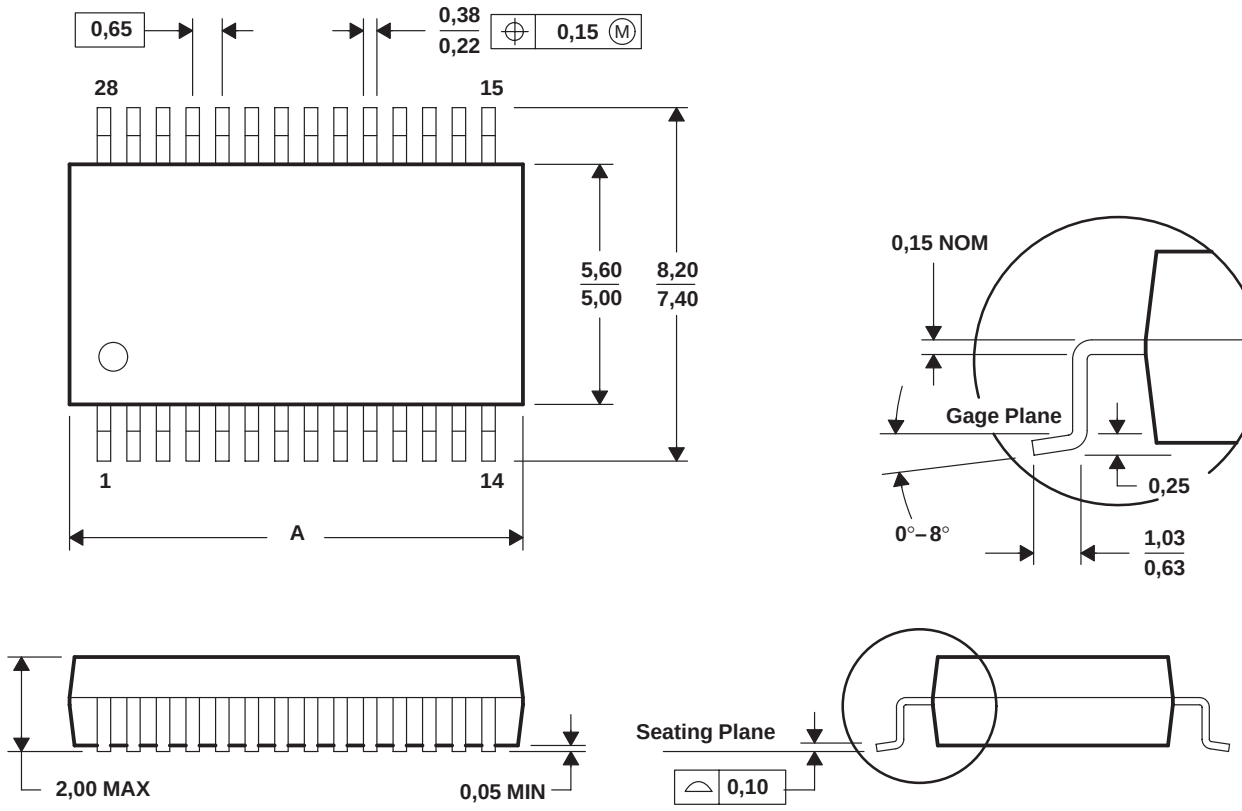
The following design recommendations benefit the TLC2942I user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-μF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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