DATA SHEET

TDA8052T
Quadrature demodulator

Objective specification
File under Integrated Circuits, IC02

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FEATURES

- Wide input frequency range (350 MHz to 650 MHz)
- On IC high precision 0˚ and 90˚ phase shifter
- 5 V supply voltage
- Internal voltage reference
- Suitable for symbol rate up to 45 Msymbols/s
- Nominal overall conversion gain (from IF input to I and Q outputs) adjustable from 42 dB to13 dB.
- Low noise AGC amplifier with 21 dB gain control range
- 30 MHz 1 dB bandwidth output buffers

APPLICATIONS

- BPSK and QPSK demodulation
- Professional and consumer satellite decoders
- Data communication system

GENERAL DESCRIPTION

The TDA8052T is a monolitic bipolar IC dedicated to BPSK and QPSK demodulation. It is designed to be used together with the TDA8043 as part of a complete BPSK/QPSK satellite demodulator and decoder. The bandwidth of the TDA8052T allows symbol rates up to 45 Msymbols/s.

It includes a low noise IF gain controlled amplifier, two matched mixers, a symmetrical oscillator, a 0˚/ 90˚ phase shifter, two low pass filters and two matched baseband amplifiers.

The high input sensitivity makes interfacing with various sources easy. The input sensitivity can be adjusted by means of an internal AGC amplifier.

The oscillator frequency can be set either by the appropriate external LC tank circuit. The internal high precision wideband phase shifter provides two oscillator signals which are 90 degrees out of phase to drive the mixers.

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	V_{CC} = 5.0 V	–	51	–	mA
$V_{i(RF)}$	Operating input level		–	57	–	dBμV
$f_{i(RF)}$	RF input signal frequency range		350	–	650	MHz
$V_{oIQ(p-p)}$	I and Q output amplitude (peak to peak value)		–	0.8	–	V
$\Delta E_{\Phi(I-Q)}$	Phase matching error between I and Q channel		–	0.7	2	deg.
$\Delta E_{G(I-Q)}$	Gain matching error between I and Q channel		–	0.15	0.8	dB
ΔG_{tilt}	Gain flatness over f_{IF} = 30MHz		–	0.3	0.5	dB
$V_{o(CLIP)(p-p)}$	Peak to peak output clipping voltage		1.6	–	–	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8052T	SO16	plastic shrink small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

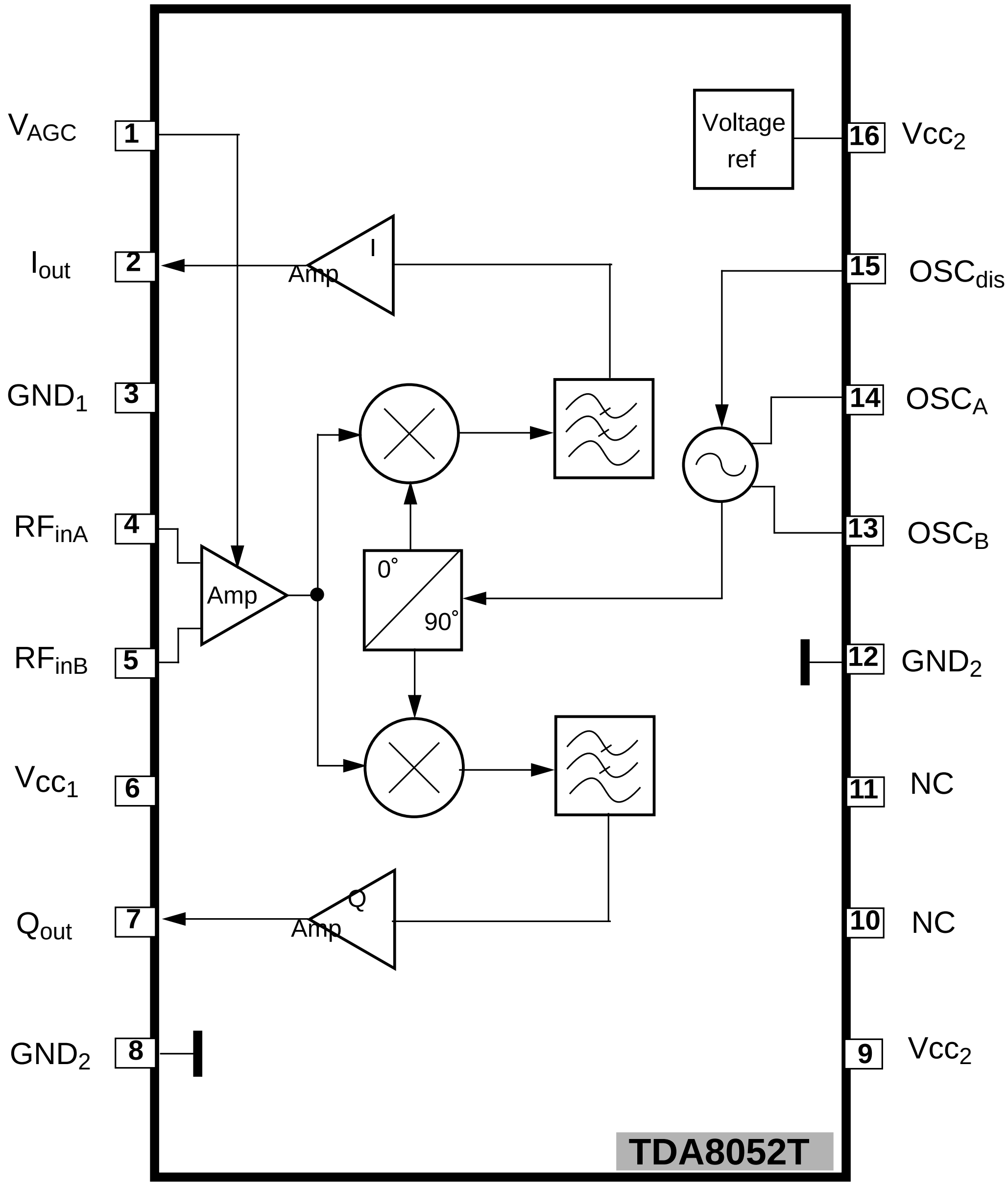


Fig.1 Block diagram

PINNING

SYMBOL	PIN	DESCRIPTION
V_{AGC}	1	gain control input voltage
I_{out}	2	I channel amplifier output
GND1	3	ground
RF_{IN-A}	4	IF input A
RF_{IN-B}	5	IF input B
V_{CC1}	6	supply voltage
Q_{out}	7	Q channel amplifier output
GND2	8	ground
V_{CC2}	9	supply voltage
n.c.	10	not connected
n.c.	11	not connected
GND2	12	ground
Osc_A	13	oscillator tank circuit A
Osc_B	14	oscillator tank circuit B
Osc_{dis}	15	oscillator disable
V_{CC2}	16	supply voltage

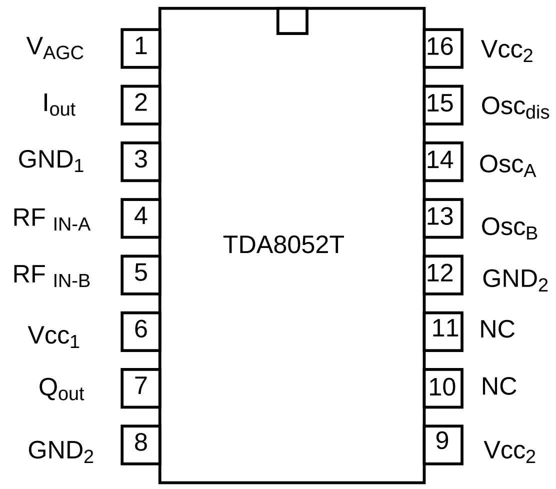


Fig.2 Pin configuration for TDA8052T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6.0	V
V_i	Voltage on all pins	–0.3	V_{CC}	V
P_{tot}	total power dissipation	–	tbf	mW
T_{stg}	IC storage temperature	–55	+150	°C
T_j	junction temperature	–	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (Typical value)	115	K/W

HANDLING

All pins withstand the ESD test in accordance with “UZW-BO/FQ-A302 (human body model)” and with “UZW-BO/FQ-B302 (machine model)”.

CHARACTERISTICS

These characteristics are guaranteed by either production test or design.
Test conditions: V_{CC} = 5 V; T_{amb} = 25 °C; R_{load} = 1 kΩ;F_{IF} = 479.5 MHz; output amplitude 800 mV (p-p) measured in application circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage	V_{CC1} and V_{CC2}	4.75	5.0	5.25	V
I_{CC1}	supply current	V_{CC} = 5.0 V	–	18	–	mA
I_{CC2}	supply current	V_{CC} = 5.0 V	–	33	–	mA
AGC						
G_{CR}	Gain control range		21	29	–	dB
G_{VAGC}	Gain control voltage Input level = $V_{i(RF)min}$ Input level = $V_{i(RF)max}$	note 1	– 0.5 3.5	– – –	– 2 4.5	– V V
R_{VAGC}	V_{AGC} input resistance		–	20	–	kΩ
QPSK demodulator						
$f_{RF\text{-}low}$	minimum IF frequency	note 6	–	–	350	MHz
$f_{RF\text{-}high}$	maximum IF frequency	note 6	650	–	–	MHz
$R_{i(RF)}$	RF input impedance (resistive part)	$f_{i(RF)}$ = 480 MHz		50		Ω
$X_{i(RF)}$	RF input impedance (reactive part)	$f_{i(RF)}$ = 480 MHz	–	5	–	Ω
$V_{i(RF)}$	RF input level		57		78	dBμV
$\Delta E\Phi_{I-Q}$	Phase matching error between I and Q channel	note 2	–	0.7	2	°
ΔEG_{I-Q}	gain matching error between I and Q channel	note 3	–	0.15	0.8	dB
ΔG_{tilt}	gain tilt error between I and Q channels	note 4	–	0.3	0.5	dB
F	DSB noise figure	source impedance = 50 Ω	–	13	17	dB
$d_{3(IQ)}$	third-order intermodulation distortion in I and Q channels	note 5	–	50	–	dB
Oscillator						
$f_{osc\text{-}low}$	Minimum oscillation frequency	note 6	–	–	350	MHz
$f_{osc\text{-}high}$	Maximum oscillation frequency	note 6	650	–	–	MHz
Δf_{osc}	frequency drift	note 7	–	–	500	kHz
		ΔVcc = ± 5%	–	–	100	kHz
N_{osc}	Oscillator phase noise	SSB at 10 kHz offset	–	91	85	dBc/Hz
$V_{osc(dis)}$	oscillator disable voltage	oscillator disabled oscillator enabled	– 4.0	– –	1.0 –	V V
I and Q baseband internal filters						
B_{-1}	Bandwidth for 1 dB attenuation		30	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B_{-30}	Bandwidth for 30 dB attenuation		–	450	–	MHz
I and Q baseband output amplifiers						
$V_{o(IQ)(DC)}$	I and Q channel DC output voltage		–	2.45	–	V
$V_{o(IQ)(p-p)}$	I and Q channel output voltage (peak to peak value)	note 8	–	0.8	–	V
$V_{clip(p-p)}$	I and Q output clipping level (peak to peak value)		1.8	–	–	V
$Z_{L(IQ)}$	I and Q channel output load impedance	note 9	500	–	–	Ω
$R_{o(IQ)}$	I and Q channel output resistance		–	67	–	Ω
$\alpha_{ct(I-Q)}$	Crosstalk between I and Q channel		30	–	–	dB

Notes

1. The Gain control voltage (V_{AGC}) is defined as the DC voltage to be applied on pin 1 to get with the appropriate RF input level, an output signal with an amplitude of 800 mV_{pp} at I and Q output.
   The lowest control voltage corresponds to the highest sensitivity and gain.
2. The phase error is defined as the phase quadrature imbalance between I and Q channel.
3. The gain error is defined as the phase quadrature imbalance between I and Q channel.
4. The tilt is defined as the difference between the maximum and the minimum channel gain measured in a frequency band of ± 30 MHz around f_{RF}. The specified tilt is the maximum tilt value found in one of the I and Q channels.
5. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in I and Q channel. The specified value is the minimum distance between wanted signal and intermodulation products measured at the output for a wanted output level of 0.8 Vpp.
6. The oscillator is tuned with an appropriate tank circuit designed for each frequency limit,
7. The drift of the oscillator frequency with temperature is defined for ΔT_{amb} = 25 °C. It is measured in the application circuit (see Fig.4) with a temperature compensated tank circuit. The temperature compensation used for this measurement is done using the application which is depicted in Fig.4.
8. Measured with an input signal F_{RF} + 500 kHz (i.e.480 MHz).
9. The load should be AC coupled.

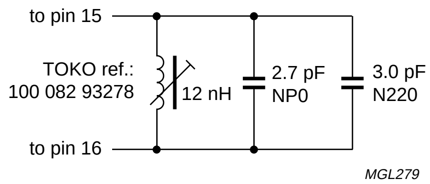


Fig.3 Temperature compensation circuit.

APPLICATION INFORMATION

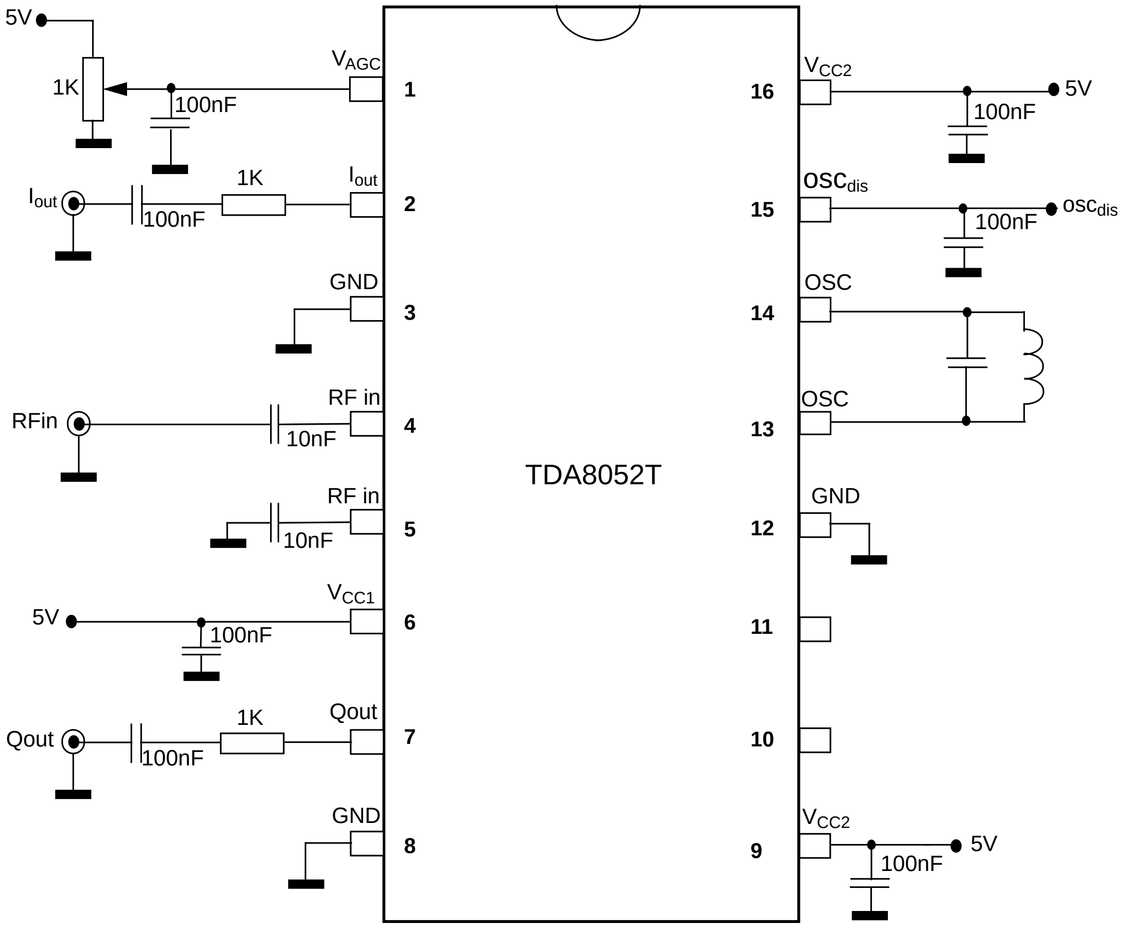
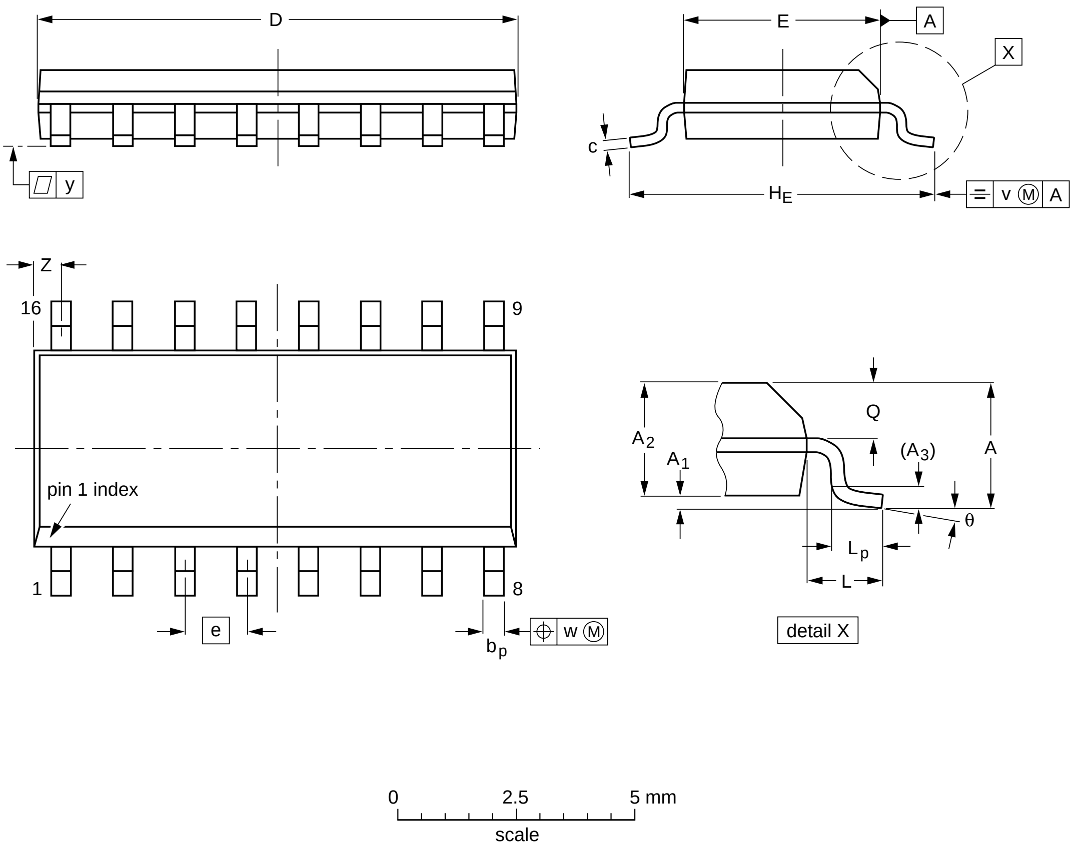


Fig.4 Typical application diagram

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^{o} 0^{o}
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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