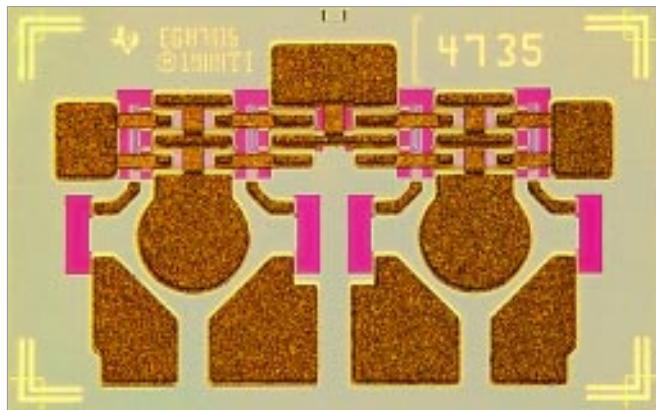


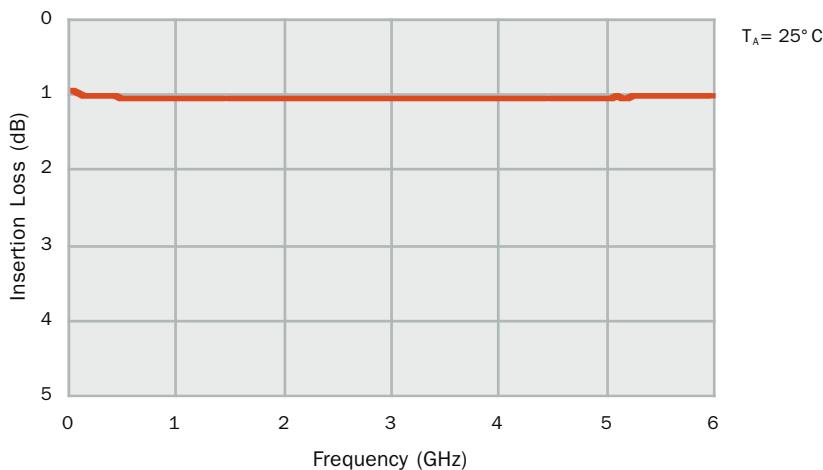
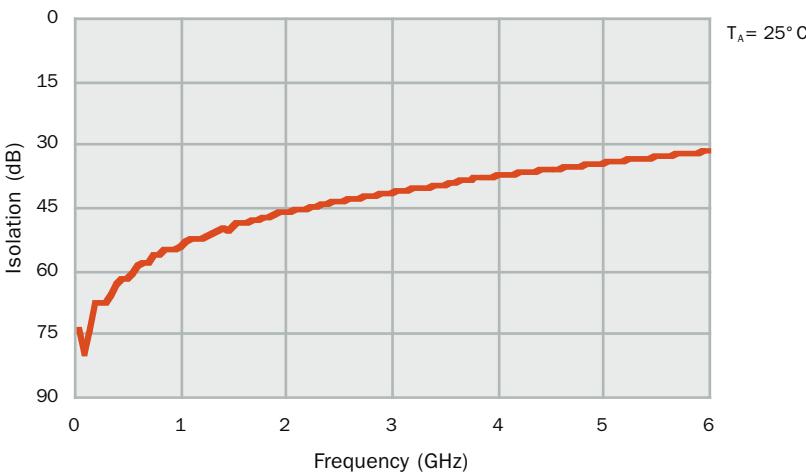
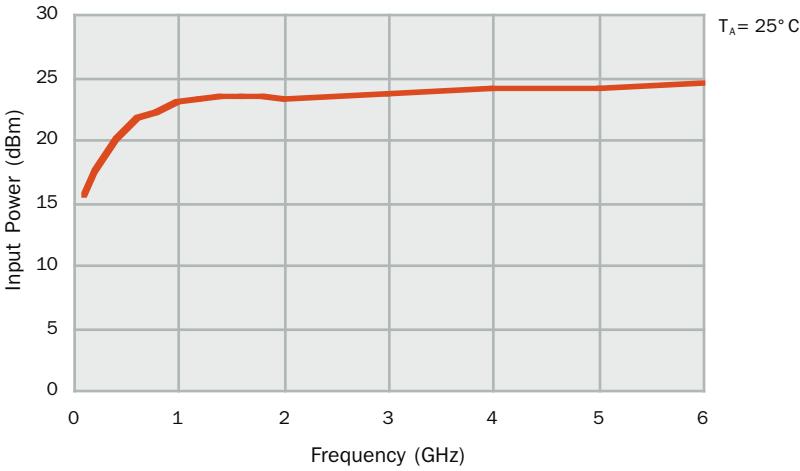
- DC to 6-GHz Frequency Range
- 1.1-dB Insertion Loss and 45-dB Isolation at Midband
- 1.2:1 Input/Output SWR
- 23-dBm Typical Input Power at 1-dB Gain Compression
- 1,066 x 0,685 x 0,152 mm (0.042 x 0.027 x 0.006 in.)

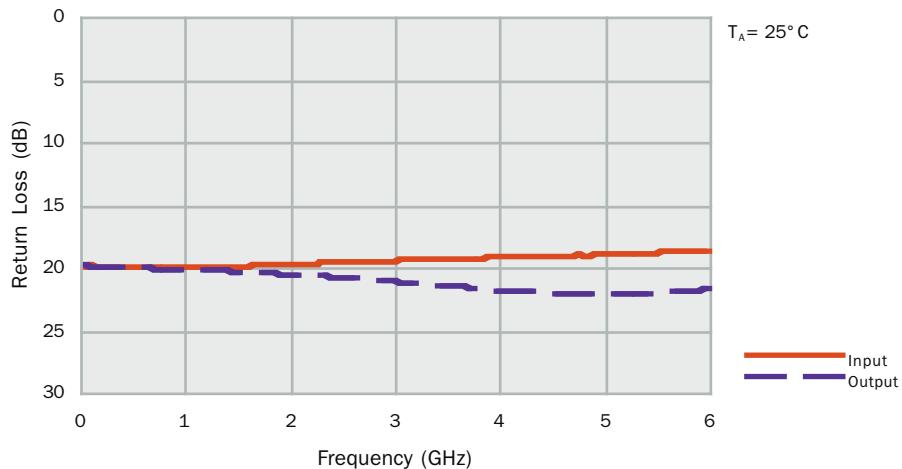
PHOTO ENLARGEMENT

DESCRIPTION

The Texas Instruments TGS8705-SCC is one of a family of low-frequency single-pole double-throw FET switches. This wideband reflective switch has low-power consumption and can be easily configured for single-pole multi-throw operation. Typical input power at 1-dB gain compression is 23-dBm. A variety of military and commercial requirements in signal modulation and processing is effectively addressed by the TGS8705-SCC.

Chip bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic-wire bonding processes. Ground is provided to the circuit through vias to the backside metallization.

**TYPICAL
INSERTION LOSS****TYPICAL
ISOLATION****TYPICAL
INPUT POWER
 P_{1dB}** 

**TYPICAL
RETURN LOSS****ABSOLUTE
MAXIMUM RATINGS**

Input continuous wave power, P_{IN}^*	1 W
Control voltage range, V_1 , V_2 , V_3 , and V_4	-10 to 0 V
Operating channel temperature, T_{CH}^{**}	150°C
Mounting temperature (30 sec), T_M	320°C
Storage temperature range, T_{STG}	-65 to 150°C

Ratings over channel temperature range, T_{CH} (unless otherwise noted)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "RF Characteristics" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

* DC blocks are not provided at RF ports.

** Operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that channel temperature be maintained at the lowest possible level.

TYPICAL S-PARAMETERS
 Low Loss Path

Frequency (GHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂		Insertion Loss (dB)
	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	
0.05	0.10	2	0.90	-1	0.90	-1	0.10	5	1.0
0.5	0.10	-1	0.89	-3	0.89	-3	0.10	-4	1.0
1.0	0.10	-1	0.88	-6	0.88	-6	0.10	-7	1.1
1.5	0.10	-2	0.88	-9	0.88	-9	0.10	-11	1.1
2.0	0.10	-3	0.88	-12	0.88	-12	0.09	-16	1.1
2.5	0.11	-5	0.88	-15	0.89	-15	0.09	-20	1.1
3.0	0.11	-8	0.89	-18	0.89	-18	0.09	-25	1.1
3.5	0.11	-12	0.89	-21	0.89	-21	0.09	-31	1.1
4.0	0.11	-17	0.89	-24	0.89	-24	0.08	-37	1.1
4.5	0.11	-22	0.89	-27	0.89	-27	0.08	-45	1.1
5.0	0.11	-29	0.89	-30	0.89	-30	0.08	-55	1.0
5.5	0.11	-36	0.89	-33	0.89	-33	0.08	-67	1.0
6.0	0.12	-43	0.89	-37	0.89	-37	0.08	-80	1.0
6.5	0.12	-51	0.89	-40	0.88	-40	0.09	-90	1.1
7.0	0.12	-61	0.89	-43	0.88	-43	0.10	-100	1.1
7.5	0.13	-71	0.89	-47	0.89	-47	0.11	-110	1.0
8.0	0.13	-83	0.88	-50	0.88	-50	0.13	-116	1.1
8.5	0.14	-94	0.88	-54	0.88	-53	0.14	-122	1.1
9.0	0.15	-105	0.88	-57	0.88	-57	0.16	-128	1.1
9.5	0.16	-114	0.87	-61	0.87	-61	0.19	-137	1.2
10.0	0.16	-120	0.86	-64	0.86	-64	0.20	-146	1.3

T_{CH} = 25°C

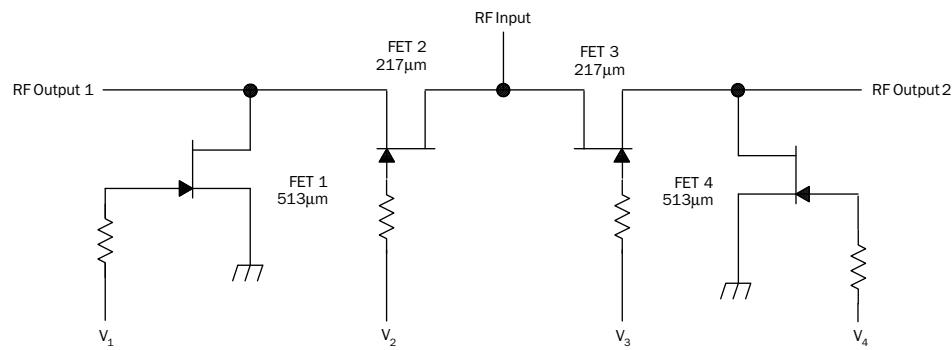
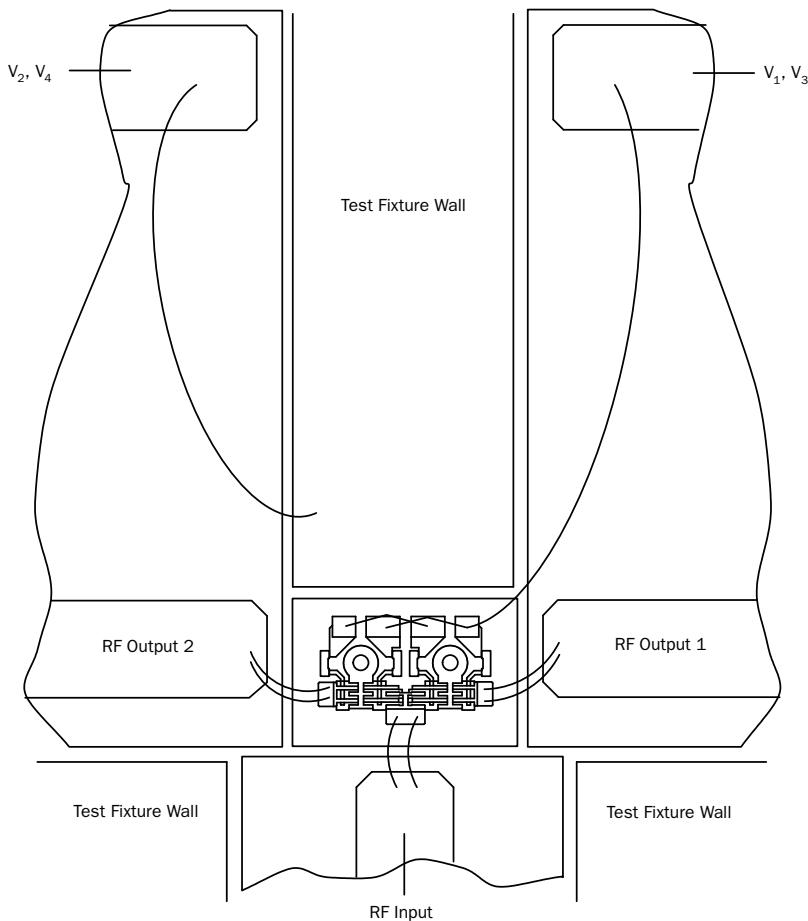
Reference planes for S-parameter data include bond wires as specified in the "Recommended Assembly Diagram". The S-parameters are also available on floppy disk and the world wide web.

TYPICAL S-PARAMETERS
 Isolated Path

Frequency (GHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂		Isolation (dB)
	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	
0.05	0.11	22	0.0002	83	0.0000	73	0.81	178	74.0
0.5	0.11	4	0.0008	102	0.0009	110	0.80	176	61.9
1.0	0.12	5	0.0019	114	0.0019	115	0.80	172	54.4
1.5	0.12	6	0.0033	120	0.0032	119	0.80	168	49.6
2.0	0.12	8	0.0048	121	0.0046	119	0.80	164	46.4
2.5	0.13	8	0.0065	125	0.0063	121	0.80	160	43.7
3.0	0.13	7	0.0083	126	0.0084	125	0.80	157	41.6
3.5	0.13	4	0.0104	128	0.0104	128	0.80	154	39.7
4.0	0.14	-1	0.0131	128	0.0128	129	0.81	150	37.7
4.5	0.14	-5	0.0156	129	0.0158	128	0.81	147	36.1
5.0	0.15	-9	0.0186	129	0.0187	129	0.81	143	34.6
5.5	0.15	-14	0.0218	130	0.0218	130	0.81	140	33.2
6.0	0.16	-19	0.0256	130	0.0254	130	0.80	138	31.8
6.5	0.16	-25	0.0300	130	0.0298	131	0.81	136	30.5
7.0	0.17	-33	0.0363	130	0.0361	131	0.82	135	28.8
7.5	0.17	-44	0.0430	126	0.0433	127	0.82	132	27.3
8.0	0.19	-56	0.0508	122	0.0511	122	0.82	129	25.9
8.5	0.22	-69	0.0630	118	0.0639	118	0.82	126	24.0
9.0	0.21	-89	0.0720	101	0.0720	101	0.81	123	22.9
9.5	0.21	-101	0.0843	86	0.0834	85	0.79	120	21.5
10.0	0.17	-106	0.0645	59	0.0631	60	0.81	120	23.8

T_{CH} = 25°C

Reference planes for S-parameter data include bond wires as specified in the "Recommended Assembly Diagram". The S-parameters are also available on floppy disk and the world wide web.

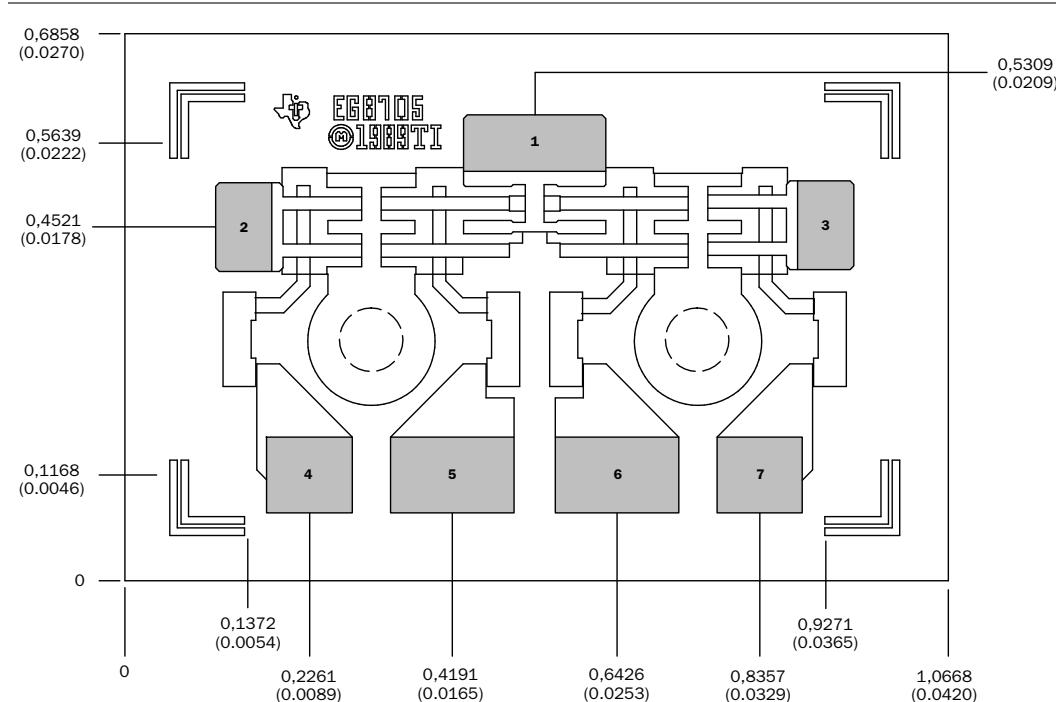
EQUIVALENT SCHEMATIC**RECOMMENDED TEST ASSEMBLY DIAGRAM**

RF connections: bond using two 1-mil diameter, 20 to 25-mil-length gold wire at both RF Input and RF Output ports for optimum RF performance.

Low-loss path is RF Input to RF Output 1 for $V_1 = -5\text{ V}$, $V_3 = 0$, $V_2 = 0$ and $V_4 = -5\text{ V}$. Low-loss path is RF Input to RF Output 2 for $V_1 = 0$, $V_3 = 0$, $V_2 = -5\text{ V}$ and $V_4 = 0$.

RF isolation will be limited by the chip operating environment.

MECHANICAL DRAWING



Units: millimeters (inches)

Thickness: 0,1524 (0.006)

Chip-edge-to-bond-pad dimensions are shown to center of bond pad.

Chip size $\pm 0,0508$ (0.0020)

Bond pad #1 (RF Input): 0,1930 x 0,0762 (0.0076 x 0.0030)

Bond pad #2 (RF Output 1): 0,0762 x 0,1194 (0.0030 x 0.0047)

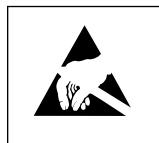
Bond pad #3 (RF Output 2): 0,0762 x 0,1194 (0.0030 x 0.0047)

Bond pad #4 (V_1): 0,1168 x 0,1016 (0.0046 x 0.0040)

Bond pad #5 (V_2): 0,1676 x 0,1016 (0.0066 x 0.0040)

Bond pad #6 (V_3): 0,1676 x 0,1016 (0.0066 x 0.0040)

Bond pad #7 (V_4): 0,1168 x 0,1016 (0.0046 x 0.0040)



This device is susceptible to damage from electric discharge. Handling and packaging of this device and/or assembly should be accomplished only with adequate provisions to prevent electrostatic discharge damage. IMPORTANT NOTICE: Export of this controlled commodity requires appropriate export license authority from the U.S. Government. © Copyright 1996. Texas Instruments Incorporated. All rights reserved.