Data Sheet
February 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7296 DS3/STS-1/E3 Integrated Line Transmitter

Features

- Fully integrated transmit interface for DS3, STS-1, or E3 applications
- Integrated pulse shaping circuit
- Intended for systems which must comply with AT&T CB119, ITU-T G.703, and ITU-T G.824, Bellcore TR-NWT-000499, ANSI T1.404
- Built-in B3ZS/HDB3 encoder and decoder
- Remote and local loopback functions
- Single 5 V power supply

Applications

- Interface for SONET, DS3, and E3 network equipment
- Digital cross connect systems
- CSU/DSU equipment
- PCM test equipment
- Fiber-optic terminals
- Multiplexers

Description

The T7296 is a fully integrated PCM line-driver IC intended for DS3 (44.736 Mbits/s), SONET STS-1 (51.84 Mbits/s), or E3 (34.368 Mbits/s) applications. The IC is designed to complement the T7295-6 DS3/SONET STS-1 or T7295-1 E3 Integrated Line Receivers. The T7296 converts input clock and dual-rail unipolar data into AMI pulses according to AT&T Technical Advisory No. 34 or ITU-T G.703 recommendations.

The device provides B3ZS (DS3) or HDB3 (E3) encoding functions for data to be transmitted to the line. A complementary decoder circuit is also included in the T7296 for decoding received signals from an external line receiver. Both encoder and decoder functions can be disabled independently with external control pins. In the receive direction, coding errors and bipolar violations are detected and flagged at an output pin.

On-chip pulse shaper circuitry eliminates the need for external components for line equalization to meet the cross connect template (DSX-3 and STSX-1). For system-level trouble shooting and testing, both transmit and receive loopbacks are possible with the built-in loopback circuit.

The T7296 is manufactured in a BiCMOS technology and is packaged in 28-pin, plastic DIP and SOJ packages. The device requires a single 5 V power supply and dissipates a maximum power of 700 mW.

Description (continued)

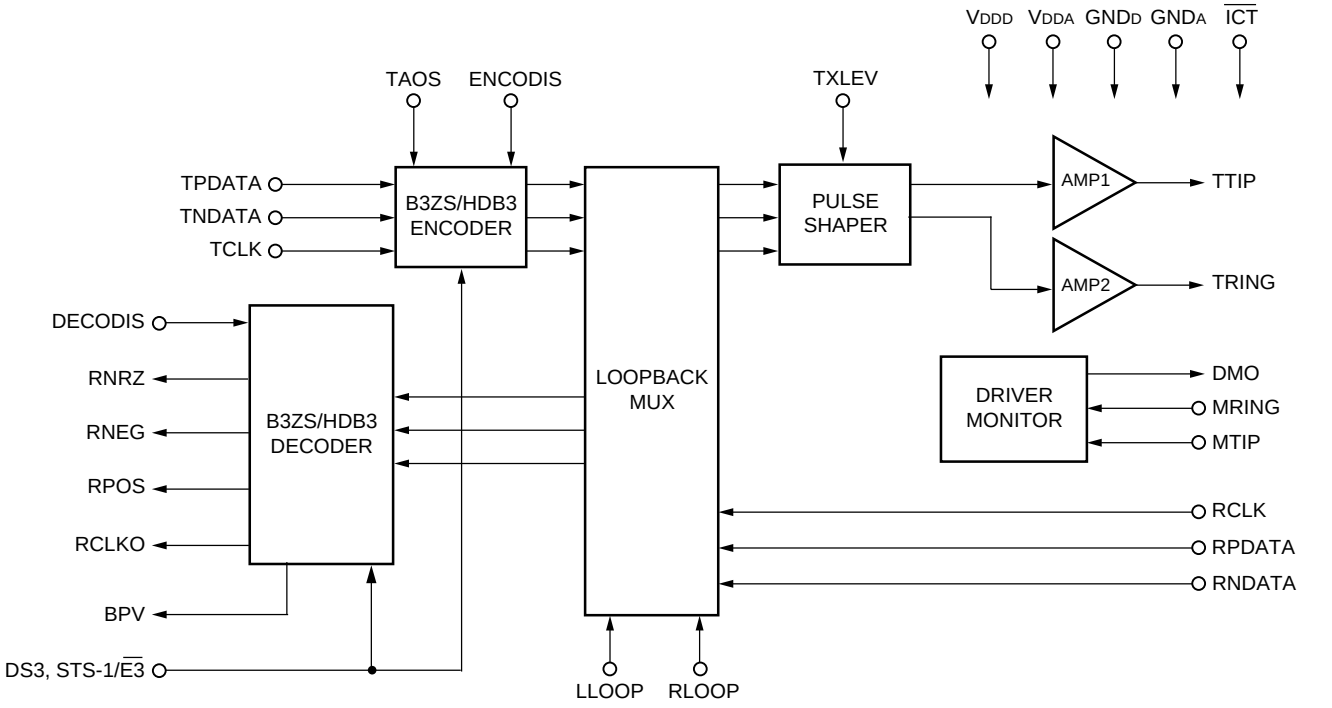

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Figure 1. Block Diagram

Pin Information

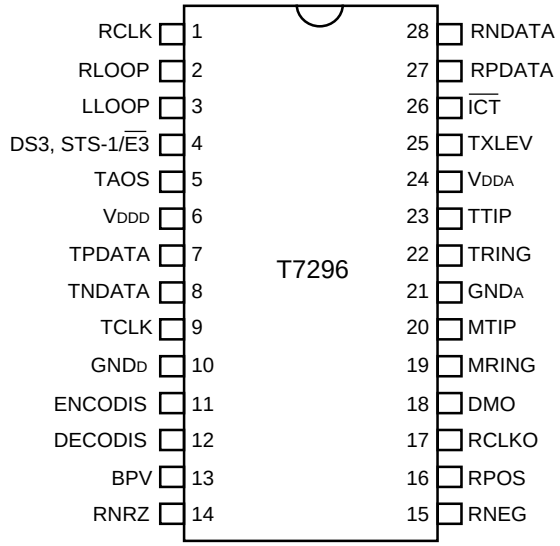

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Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	RCLK	I	**Receive Clock Input.** Input sampling clock for RPDATA and RNDATA.
2	RLOOP	I	**Remote Loopback.** A high on this pin causes RPDATA and RNDATA to be transmitted to the line using RCLK. Setting LLOOP and RLOOP high simultaneously is not permitted.
3	LLOOP	I	**Local Loopback.** A high on this pin causes TPDATA and TNDATA to pass through the encoder and output at RPOS and RNEG, respectively. Setting LLOOP and RLOOP high simultaneously is not permitted.
4	DS3, STS-1/$\overline{E3}$	I	**DS3, STS-1, or $\overline{E3}$ Select.** A high on this pin selects DS3 or STS-1 operation and sets the encoder and decoder in B3ZS mode. A low selects E3 operation and sets the encoder and decoder in HDB3 mode.
5	TAOS	I	**Transmit All 1s Select.** A high on this pin causes a continuous AMI all-1s pattern to be transmitted to the line. The frequency is determined by TCLK.
6	V_{DDD}	—	**5 V Digital Supply (±5%).** For all logic circuitry.
7	TPDATA	I	**Transmit Positive Data.** TPDATA is sampled on the falling edge of TCLK. Pins 7 and 8 can be tied together for binary input signals.
8	TNDATA	I	**Transmit Negative Data.** TNDATA is sampled on the falling edge of TCLK. Pins 7 and 8 can be tied together for binary input signals.
9	TCLK	I	**Transmit Clock for TPDATA and TNDATA.**
10	GND_D	—	**Digital Ground.** For all logic circuitry.
11	ENCODIS	I	**Encoder Disable.** A high on this pin disables B3ZS or HDB3 encoding functions, unless overridden by a TAOS request. Set ENCODIS high if TPDATA and TNDATA are already encoded.
12	DECODIS	I	**Decoder Disable.** A high on this pin disables B3ZS or HDB3 decoding functions.
13	BPV	O	**Bipolar Violation Output.** This pin goes high for one bit period when a bipolar violation or a coding error not corresponding to the appropriate coding rule is detected in the RPDATA/RNDATA signals.
14	RNRZ	O	**Receive Binary Data.** The signal on this pin is the ORed-output of RPOS and RNEG.
15	RNEG	O	**Receive Negative Data.** This signal is the decoded version of RNDATA.*
16	RPOS	O	**Receive Positive Data.** This signal is the decoded version of RPDATA.*
17	RCLKO	O	**Receive Clock Output.** This signal is the inverted version of RCLK.
18	DMO	O	**Driver Monitor Output.** If no transmitted AMI signal is present on MTIP and MRING for 128 ± 32 TCLK clock periods, DMO goes high until the next AMI signal is detected.
19	MRING	I^u	**Monitor Ring Input.** AMI signal from TRING can be connected to this pin for line driver failure detection. Internally pulled high.
20	MTIP	I^u	**Monitor Tip Input.** AMI signal from TTIP can be connected to this pin for line driver failure detection. Internally pulled high.
21	GND_A	—	**Analog Ground.** For analog circuitry.
22	TRING	O	**Transmit Ring Output.** Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
23	TTIP	O	**Transmit Tip Output.** Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
24	V_{DDA}	—	**5 V Analog Supply (±5%).** For analog circuitry.

* If a bipolar violation occurs, RPOS and RNEG can correspond to decoded versions of RPDATA and RNDATA, respectively. If DECODIS is high, RPOS and RNEG always track RPDATA and RNDATA, respectively.

Note: Pins with the I^u designation have an internal pull-up.

Pin Information (continued)

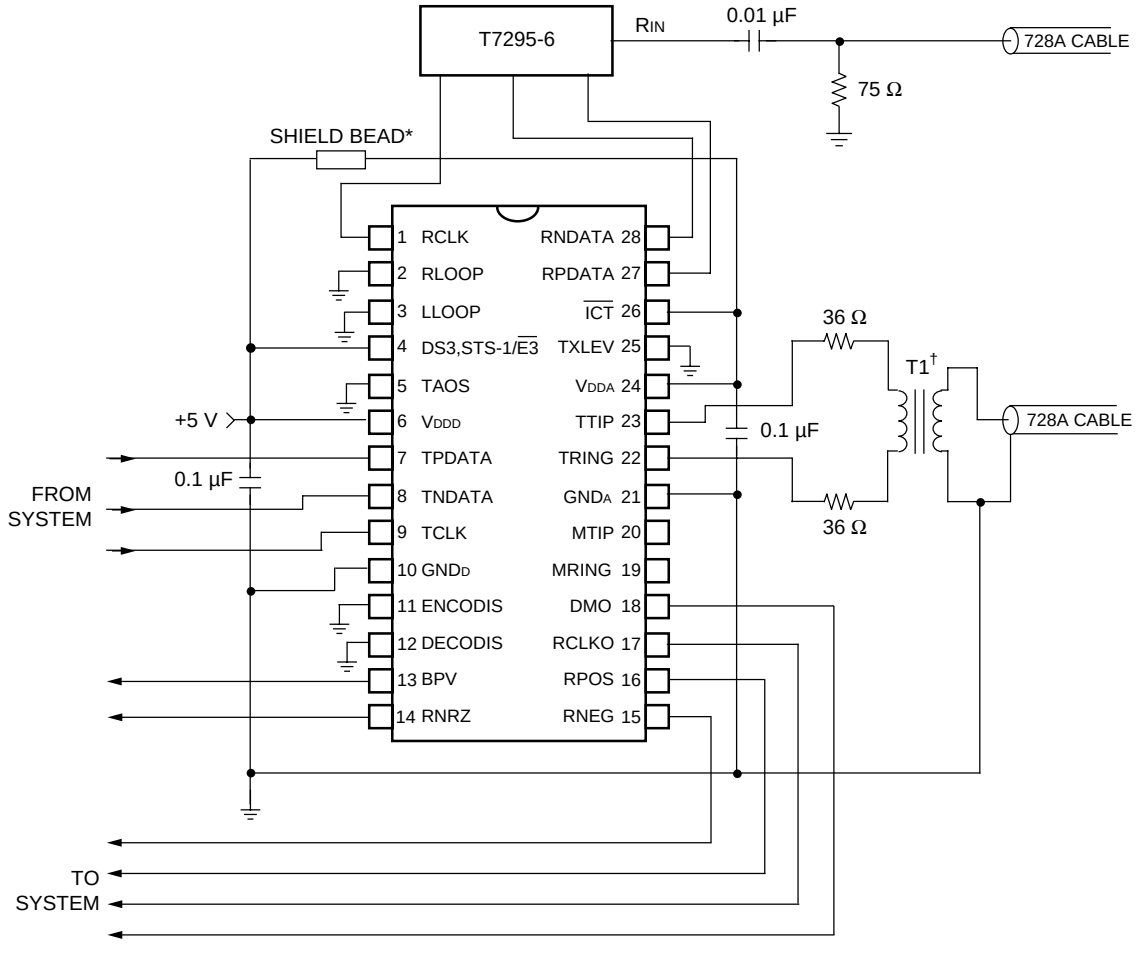
Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
25	TXLEV	I	**Transmit Level Select.** The output signal amplitude at TTIP and TRING can be varied by setting this pin high or low. When the cable length is greater than 225 ft., TXLEV should be set high. When it is below 225 ft., it should be set low. This pin is active only when the DS3, STS-1/$\overline{E3}$ input (pin 4) is set high (DS3, STS-1 mode).
26	$\overline{ICT}$	I^u	**In-Circuit Testing (Active-Low).** A low at this pin causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. Internally pulled high.
27	RPDATA	I	**Receive Positive Data.** NRZ input data to the decoder block. Sampled on the falling edge of RCLK.
28	RNDATA	I	**Receive Negative Data.** NRZ input data to the decoder block. Sampled on falling edge of RCLK.

* If a bipolar violation occurs, RPOS and RNEG can correspond to decoded versions of RPDATA and RNDATA respectively. If DECODIS is high, RPOS and RNEG always track RPDATA and RNDATA, respectively.

Note: Pins with the I^u designation have an internal pull-up.

Overview



* Shield bead is the *FairRite*‡ 2643000101 or equivalent.
† Output transformer *Pulse Engineering*§ PE-65966 (through-hole) or PE-65967 (surface mount) or equivalent.
‡ *FairRite* is a registered trademark of FairRite Products Corporation.
§ *Pulse Engineering* is a registered trademark of Pulse Engineering, Inc.

Note: Lucent Technologies does not endorse the use of or assume liability for the use of any bead or transformer.

Figure 3. T7296 Application DS3 Mode, Less Than 225 Feet of Cable

Overview (continued)

System Description

B3ZS/HDB3 Encoder

Data to be transmitted is input to the encoder block to be encoded either in B3ZS or HDB3 as determined by the state of the DS3, STS-1/$\overline{E3}$ pin. Input data format can be unipolar or binary. For binary signals, TPDATA and TNDATA need to be connected together externally. The line code used for DS3 is B3ZS. In this mode, each block of three consecutive zeros is removed and replaced by one of two codes that contain bipolar violations. These replacement codes are B0V and 00V, where B indicates a pulse conforming with the bipolar rule, and V represents a pulse violating the rule. The choice of these codes is made such that an odd number of B pulses will be transmitted between consecutive bipolar violation (BPV) pulses. For E3 format, the line code is HDB3. The encoding rule of HDB3 is similar to B3ZS except that the number of consecutive zeros is increased to four before a code replacement can take place. The replacement codes in this case are 000V and B00V.

STS-1 operation is achieved by placing the part in the DS3 mode and using 51.84 MHz clocks. Logic operation for STS-1 is the same for DS3.

Transmit All 1s Select

Setting TAOS high causes continuous AMI encoded 1s to be transmitted to the line. In this mode, input TPDATA and TNDATA are ignored. If remote loopback (RLOOP) is set high, any TAOS request is ignored.

Remote Loopback

Setting RLOOP high causes received RPDATA and RNDATA to be transmitted to the line through TTIP and TRING. The data rate is determined by RCLK. In this mode, TPDATA and TNDATA are ignored.

Local Loopback

Setting LLOOP high causes TPDATA and TNDATA to go through both the encoder and the decoder. In this mode, the signals transmitted on RCLKO, RPOS, and RNEG correspond to those received on TCLK, TPDATA, and TNDATA, respectively. TPDATA and TNDATA are transmitted to the line unless overridden by a TAOS request. Setting both RLOOP and LLOOP high simultaneously is not permitted.

B3ZS/HDB3 Decoder

The decoder block is included to perform B3ZS or HDB3 decoding as determined by the state of the DS3, STS-1/$\overline{E3}$ pin. In the B3ZS format, the decoder detects both B0V and 00V codes and replaces them with 000 data. If HDB3 decoding is selected by setting the DS3, STS-1/$\overline{E3}$ pin low, the B00V and 000V codes are detected and replaced with the 0000 code. In both cases, bipolar violation and coding errors that do not conform to the coding scheme are detected and indicated at the BPV output pin.

Decoder Disable

For testing purposes and in applications where the decoder needs to be bypassed, the decoder can be disabled by setting DECODIS high. In this mode, all bipolar violation pulses are indicated at the BPV pin.

Bipolar Violation Detection

The BPV pin goes high for one bit period when a code error or a bipolar violation not corresponding to the appropriate coding rule is detected on the RPDATA/RNDATA signal. The violation pulse is always removed from the decoder outputs RPOS/RNEG when DECODIS is set low.

Pulse Shaper

The pulse shaper circuit uses a combination of filters and slew-rate control techniques to preshape the pulse to be transmitted to the line. The amplitude of the transmit pulse can be adjusted by using the TXLEV (transmit level) pin. When the distance to the cross connect exceeds 225 ft., TXLEV should be set high. When the distance is less than 225 ft., TXLEV should be set low. Setting TXLEV high enables the transmitter to send out a nominal 1.0 V peak pulse. Setting TXLEV low enables the transmitter to send out a nominal 850 mV peak pulse. The state of the TXLEV pin has no effect on E3 operation.

Driver Monitor

Using TTIP and TRING as inputs, the driver monitor detects driver failure by monitoring the activities at MTIP and MRING. If no signal is detected on these pins for 128 ± 32 TCLK cycles, DMO is set high until the next AMI signal is detected.

DS3 Signal Requirements at the DSX

For DS3 operation, pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the cross connect. The cross connect exists at the point where the transmitted signal reaches the distribution frame jack. The T7296 can transmit through 450 ft. of 728A cable to the DSX-3 in DS3 mode. Table 2 lists the signal requirements.

Currently, two isolated pulse template requirements exist: the ANSI TI.404 pulse template (see Table 3 and Figure 4) and the Bellcore TR-NWT-000499 pulse template (see Table 4 and Figure 5). The pulse transmitted by the T7296 meets these templates.

Table 2. DSX-3 Interconnection Specification

Parameter	Specification
Line Rate	44.736 Mbits/s ± 20 ppm.
Line Code	Bipolar with three-0 substitution (B3ZS).
Test Load	75 Ω ± 5%.
Pulse Shape	An isolated pulse must fit the template in Figure 4 or Figure 5.* The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36 V pk and 0.85 V pk, measured at the center of the pulse.
Power Levels	For an all-1s transmitted pattern, the power at 22.368 MHz ± 0.002 MHz must be –1.8 dBm to +5.7 dBm, and the power at 44.736 MHz ± 0.002 MHz must be –21.8 dBm to –14.3 dBm.†‡

* The pulse template in G.703 is shown in Figure 5 and specified in Table 4. The proposed G.703 further states that the voltage in a time slot containing a zero must not exceed ±5% of the peak pulse amplitude, except for the residue of preceding pulses.
† The power levels specified by the proposed G.703 are identical except that the power is to be measured in 3 kHz bands.
‡ The all-1s pattern must be a pure all-1s signal, without framing or other control bits.

Table 3. DSX-3 Pulse Template Boundaries for ANSI TI.404 (See Figure 4.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$T \le -0.36$	–0.03	$T \le -0.68$	+0.03
$-0.36 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T$	–0.03	$+0.36 \le T$	$0.05 + 0.407e^{-1.84[T - 0.36]}$

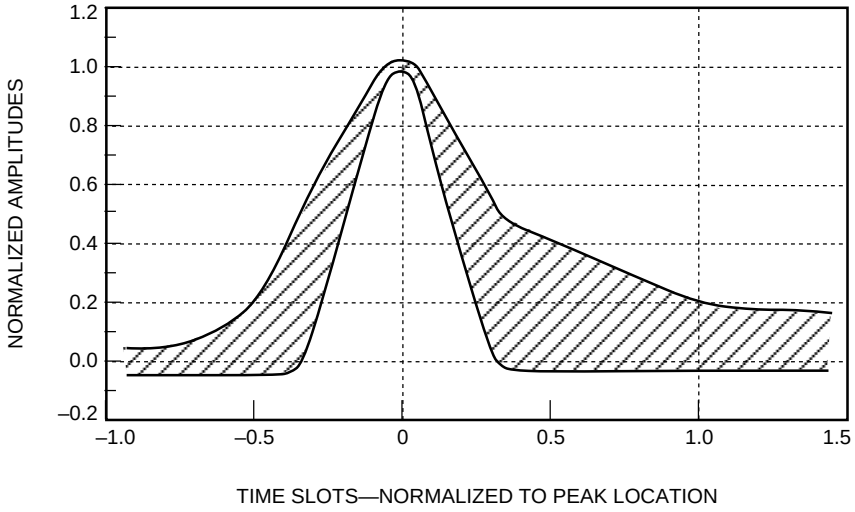


Figure 4. DSX-3 Isolated Pulse Template for ANSI T1.404

DS3 Signal Requirements at the DSX (continued)

Table 4. DSX-3 Pulse Template Boundaries for Bellcore TR-NWT-000499 (See Figure 5.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$-0.85 \le T \le -0.36$	-0.03	$-0.85 \le T \le -0.68$	$+0.03$
$-0.36 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T \le +1.4$	-0.03	$+0.36 \le T \le +1.4$	$0.08 + 0.407e^{-1.84[T - 0.36]}$

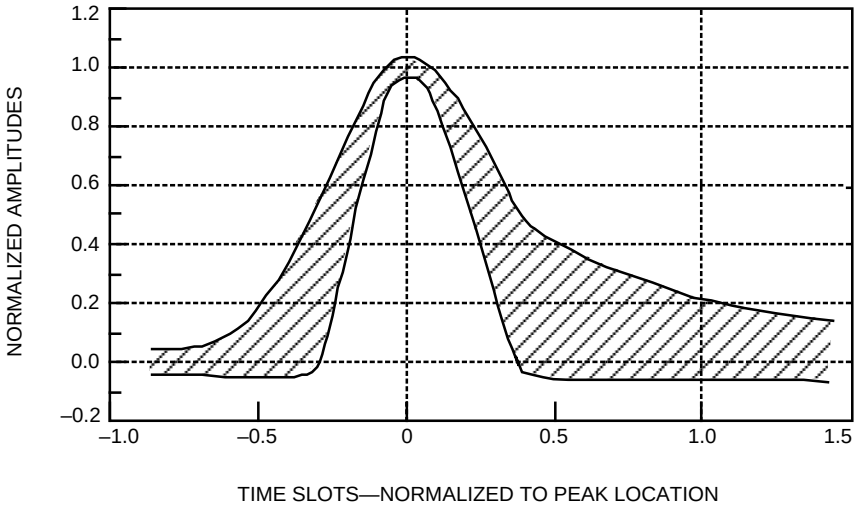


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Figure 5. DSX-3 Isolated Pulse Template for Bellcore TR-NWT-000499

STS-1 Signal Requirements at the STSX-1

For STS-1 operation, pulse characteristics are specified at the STSX-1, which is an interconnection and test point referred to as the cross connect. The cross connect exists at the point where the transmitted signal reaches the distribution frame jack. The T7296 can transmit through 450 ft. of 728A cable to the STSX-1 in STS-1 mode. An isolated pulse template is specified per ANSI T1.102 standards (see Figure 6). The pulse transmitted by the T7296 meets this template.

Table 5. STSX-1 Interconnection Specification

Parameter	Specification
Line Rate	51.84 Mbits/s.
Line Code	Bipolar with three-0 substitution (B3ZS).
Test Load	75 Ω ± 5%.
Power Levels	A wide-band power level measurement at the STSX-1 interface using a low-pass filter with a 3 dB cutoff frequency of at least 200 MHz is within –2.7 dBm and 4.7 dBm.

Table 6. Pulse Template Boundaries for ANSI T1.102 (See Figure 6.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$-0.85 \le T \le -0.38$	-0.03	$-0.85 \le T \le -0.68$	$+0.03$
$-0.38 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T \le +1.4$	-0.03	$+0.26 \le T \le +1.4$	$0.1 + 0.61e^{-2.4[T - 0.26]}$

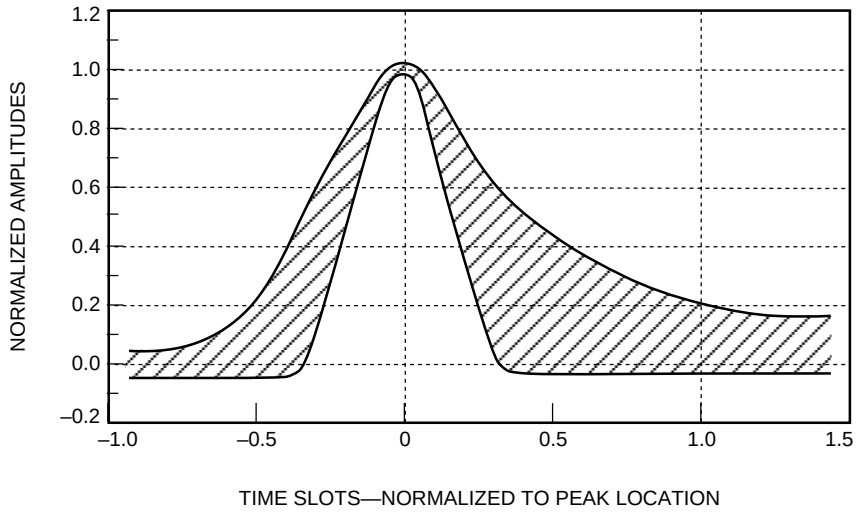

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Figure 6. STSX-1 Isolated Pulse Template for ANSI T1.102

E3 Signal Requirements

For E3 operation, pulse characteristics are defined below. Table 6 lists the signal requirements, and Figure 7 illustrates the isolated pulse template requirements as specified in the ITU-T recommendation G.703. The pulse transmitted by the T7296 meets this template.

Table 7. E3 Pulse Specifications

Parameter	Value
Pulse Shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 7), regardless of the sign.
Test Load Impedance	75 Ω resistive.
Nominal Peak Voltage of a Mark (pulse)	1.0 V.
Peak Voltage of a Space (no pulse)	0 V ± 0.1 V.
Nominal Pulse Width	14.55 ns.
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of a Pulse Interval	0.95 to 1.05.
Ratio of the Widths of Positive and Negative Pulses at Nominal Half-Amplitude	0.95 to 1.05.

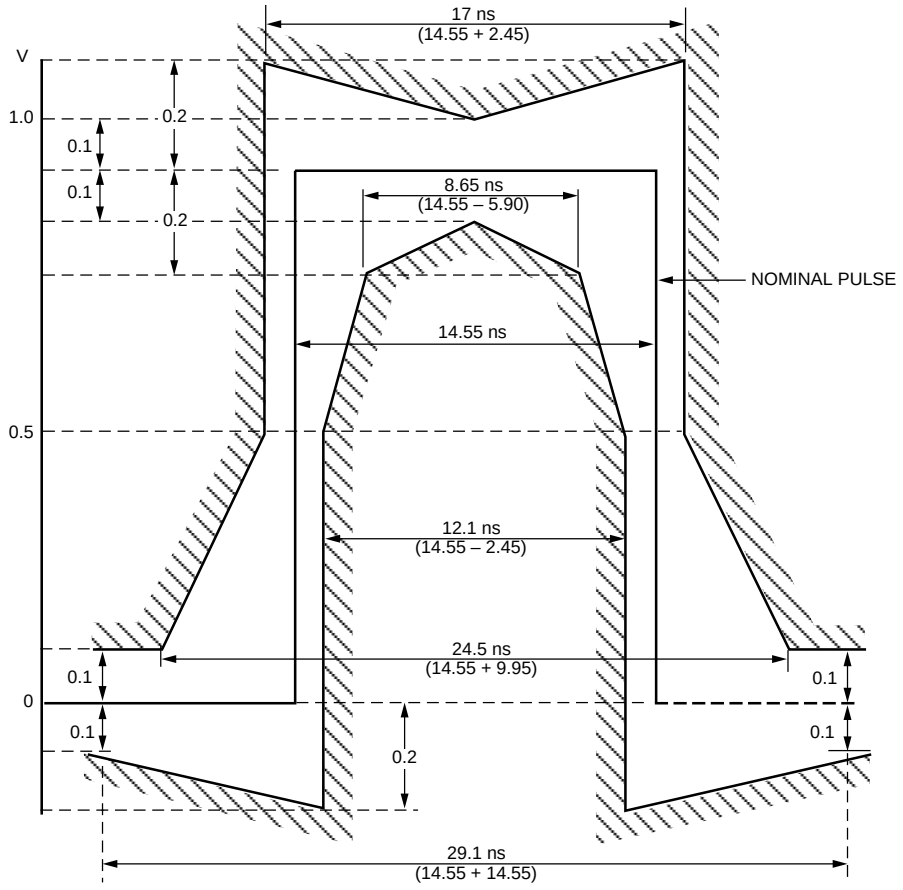

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Figure 7. Isolated E3 Pulse Template for G.703 Standards

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply	V_{DD}	–0.5	6.5	V
Storage Temperature	T_{stg}	–65	150	°C
Power Dissipation Plastic SOJ Package	P_{diss}	—	725	mW
Power Dissipation Plastic DIP Package	P_{diss}	—	1	W
Input Voltage (any pin)	—	–0.5	V_{DD} + 0.5	V
Input Current (any pin)	—	—	10	mA

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely accepted and can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	**Voltage**
T7296	>2000 V

Electrical Characteristics

Test conditions: V_{DD} = 5 V ± 5%, T_A = –40 °C to +85 °C, unless otherwise specified.

Table 8. dc Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
dc Supply Voltage	V_{DDD}, V_{DDA}	4.75	5	5.25	V
Supply Current*	—	—	—	133	mA
Input Low Voltage	V_{IL}	0	—	0.5	V
Input High Voltage	V_{IH}	0.7V_{DDD}	—	V_{DDD}	V
Output Low Voltage: Iout –4.0 mA	V_{OL}	GND_D	—	0.4	V
Output High Voltage: Iout 3.0 mA	V_{OH}	V_{DDD} – 0.5	—	V_{DDD}	V
Input Leakage Current (all pins except MRING, MTIP, and $\overline{ICT}$)	I_L	—	—	±10	µA
Input Leakage Current (MRING, MTIP, and $\overline{ICT}$ pins at 0 V)	I_L	–50	—	–150	µA
Input Capacitance	C_I	—	—	10	pF
Load Capacitance	C_L	—	—	10	pF

* Supply current is measured with transmitter sending an all-1s AMI signal and with transmit level (TXLEV) set high.

Timing Characteristics

Test conditions: V_{DD} = 5 V ± 5%, T_A = –40 °C to +85 °C unless otherwise specified. All timing characteristics are measured with 10 pF loading.

Table 9. Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
—	TCLK Clock Duty Cycle (DS3/STS-1)	45	50	55	%
—	TCLK Clock Duty Cycle (E3)	47	50	53	%
tR	TCLK Clock Rise Time (10% to 90%)	—	—	4.0	ns
tF	TCLK Clock Fall Time (90% to 10%)	—	—	4.0	ns
tTSU	Setup Time: TPDATA/TNDATA to TCLK Falling	4.0	—	—	ns
tTHO	Hold Time: TCLK Falling to TPDATA/TNDATA	5.0	—	—	ns
tTDY	Propagation Delay: TCLK Rising to TTIP/TRING*	0.6	—	14	ns
—	RCLK Clock Duty Cycle	45	50	55	%
tR	RCLK Clock Rise Time (10% to 90%)	—	—	4.0	ns
tF	RCLK Clock Fall Time (90% to 10%)	—	—	4.0	ns
tRSU	Setup Time: RPDATA/RNDATA to RCLK Falling	4.0	—	—	ns
tRHO	Hold Time: RCLK Falling to RPDATA/RNDATA	5.0	—	—	ns
tR	RCLKO Clock Rise Time (10% to 90%)	—	—	4.0	ns
tF	RCLKO Clock Fall Time (90% to 10%)	—	—	4.0	ns
tRDY	Propagation Delay: RCLKO Rising to RPOS/RNEG/RNRZ†	—	—	4.0	ns

* When the encoder is enabled, a handling delay of four and a half TCLK clock cycles for B3ZS and five and a half clock cycles for HDB3 always exists between TPDATA/TNDATA and TTIP/TRING. The handling delay is reduced to two clock cycles when the encoder is disabled.

† When the decoder is enabled, a handling delay of six and a half RCLK clock cycles always exists between RPDATA/RNDATA and RPOS/RNEG/RNRZ. The handling delay is reduced to one and a half RCLK clock cycles when the decoder is disabled.

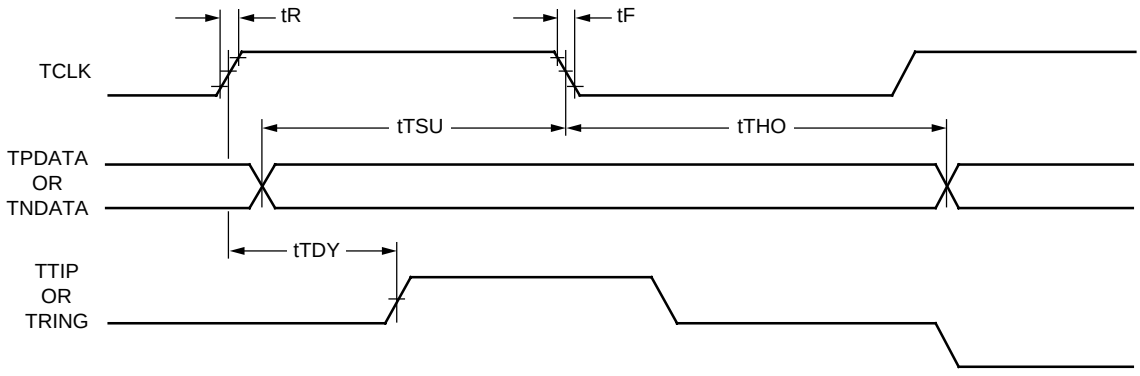

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Figure 8. Transmit System-Side Timing Diagram

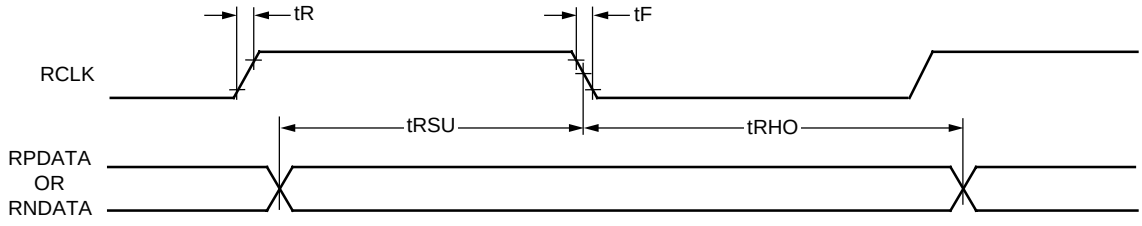

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Figure 9. Receive Line-Side Timing Diagram

Timing Characteristics (continued)

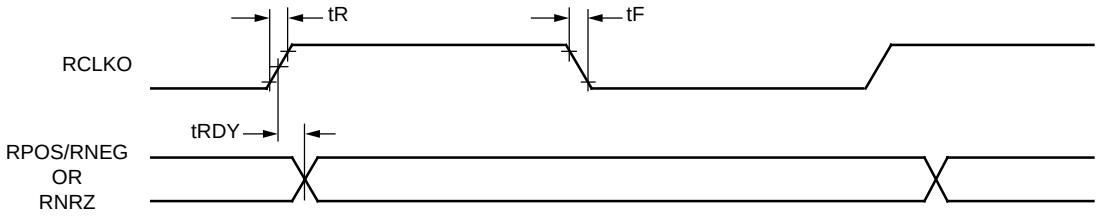

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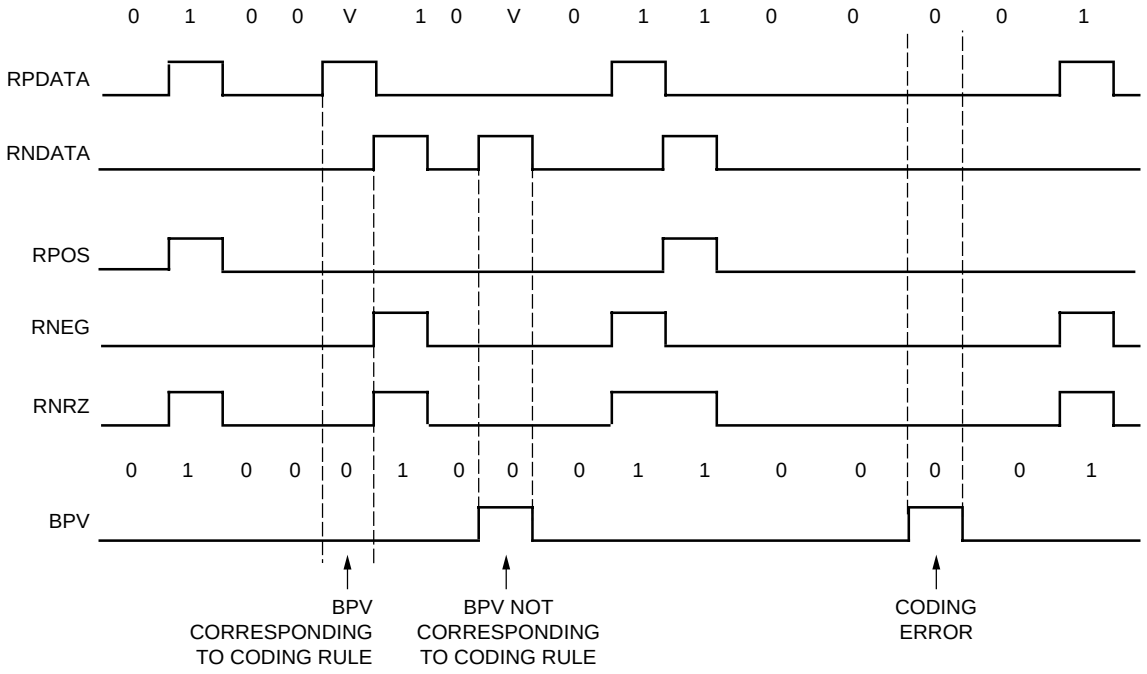
Figure 10. Receive System-Side Timing Diagram



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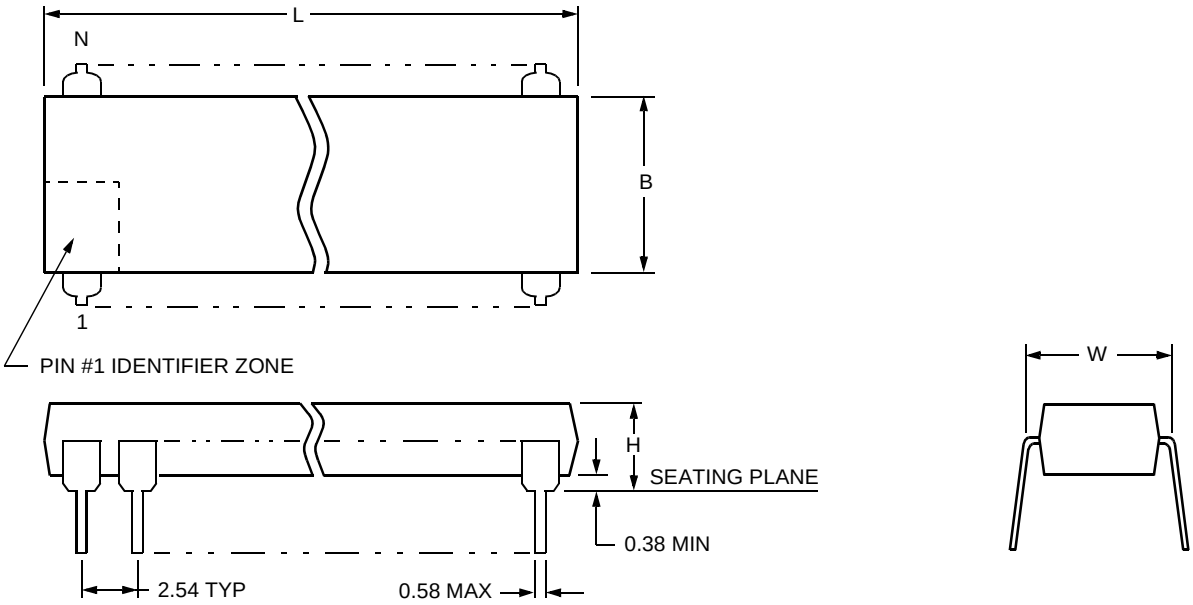
Note: The delay from RPDATA/RNDATA to RPOS/RNEG/RNRZ is not shown in this figure.

Figure 11. Example of Bipolar Violations for B3ZS Mode

Outline Diagrams

28-Pin, Plastic DIP

Dimensions are in millimeters.



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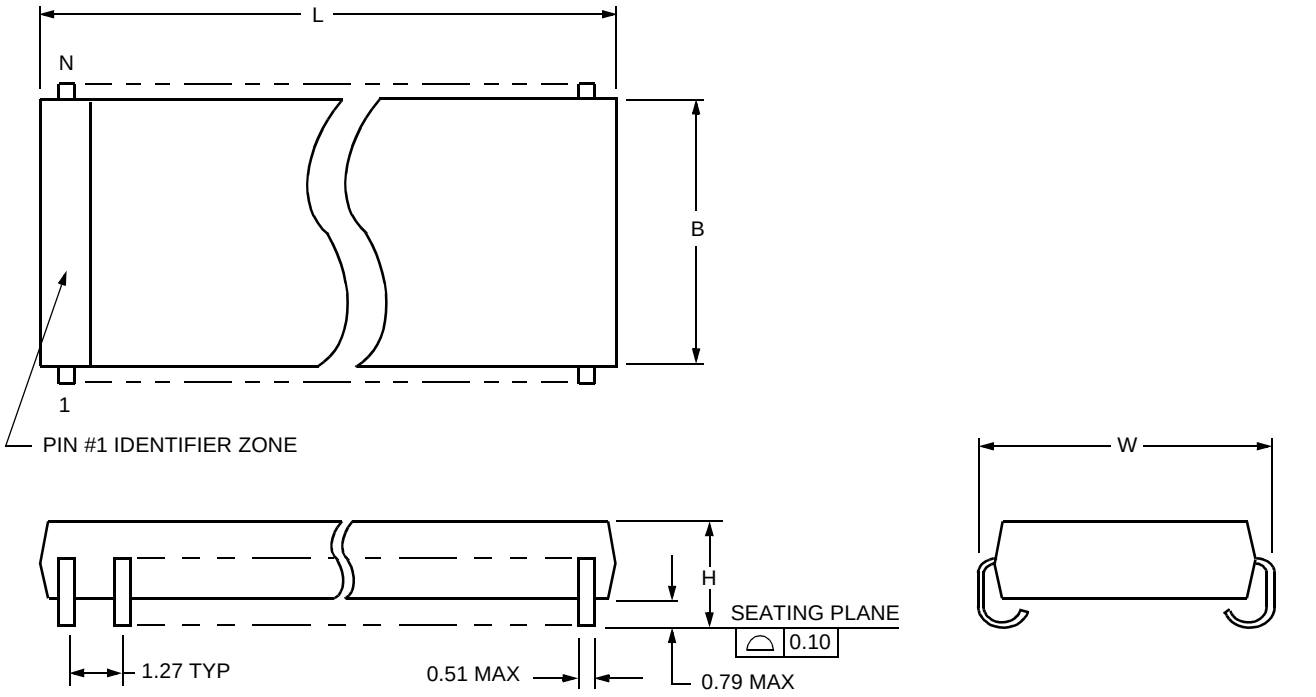
Number of Pins (N)	Package Dimensions (DIP)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	37.34	13.97	15.49	5.59

Outline Diagrams (continued)

28-Pin, Plastic SOJ

Dimensions are in millimeters.



5-4413.R4

Number of Pins (N)	Package Dimensions (SOJ)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	18.03	7.62	8.81	3.18

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7296 - - - EL	28-Pin, Plastic SOJ	–40 °C to +85 °C	106932056
T - 7296 - - - PL	28-Pin, Plastic DIP	–40 °C to +85 °C	106932064

Standards Documentation

Telecommunication technical standards and reference documentation may be obtained from the following sources:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, NY 10036

Tel: 212-642-4900
FAX: 212-302-1286

AT&T Publications:

AT&T Customer Information Center (CIC)

Tel: 800-432-6600
FAX: 800-566-9568 (in U.S.A.)
317-322-6484 (outside U.S.A.)

Bellcore (U.S.A.):

Bellcore Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (in U.S.A.)
Tel: 908-699-5800
FAX: 908-336-2559

ITU-T

International Telecommunication Union-Telecommunication Sector

Place des Nations
CH 1211
Geneve 20, Switzerland
Tel: 41-22-730-5285
FAX: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
FAX: 81-3-3432-1553

DS00-143PDH Replaces DS97-039TIC to Incorporate the Following Updates

1. Page 4, In pin description for TXLEV and Figure 3 changed 120 ft. to 225 ft.
2. Page 5, Pulse Shaper section, changed 120 ft. to 225 ft.
3. Page 14, Ordering Information section, corrected number of pins for the plastic DIP package to 28.

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ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

February 2000
DS00-143PDH (Replaces DS97-039TIC)