

Description

The TMPR3904F is a 32-bit RISC micro controller of the TX39 family. The TMPR3904F uses the TX39/H Processor Core as the CPU, which is a RISC CPU core Toshiba developed based on the MIPS® R3000A architecture. The TMPR3904F has built-in peripheral circuits such as DRAM and ROM Memory Controllers, DMA Controllers, Serial and Parallel Communication Ports, and Timer/Counter implementations.

The TX39/H core and added Direct Memory Access Controller (DMAC) features of this chip allow the transfer of data to and from system memory with high performance.

Microprocessor Features

- Built-in TX3900 Processor Core
 - Developed based on the R3000A architecture
 - Instruction cache 4KB and Data cache 1KB
 - Built-in Debug Support Unit (DSU)
 - Five-stage pipeline: Fetch, Decode, Execute, Memory access, and Register write
 - Incorporates single cycle 32-bit DSP function Multiply-Accumulate (MAC) instruction
- Power Supply: $V_{DD} = 3.3V \pm 0.3V$
- Maximum Operating Frequency: 50MHz
- Package: 208 pin plastic QFP

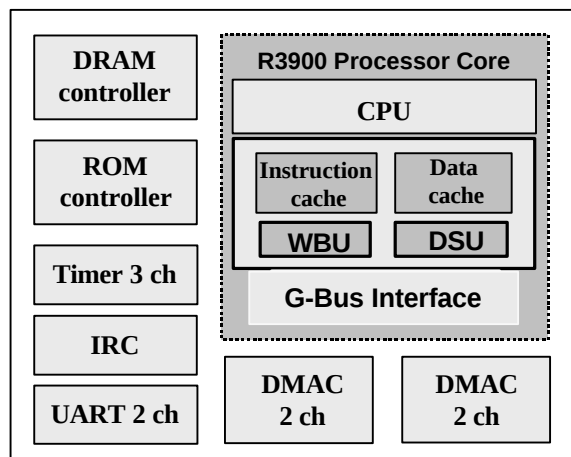


Figure 1. TMPR3904F Simplified Block Diagram

Peripheral Features

- DRAM Controller
 - Supports 2 channels of DRAM memories
 - Each channel supports up to four banks of memory
 - Independent memory size and timing set-up for each channel
 - Support of 32/ 16-bit static bus sizing
 - Supports both fast and hyper page EDO modes
- ROM Controller
 - Supports 2 channels of ROM controller
 - Supports page mode ROM support
 - Supports various memory size of 1M/2M/4M/8M/16M/32M byte per channel
 - Supports 32/16-bit static bus sizing
 - Supports Mask ROM, EPROM, E²PROM, SRAM, and Flash Memory
- Timer/Counter
 - 3-channel 24-bit up-counter
 - Interval, Watchdog, and Pulse Generator timer modes
- Serial I/O Ports
 - Two-channel UART
 - Baud rate generator and modem flow control
- Interrupt Controller
 - Priority process of 17 interrupt sources: nine internals, eight externals
 - Non-maskable Interrupt (NMI)
- Direct Memory Access Controller (DMAC)
 - Independent 2-channel DMA
 - Supports both with and without snoop bus ownership requests
 - Supports memory-to-memory, memory-to-I/O, and I/O-to-memory transfer devices
 - Supports Internal/External transfer requests
 - Supports both Dual Address and Single Address transfer modes
 - Supports device sizes of: 32-bit memory; 8, 16, or 32-bit I/O
- Parallel I/O (PIO) Ports
 - Three 8-bit ports (one exclusive, two shared)

Table 1. Pin Assignment

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	XIN	29	VSS	57	A[19]	85	TSTO1
2	VDD	30	TOUT[2]	58	A[20]	86	BOOT16
3	LAST*	31	TOUT[3]	59	A[21]	87	HALF*
4	R/W*	32	WE*	60	VSS	88	ENDIAN
5	BE[3]*	33	A[1]	61	VDD	89	BUSGNT*
6	BE[2]*	34	VDD	62	A[22]	90	BUSREL*
7	BE[1]*	35	A[2]	63	A[23]	91	DACK[0]
8	BE[0]*	36	A[3]	64	A[24]	92	DACK[1]
9	VSS	37	A[4]	65	A[25]	93	DACK[2]
10	VDD	38	VSS	66	A[26]	94	DACK[3]
11	RAS0[0]*	39	A[5]	67	A[27]	95	DONE*
12	RAS0[1]*	40	A[6]	68	VSS	96	VSS
13	RAS0[2]*	41	A[7]	69	VDD	97	VDD
14	VDD	42	A[8]	70	A[28]	98	DREQ[0]
15	VSS	43	VDD	71	A[29]	99	DREQ[1]
16	RAS0[3]*	44	VSS	72	A[30]	100	DREQ[2]
17	RAS1[0]*	45	A[9]	73	A[31]	101	DREQ[3]
18	RAS1[1]*	46	A[10]	74	CE0[0]*	102	HAVEIT
19	VSS	47	A[11]	75	CE0[1]*	103	BUSREQ*
20	RAS1[2]*	48	A[12]	76	CE1[0]*	104	VDD
21	RAS1[3]*	49	A[13]	77	CE1[1]*	105	SCS[3]*
22	CAS[0]*	50	A[14]	78	OE1*	106	SCS[2]*
23	CAS[1]*	51	A[15]	79	VSS	107	SCS[1]*
24	VDD	52	VDD	80	VDD	108	SCS[0]*
25	CAS[2]*	53	VSS	81	OE0*	109	VSS
26	CAS[3]*	54	A[16]	82	SWE0*	110	PIO0[0]
27	TOUT[0]	55	A[17]	83	SWE1*	111	PIO0[1]
28	TOUT[1]	56	A[18]	84	TSTO2	112	PIO0[2]

*Active-low signal

Table 1. Pin Assignment (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
113	PIO0[3]	137	VDD	161	D[10]	185	INT[7]
114	VDD	138	D[28]	162	D[9]	186	VSS
115	PIO0[4]	139	D[27]	163	D[8]	187	PCST[2]
116	PIO0[5]	140	D[26]	164	VSS	188	PCST[1]
117	PIO0[6]	141	D[25]	165	VDD	189	PCST[0]
118	PIO0[7]	142	VSS	166	D[7]	190	GDCLK
119	VSS	143	D[24]	167	D[6]	191	SDAO
120	TIMOUT2	144	D[23]	168	D[5]	192	DBGE*
121	TIMOUT1	145	D[22]	169	D[4]	193	SDI*
122	TIMIN2	146	D[21]	170	D[3]	194	DRESET*
123	TIMIN1	147	VDD	171	D[2]	195	TEST*
124	SCLK	148	VSS	172	VSS	196	RESET*
125	SIN1	149	D[20]	173	VDD	197	ACK*
126	SIN0	150	D[19]	174	D[1]	198	BUSERR*
127	SCNT1[1]	151	D[18]	175	D[0]	199	BSTART*
128	SCNT0[1]	152	D[17]	176	NMI*	200	VSS
129	VDD	153	D[16]	177	INT[0]	201	VDD
130	SOUT1	154	D[15]	178	INT[1]	202	SYSCLK
131	SOUT0	155	D[14]	179	INT[2]	203	PLLOFF*
132	SCNT1[0]	156	VDD	180	VDD	204	CLKEN
133	SCNT0[0]	157	VSS	181	INT[3]	205	VDDP
134	D[31]	158	D[13]	182	INT[4]	206	VSSP
135	D[30]	159	D[12]	183	INT[5]	207	VSS
136	D[29]	160	D[11]	184	INT[6]	208	XOUT

*Active-low signal

TMPR3904F 32-bit MIPS RISC Microprocessor

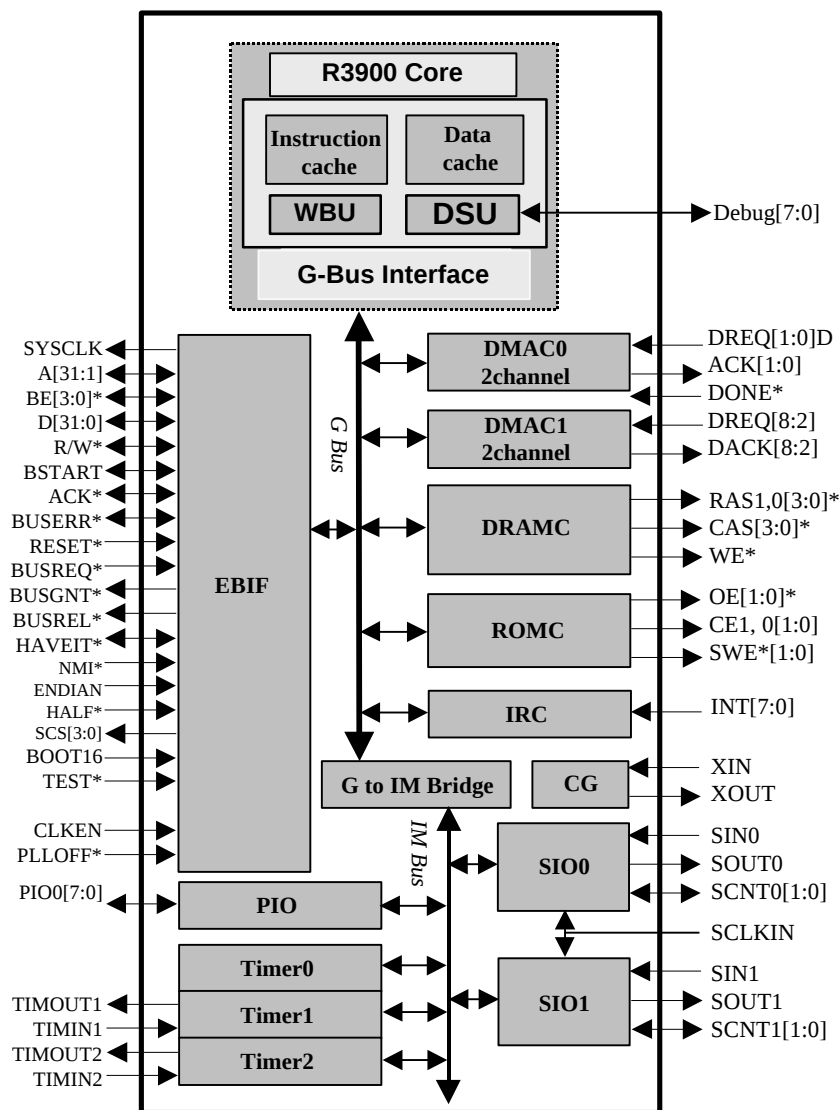


Figure 2. TMPR3904F Internal Block Diagram

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