features

- Regulated 3.3-V Output Voltage With up to 100-mA Output Current From a 1.8-V to 3.6-V Input Voltage
- Less Than 5-mV$_{(PP)}$ Output Voltage Ripple Achieved With Push-Pull Topology
- Integrated Low-Battery and Power-Good Detector
- Switching Frequency Can Be Synchronized to External Clock Signal
- Extends Battery Usage With up to 90% Efficiency and 35-μA Quiescent Supply Current
- Reliable System Shutdown Because Output Capacitor Is Discharged When Device Is Disabled
- Easy-To-Design, Low-Cost, Low-EMI Power Supply Since No Inductors Are Used
- 0.05-μA Shutdown Current, Battery Is Isolated From Load in Shutdown Mode
- Compact Converter Solution in UltraSmall 10-pin MSOP With Only Four External Capacitors Required
- Evaluation Module Available (TPS60200EVM-145)

applications

- Replaces DC/DC Converters With Inductors in Battery Powered Applications Like:
  - Two Battery Cells to 3.3-V Conversion
  - MP3 Portable Audio Players
  - Battery-Powered Microprocessor Systems
  - Backup-Battery Boost Converters
  - PDA's, Organizers, and Cordless Phones
  - Handheld Instrumentation
  - Glucose Meters and Other Medical Instruments

description

The TPS6020x step-up, regulated charge pumps generate a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage. The devices are typically powered by two Alkaline, NiCd or NiMH battery cells and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA for the TPS60200 and TPS60201 and 50 mA for the TPS60202 and TPS60203, all from a 2-V input. Only four external capacitors are needed to build a complete low-ripple dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output.

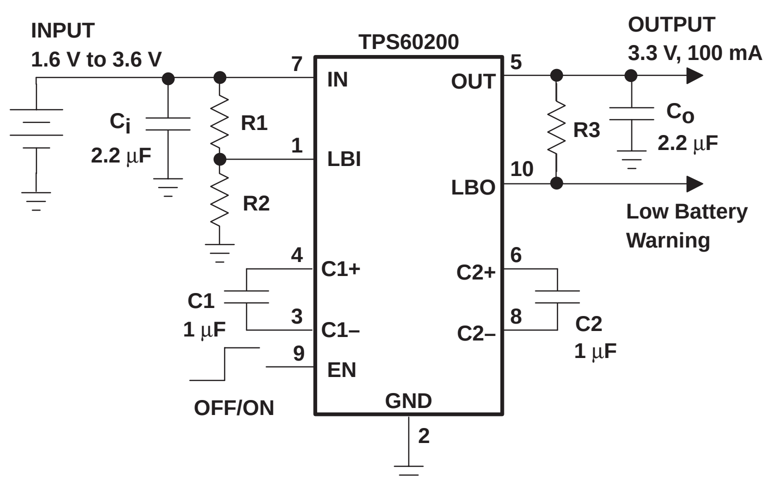
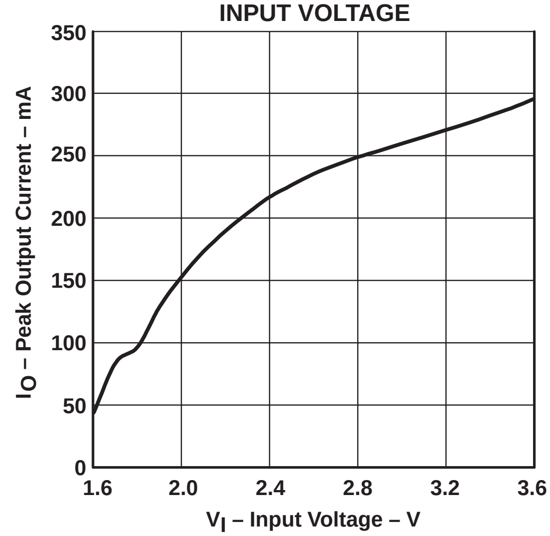


Figure 1. Typical Application Circuit With Low-Battery Warning

TPS60200
PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

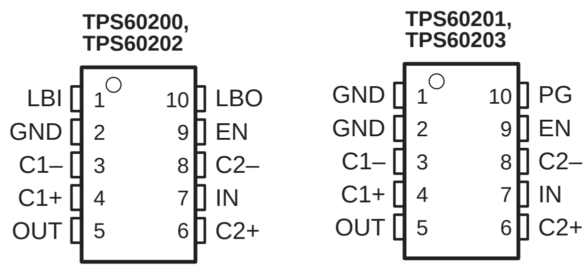
description (continued)

The devices operate in the newly developed LinSkip mode. In this operating mode, the device switches seamlessly from the power saving pulse-skip mode at light loads to the low-noise constant-frequency, linear-regulation mode once the output current exceeds the LinSkip threshold of about 7 mA. Even in pulse-skip mode the output ripple is maintained at a very low level because the output resistance of the charge pump is still regulated.

Three operating modes can be programmed using the EN pin. EN = low disables the device, shuts down all internal circuits and disconnects the output from the input. EN = high enables the device and programs it to run from the internal oscillator. The devices operate synchronized to an external clock signal if EN is clocked; thus switching harmonics can be controlled and minimized. The devices include a low-battery detector that issues a warning if the battery voltage drops below a user-defined threshold voltage or a power-good detector that goes active when the output voltage reaches about 90% of its nominal value.

Device options with either a low-battery or power good detector are available. This dc/dc converter requires no inductors therefore EMI of the system is reduced to a minimum. It is available in the small 10-pin MSOP package (DGS).

DGS PACKAGES



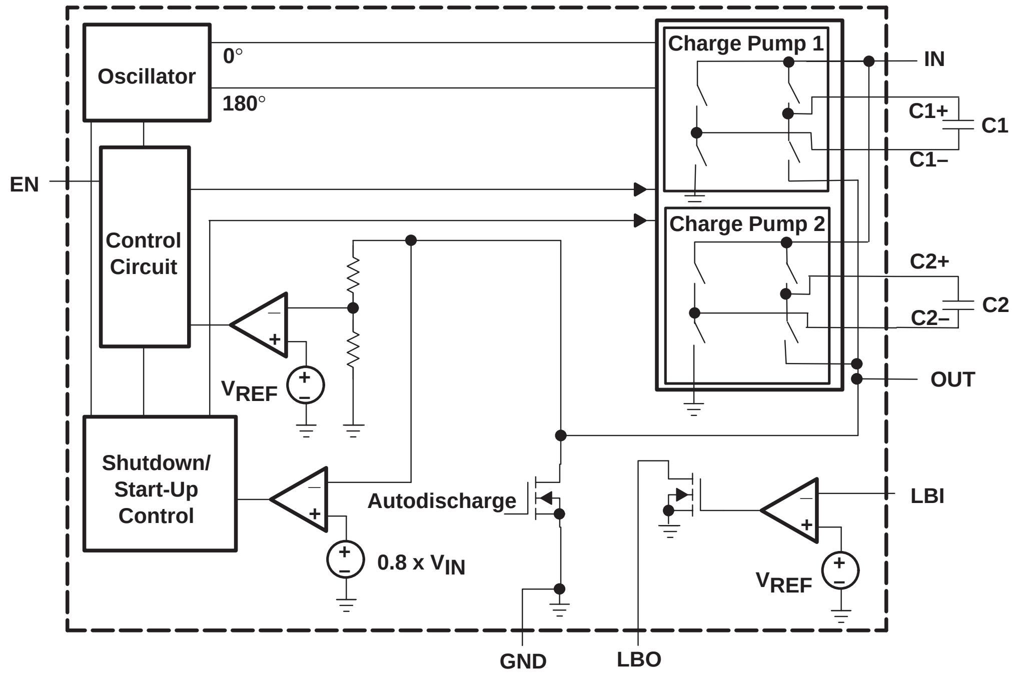
AVAILABLE OPTIONS

T_A	PART NUMBER†	MARKING DGS PACKAGE	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE (V)	DEVICE FEATURES
–40°C to 85°C	TPS60200DGS	AEX	100	3.3	Low-battery detector
	TPS60201DGS	AEY	100	3.3	Power-good detector
	TPS60202DGS	AEZ	50	3.3	Low-battery detector
	TPS60203DGS	AFA	50	3.3	Power-good detector

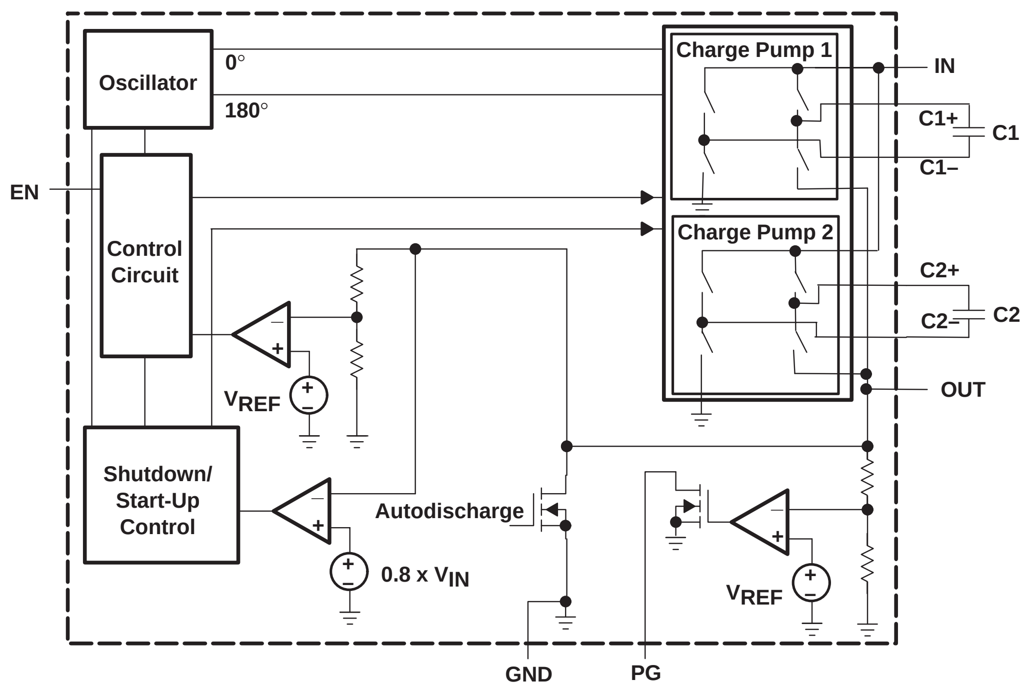
† The DGS package is available taped and reeled. Add R suffix to device type (e.g. TPS60200DGSR) to order quantities of 3000 devices per reel.

functional block diagrams

TPS60200 and TPS60202 with low-battery detector



TPS60201 and TPS60203 with power-good detector



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	4		Positive terminal of the flying capacitor C1
C1–	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2–	8		Negative terminal of the flying capacitor C2
EN	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. – EN = Low disables the device. Output and input are isolated in the shutdown mode and the output capacitor is automatically discharged. – EN = High lets the device run from the internal oscillator. – If an external clock signal is applied to the EN pin, the device is in Sync–Mode and runs synchronized at the frequency of the external clock signal.
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_O.
LBI/GND	1	I	Low-battery detector input for TPS60200 and TPS60202. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the devices TPS60201 and TPS60203, this pin has to be connected to ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for TPS60200 and TPS60202. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for TPS60201 and TPS60203. As soon as the voltage on OUT reaches about 90% of it is nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_O.

detailed description

operating principle

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V $\pm$ 4%. Designed specifically for space critical battery powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown/start-up circuit, a control circuit, and an auto-discharge transistor (see functional block diagrams).

push-pull operating mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, i.e. they operate with a 180°C phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

detailed description (continued)

constant-frequency mode

When the output current is higher then the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the $r_{DS(ON)}$ of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

pulse-skip mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

start up, shutdown, and auto-discharge

During start-up, i.e. when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage V_O reaches $0.8 \times V_I$. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33-Ω or 66-Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 µA. The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the products shelf life.

Additionally, the output capacitor will automatically be discharged after EN is taken low. This ensures that the system, when switched off, is in a stable and reliable condition since the supply voltage is removed from the supply pins.

synchronization to an external clock signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 µs.

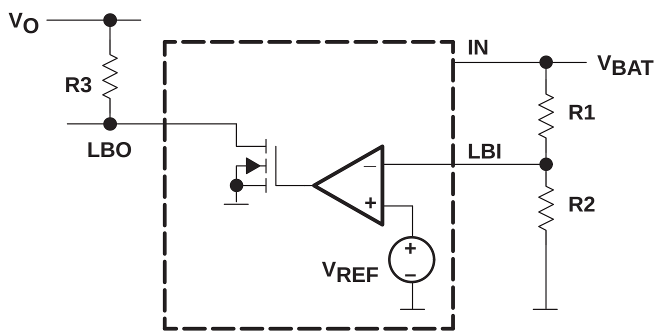
When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

detailed description (continued)

low-battery detector (TPS60200 and TPS60202)

The low-battery comparator trips at 1.18 V ±4% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.



$$V_{(TRIP)} = 1.18\ V \left(1 + \frac{R1}{R2}\right)$$

Figure 2. Programming of the Low-Battery Comparator Trip Voltage

A 100 nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V_{LBI} = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\ M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

detailed description (continued)

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

$V_{(IN)}$/V	R1/kΩ	R2/kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$/V
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

power-good detector (TPS60201 and TPS60203)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range: IN, OUT, EN, LBI, LBO, PG to GND . . . . –0.3 V to 3.6 V
C1+, C2+ to GND . . . . –0.3 V to (V_O + 0.3 V)
C1–, C2– to GND . . . . –0.3 V to (V_I + 0.3 V)
Continuous total power dissipation . . . . See dissipation rating table
Continuous output current TPS60200, TPS60201 . . . . 150 mA
Continuous output current TPS60202, TPS60203 . . . . 75 mA
Storage temperature range, T_{stg} . . . . –55°C to 150°C
Maximum junction temperature, T_J . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE 1 FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	424 mW	3.4 mW/°C	187 mW	136 mW

The thermal resistance junction to ambient of the DGS package is R_{TH-JA} = 294°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	1.6		3.6	V
Input capacitor, C_i		2.2		µF
Flying capacitors, C1, C2		1		µF
Output capacitor, C_O		2.2		µF
Operating junction temperature, T_J	–40		125	°C

electrical characteristics at C_i = 2.2 μF, C1 = C2 = 1 μF, C_O = 2.2 μF, T_A = –40°C to 85°C, V_I = 2.4 V, EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	TPS60200 and TPS60201, V_I = 2 V	100			mA
		TPS60202 and TPS60203, V_I = 2 V	50			mA
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17		3.43	V
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	V
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	V
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	μA
$I_{(SD)}$	Shutdown supply current	EN = 0 V		0.05	1	μA
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	kHz
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	EN input high voltage	V_I = 1.6 V to 3.6 V	0.7 × V_I			V
$I_{lkg(EN)}$	EN input leakage current	EN = 0 V or V_I		0.01	0.1	μA
	Output capacitor auto discharge time	EN is set from V_I to GND, Time until V_O < 0.5V		0.6		ms
	Output resistance in shutdown	EN = 0V		70		Ω
	LinSkip threshold	V_I = 2.2V		7		mA
	Output load regulation	10 mA < I_O < $I_{O(MAX)}$; T_A = 25°C		0.01		%/mA
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 x $I_{O(MAX)}$, T_A = 25°C		0.6		%/V
$I_{(SC)}$	Short circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

electrical characteristics for low-battery comparator of devices TPS60200 and TPS60202 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6V to 2.2V, T_c = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		2	50	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	μA

NOTE: During start-up of the converter the LBO output signal is invalid for the first 500 μs.

electrical characteristics for power-good comparator of devices TPS60201 and TPS60203 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_c = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_c = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage Low	V_O = 0V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	μA

NOTE: During start-up of the converter the PG output signal is invalid for the first 500 μs.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60200 and TPS60202)	3, 4
		vs Input voltage	5
I_Q	Quiescent supply current	vs Input voltage	6
V_O	Output voltage	vs Output current (TPS60200 and TPS60202)	7, 8
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V_O	Output voltage ripple	vs Time	11, 12, 13
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	Load transient response		15
	Line transient response		16
I_O	Peak output current	vs Input voltage (TPS60200)	17

NOTE: All typical characteristics were measured using the typical application circuit of Figure 18 (unless otherwise noted).

TPS60200
EFFICIENCY
vs
OUTPUT CURRENT

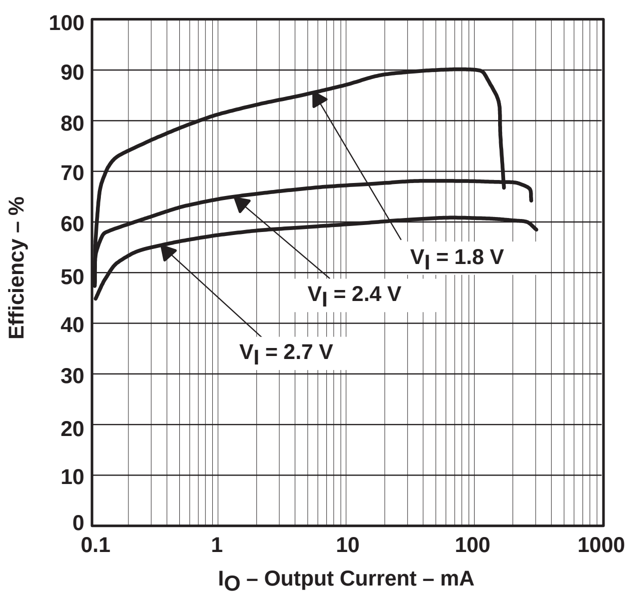


Figure 3

TPS60202
EFFICIENCY
vs
OUTPUT CURRENT

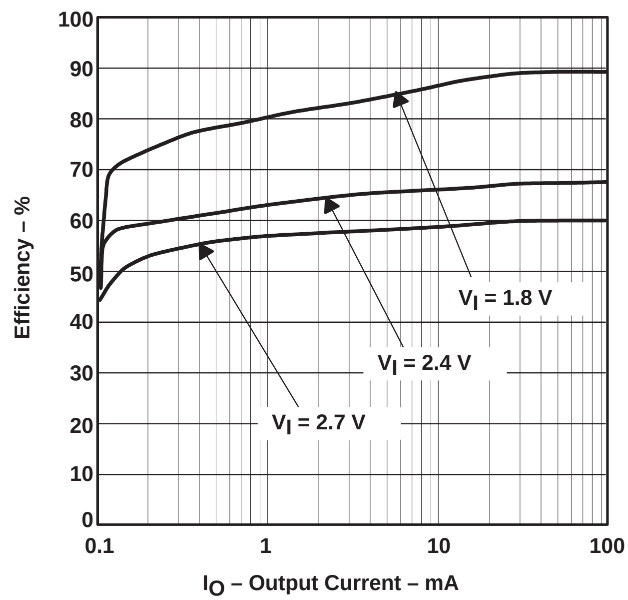


Figure 4

TYPICAL CHARACTERISTICS

TPS60200
EFFICIENCY vs INPUT VOLTAGE

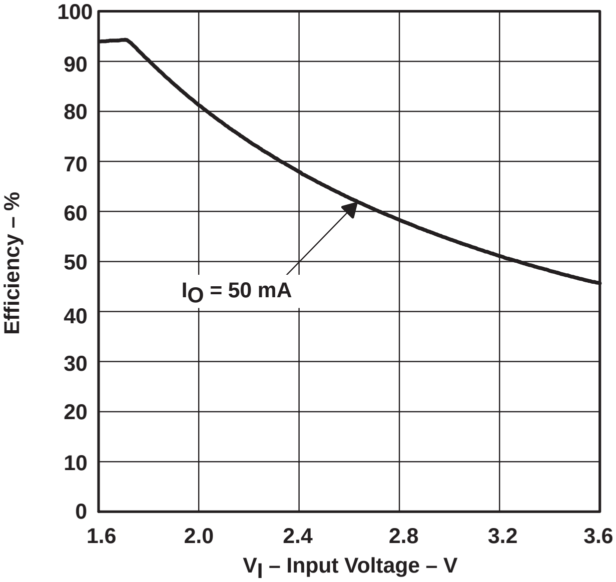


Figure 5

QUIESCENT SUPPLY CURRENT vs INPUT VOLTAGE

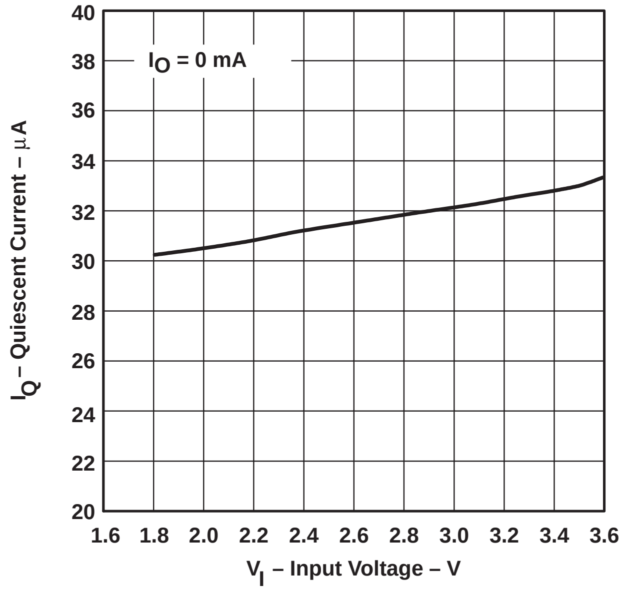


Figure 6

TPS60200
OUTPUT VOLTAGE vs OUTPUT CURRENT

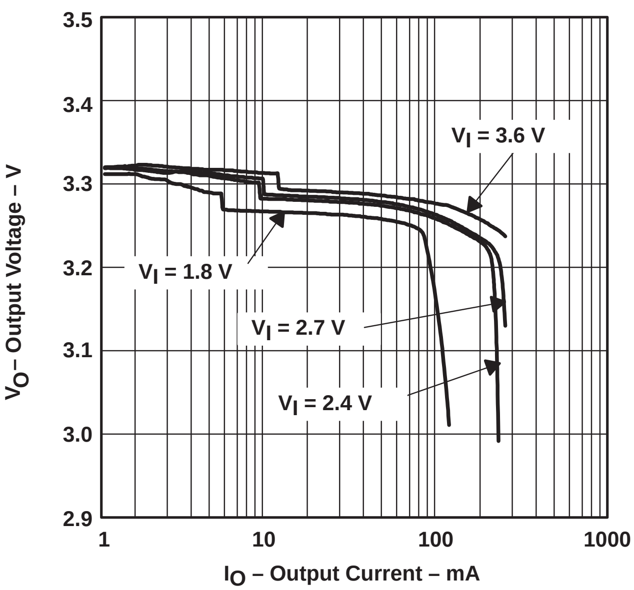


Figure 7

TPS60202
OUTPUT VOLTAGE vs OUTPUT CURRENT

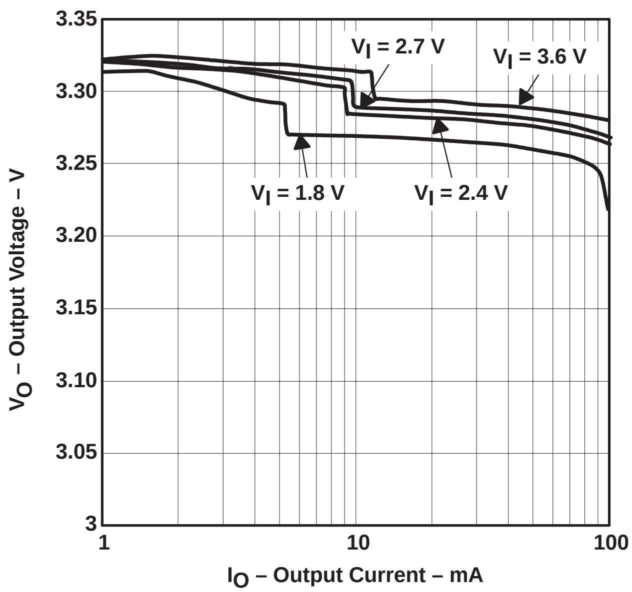


Figure 8

TYPICAL CHARACTERISTICS

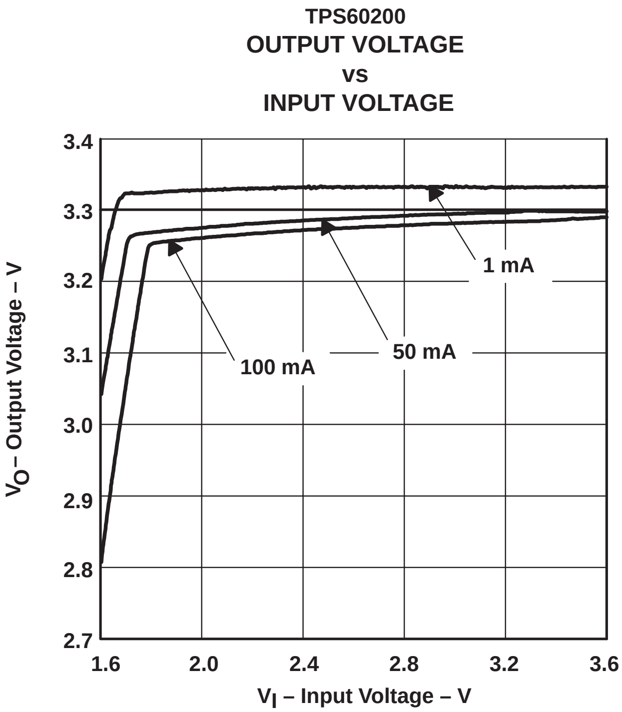


Figure 9

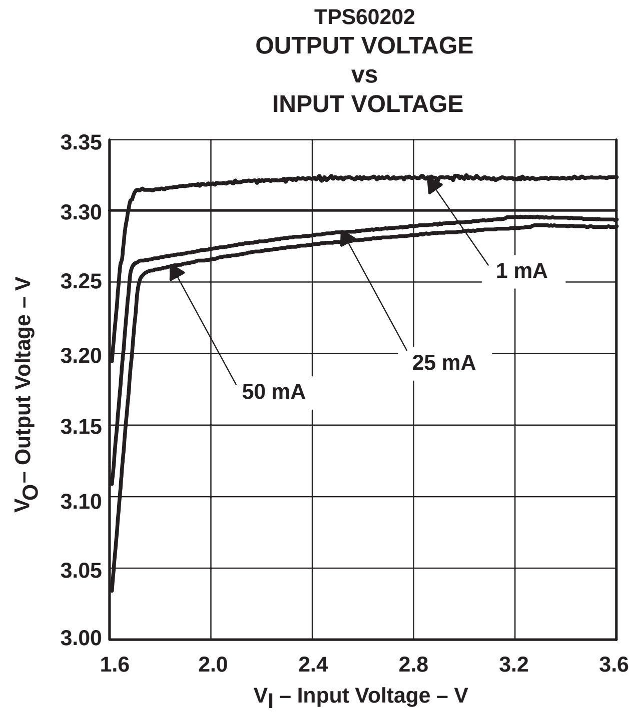


Figure 10

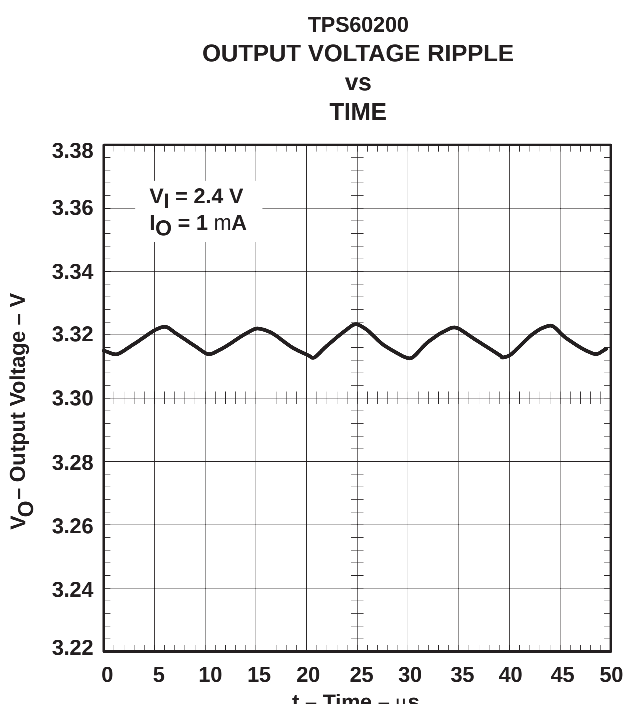


Figure 11

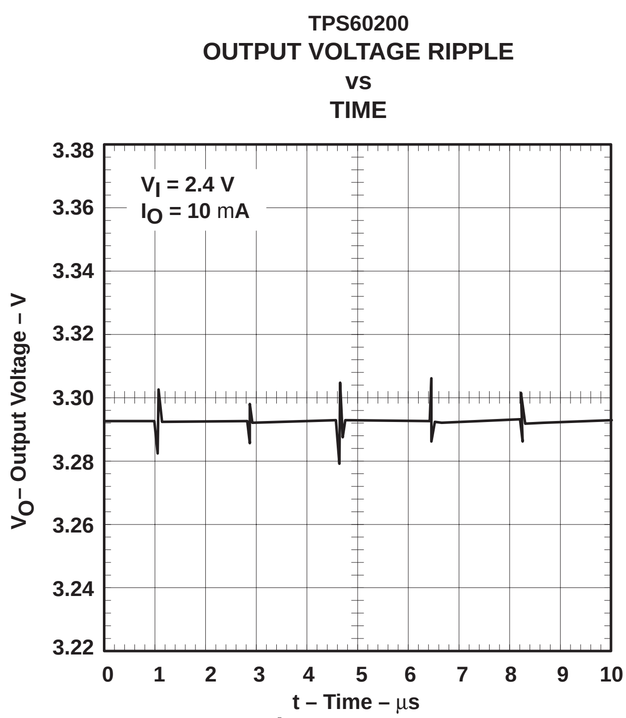


Figure 12

TYPICAL CHARACTERISTICS

TPS60200
OUTPUT VOLTAGE RIPPLE
vs
TIME

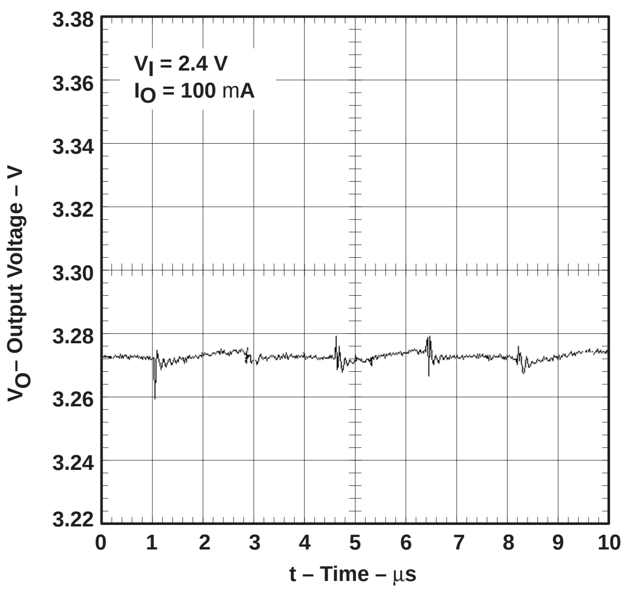


Figure 13

START-UP TIMING

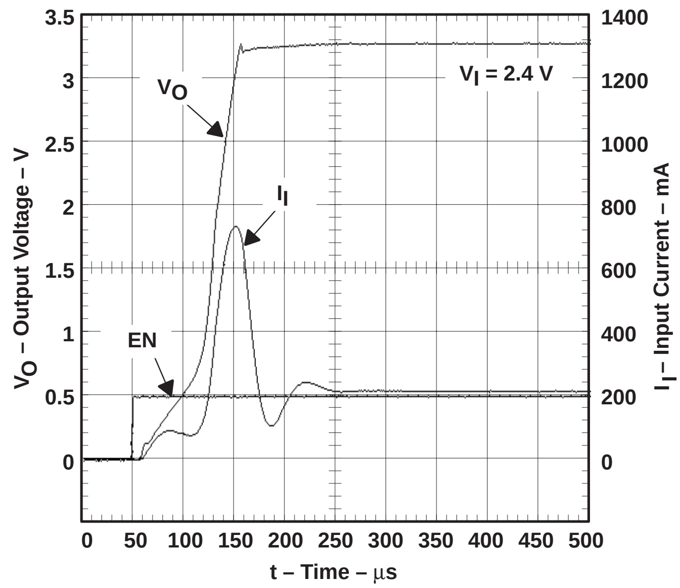


Figure 14

TPS60200
LOAD TRANSIENT RESPONSE

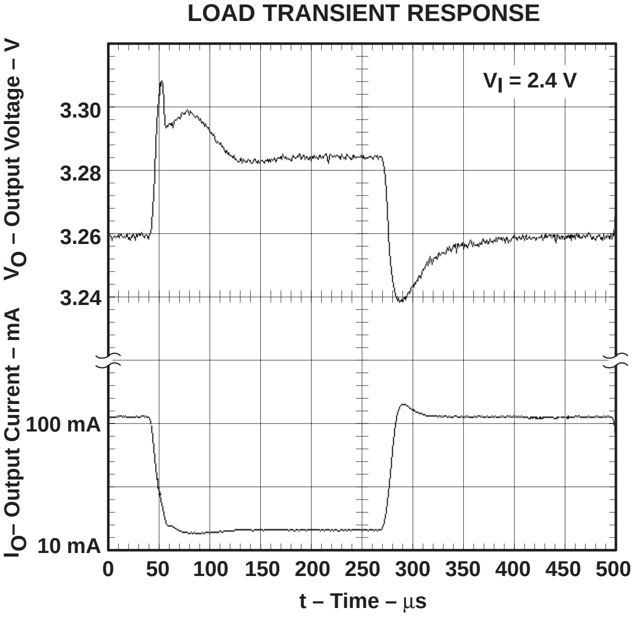


Figure 15

TPS60200
LINE TRANSIENT RESPONSE

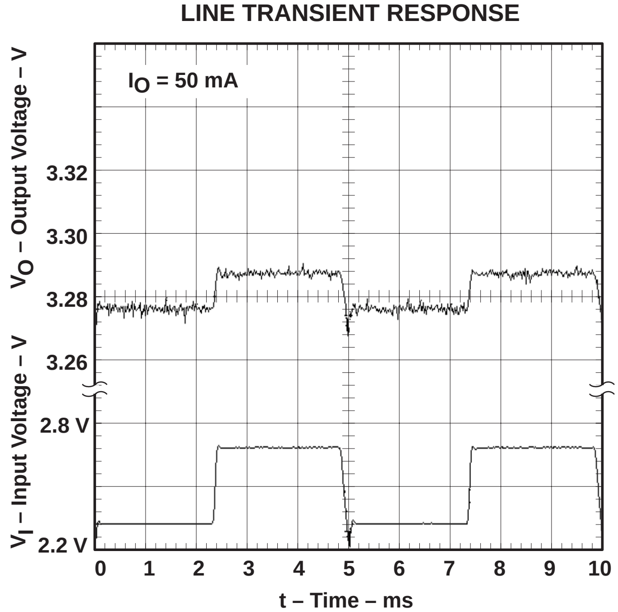


Figure 16

TYPICAL CHARACTERISTICS

**TPS60200
PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE**

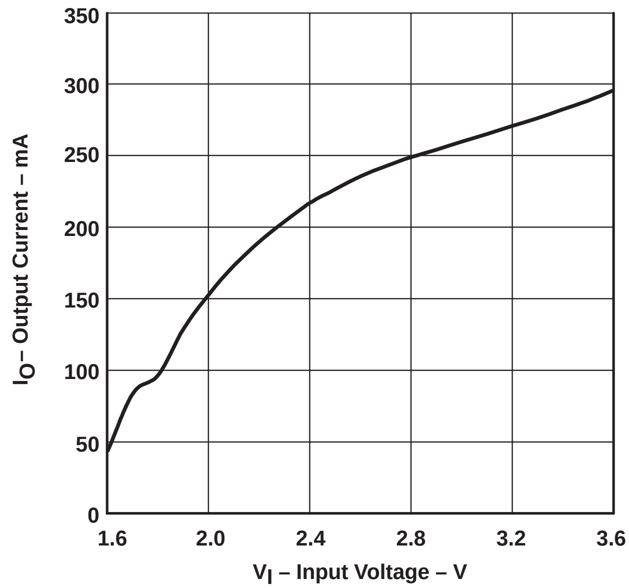


Figure 17

APPLICATION INFORMATION

capacitor selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (<0.1 Ω) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest, a 1-μF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. C_i is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (C_O) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 μF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 2 lists recommended capacitor values.

APPLICATION INFORMATION

Table 2. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L (mA)	FLYING CAPACITORS, C1/C2 (µF)	INPUT CAPACITOR, C_i (µF)	OUTPUT CAPACITOR, C_O (µF)	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$ (mV)	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ (mV)
0–100	1	2.2	2.2	3	20
0–100	1	4.7	4.7	3	10
0–100	1	2.2	10	3	7
0–100	2.2	4.7	4.7	3	10
0–50	0.47	2.2	2.2	3	20
0–25	0.22	2.2	2.2	5	15
0–10	0.1	2.2	2.2	5	15

Table 3. Recommended Capacitor Types

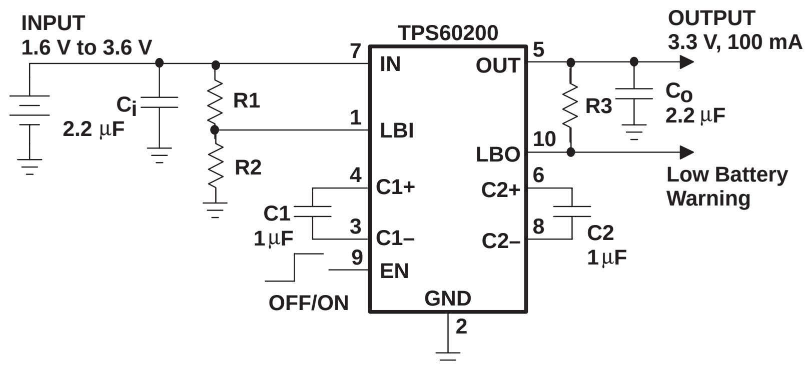
MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
	EMK212BJ224MG	0805	0.22 µF	Ceramic
	EMK212BJ474MG	0805	0.47 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106ML	1206	10 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

APPLICATION INFORMATION

typical operating circuit TPS60200 and TPS60202



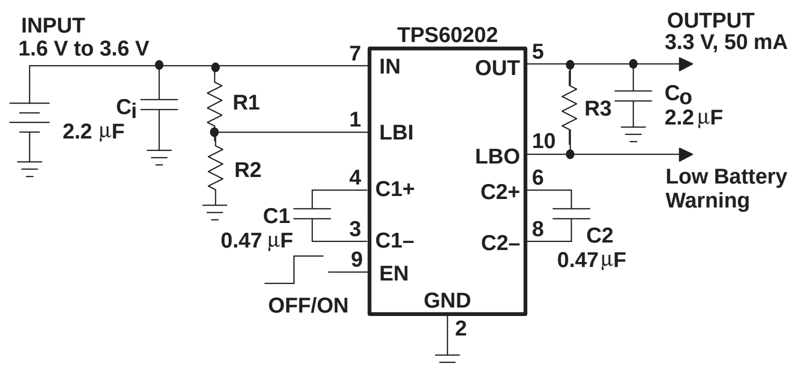
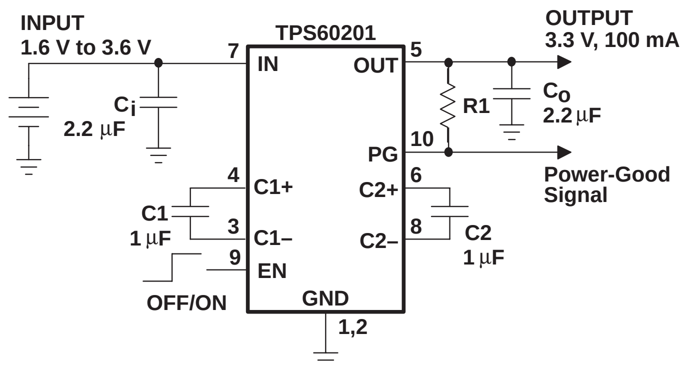


Figure 18. Typical Operating Circuit TPS60200 and TPS60202 With Low-Battery Detector

APPLICATION INFORMATION

typical operating circuit TPS60201 and TPS60203



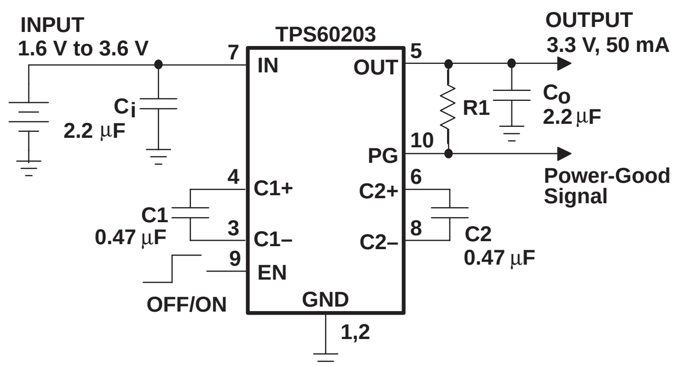


Figure 19. Typical Operating Circuit TPS60201 and TPS60203 With Power-Good Detector

power dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated by:

$$P_{(DISS)} = I_O \times \left(2 \times V_I - V_O\right) \qquad \text{for } I_{(Q)} << I_O \tag{5}$$

By observing equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\Theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125°C - 85°C}{390\ mW} = 102°C/W \tag{6}$$

APPLICATION INFORMATION

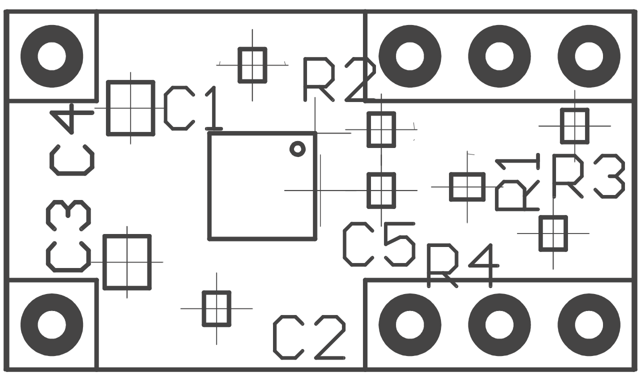
power dissipation (continued)

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\Theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However in a battery powered application, both V_I and T_A will typically be lower than the worst case ratings used in equation 6 , and power dissipation should not be a problem in most applications.

layout and board space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 20.

An evaluation module for the TPS60200 is available and can be ordered under product code TPS60200EVM–145. The EVM uses the layout shown in Figure 20. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket, therefore, the space needed for the IC, the external parts, and 8 pins is 17,9 mm x 10,2 mm = 182,6 mm^2.



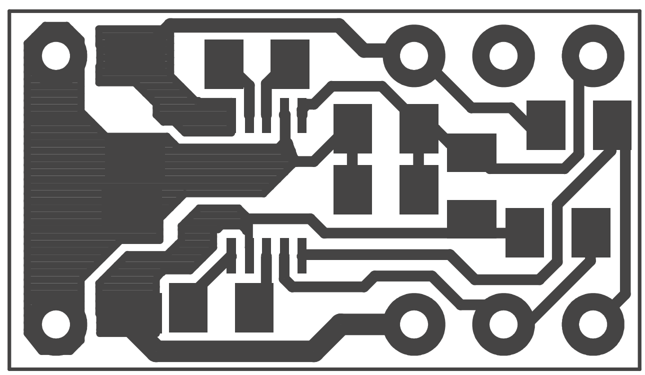


Figure 20. Recommended Component Placement and Board Layout

Table 5. Component Identification

IC1	TPS60200
C1, C2	Flying capacitors
C3	Input capacitors
C4	Output capacitors
C5	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

APPLICATION INFORMATION

device family products

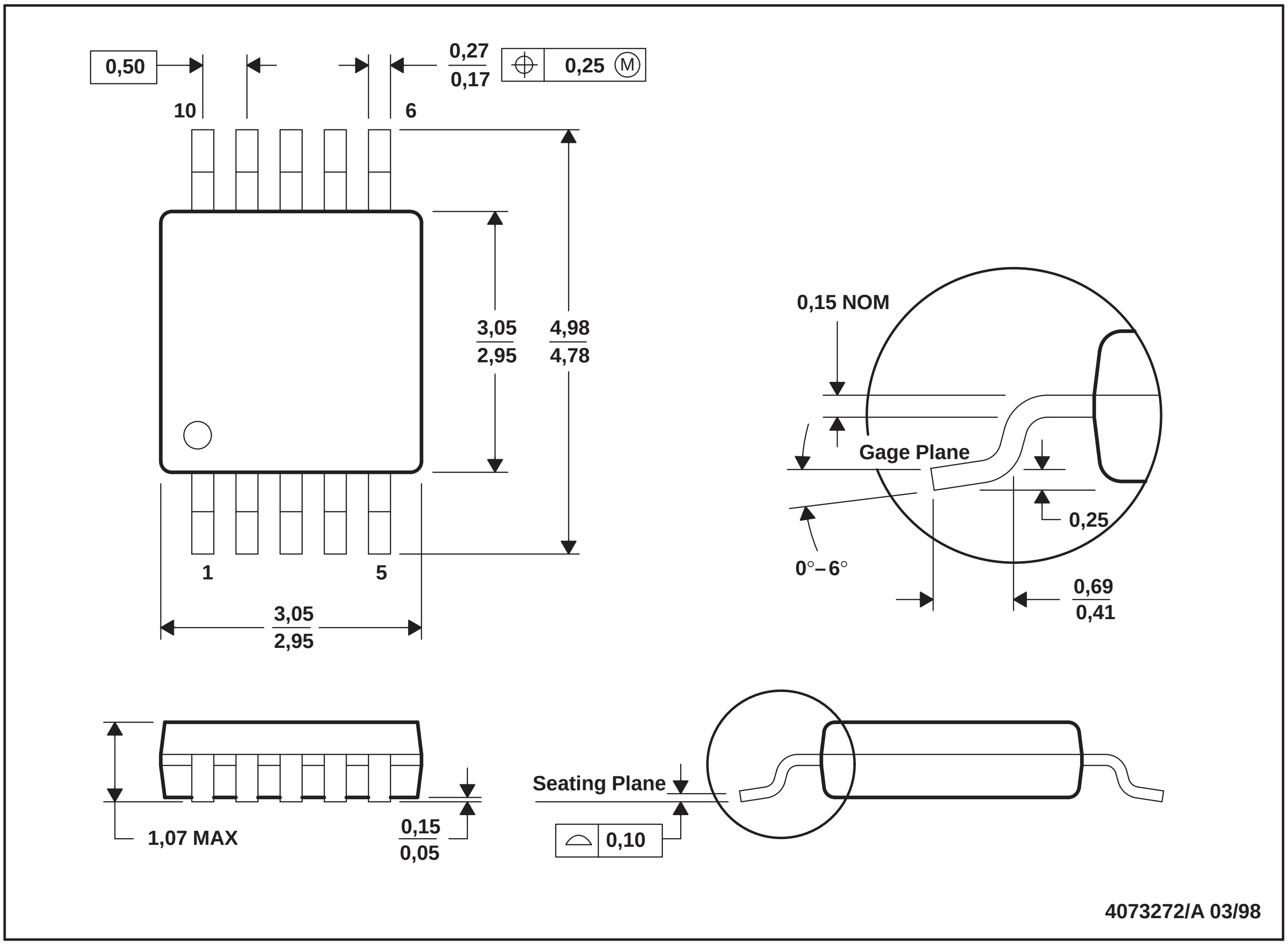
Other charge pump dc-dc converters in this family are:

Table 6. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5.0 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5.0 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with power-good comparator
TPS60132	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with power-good comparator

MECHANICAL DATA

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

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