Bluetooth Single-Chip Transceiver IC

Description

The T2901 is an RF-IC intended for Bluetooth applications in the 2.4 GHz to 2.5 GHz ISM band. The HP-VFQFP-N48 packaged IC is a complete transceiver including image rejection mixer, IF amplifier, FM demodulator, baseband filter, RSSI, TX preamplifier, power-ramping generator for power amplifiers, integrated synthesizer, fully integrated VCO, TX filter and modulation compensation circuit for advanced closed-loop modulation concept. No mechanical adjustment is necessary in production.

Features

- Supply–voltage range 3V to 4.6 V (unregulated)
- Auxiliary–voltage regulator on chip
- Low current consumption
- Few low cost external components
- No mechanical adjustment required
- Image rejection receiver
- Fully integrated GFSK–Modulator
- Unlimited multislot operation with advanced closed loop modulation
- TX ampl. (+3dBm in steps controllable output power)
- Integrated ramp–signal generator and power control for an additional +20 dBm SiGe power ampl. T7024
- Bluetooth compatible

Block Diagram

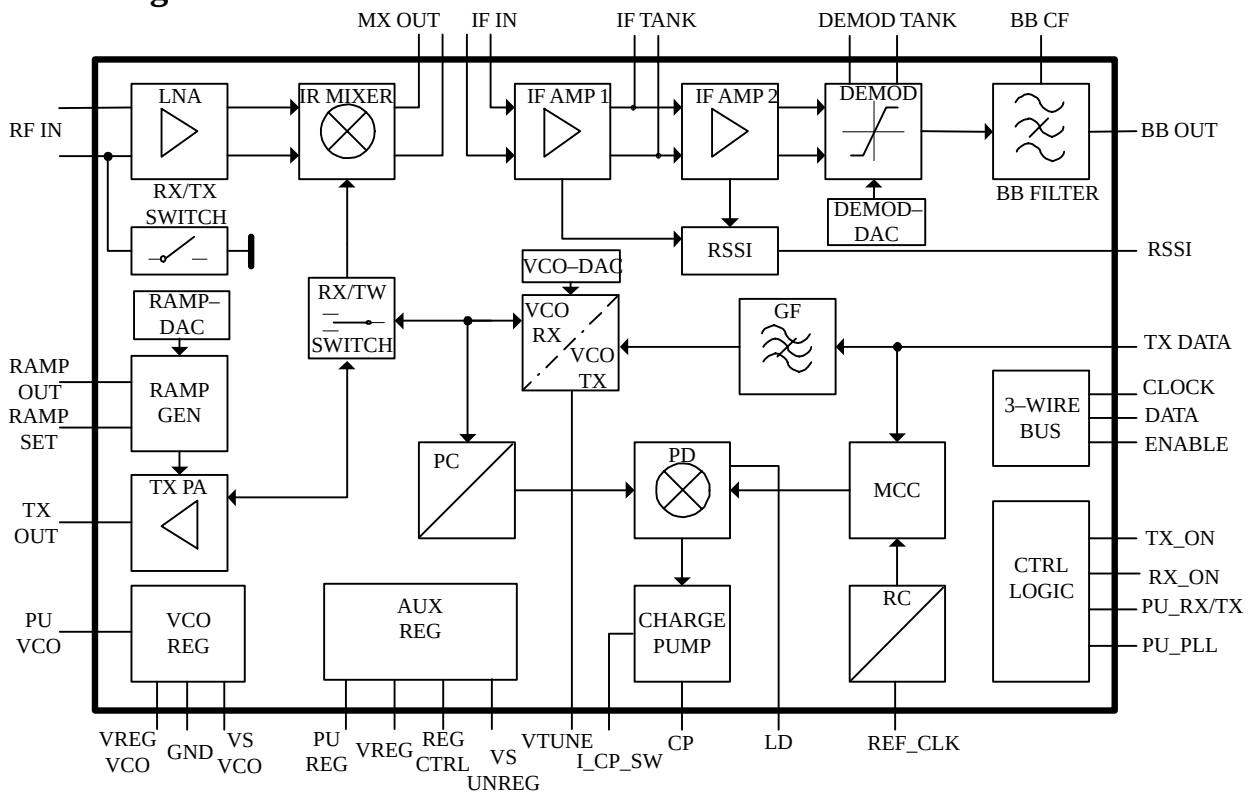


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T2901–PLT	HP-VFQFP-N48	Tray
T2901–PLQ	HP-VFQFP-N48	Taped and reeled

Functional Block Description

Name	Description
AUX REG	Auxiliary voltage regulator
BBF	Baseband filter
CP	Charge pump
DAC	D/A converter for demodulator tuning
GF	Gaussian filter for transmit data
IF AMP1	1st intermediate frequency amplifier
IF AMP2	2nd intermediate frequency amplifier
IR MIXER	Image rejection mixer
LNA	Low noise amplifier

Name	Description
MCC	Modulation-compensation circuit
PC	Programmable counter
PD	Phase detector
RAMP GEN	Ramp-signal generator
RC	Reference counter
RSSI	Received signal-strength indicator
TX PA	Transmit power amplifier
VCO	Voltage-controlled oscillator
VCO REG	Voltage regulator for VCO

Pinning

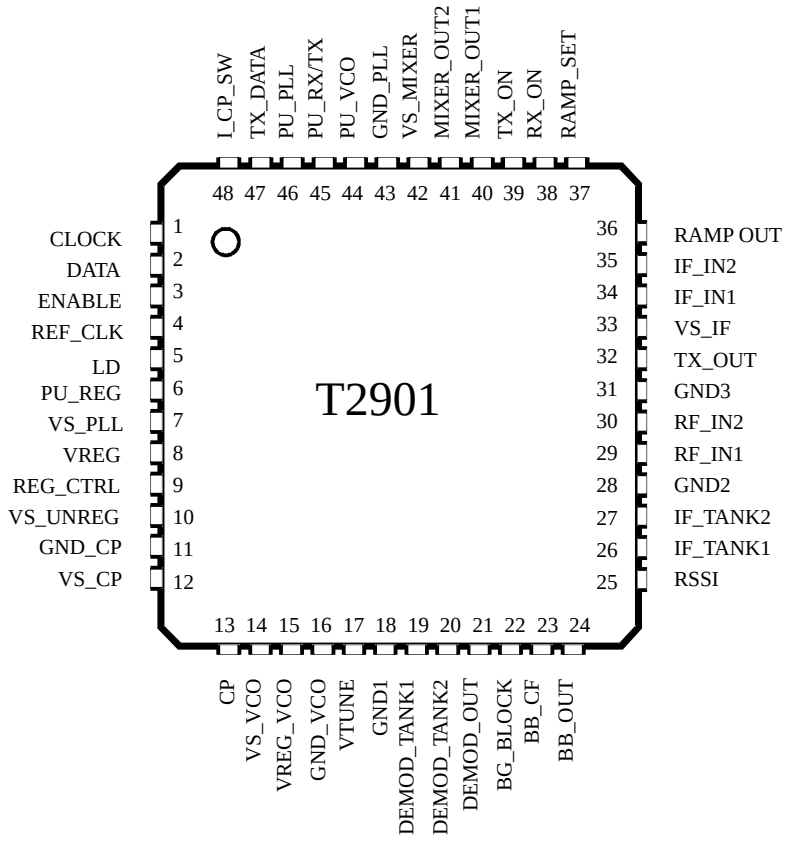
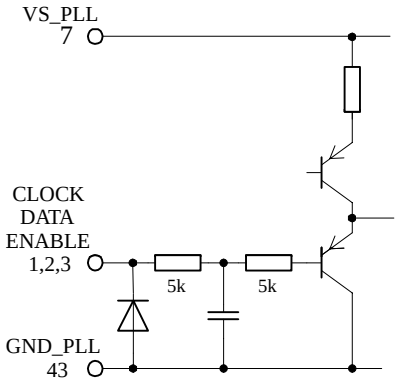
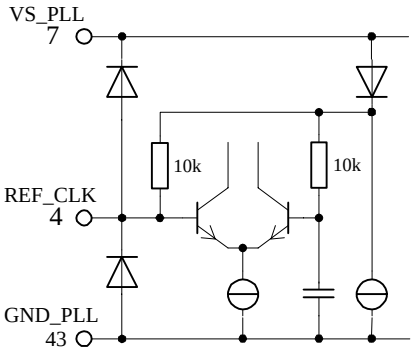
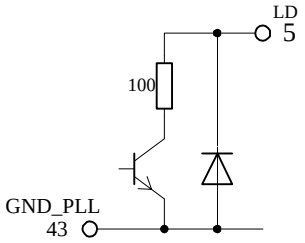
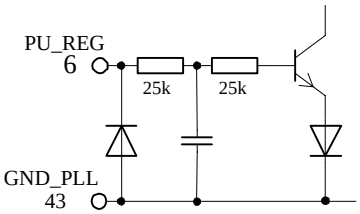
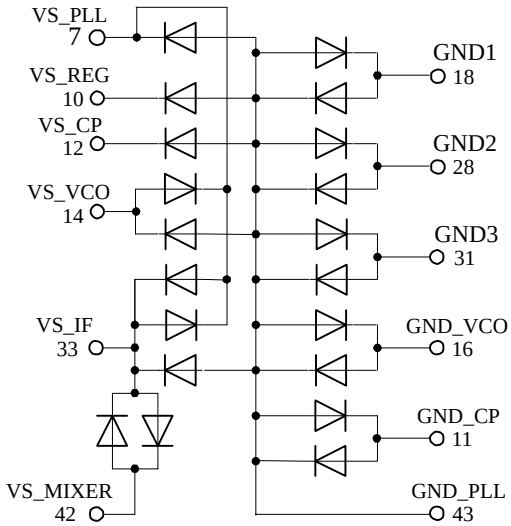
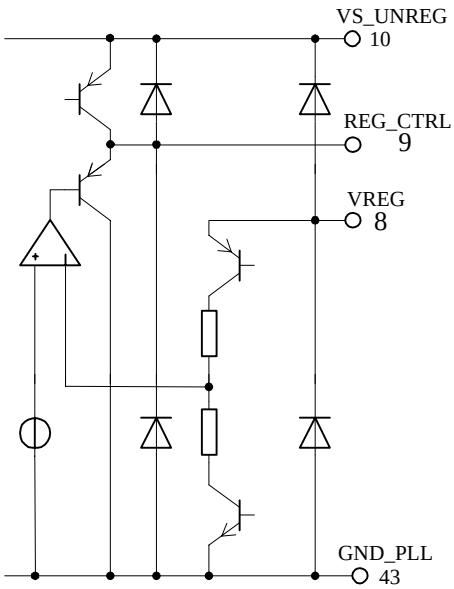
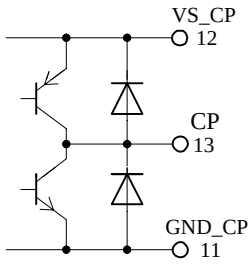


Figure 2. Pinning

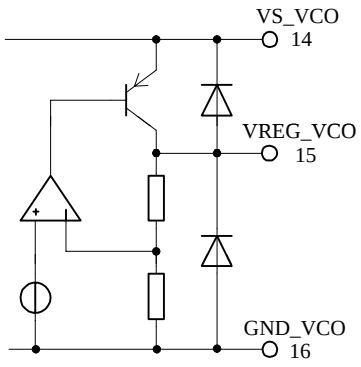
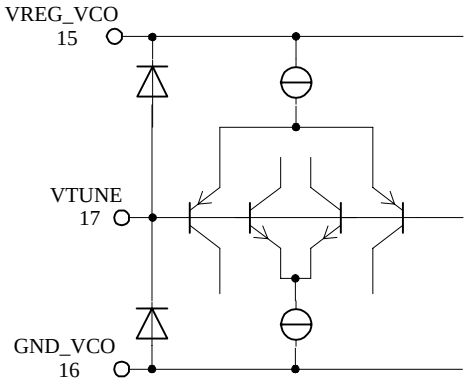
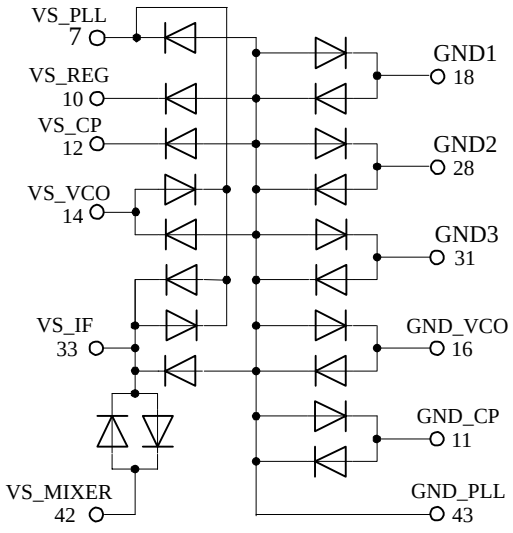
Pin Description

Pin	Symbol	Function	Configuration
1	CLOCK	3-wire-bus: Clock input	
2	DATA	3-wire-bus: Data input	
3	ENABLE	3-wire-bus: Enable input	
4	REF_CLK	Reference-frequency input	
5	LD	Lock-detect output	
6	PU_REG	Power-up input for aux. voltage regulator	

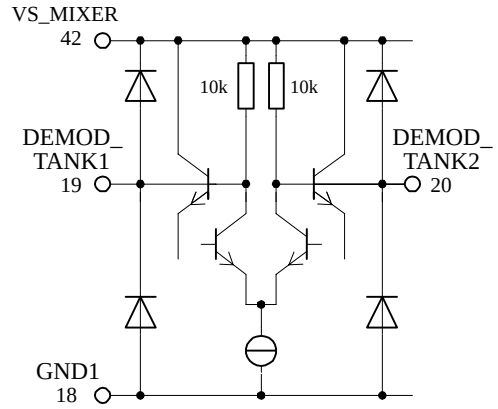
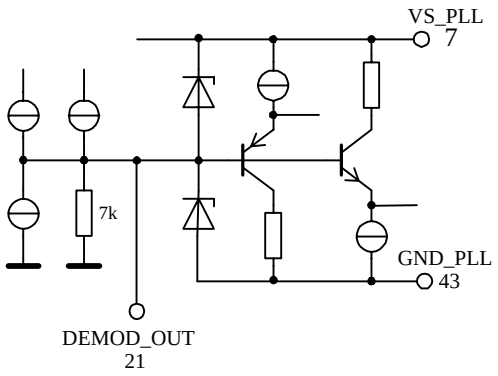
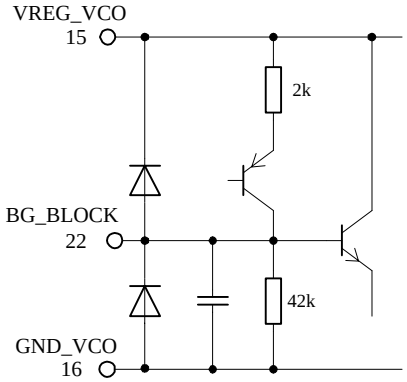
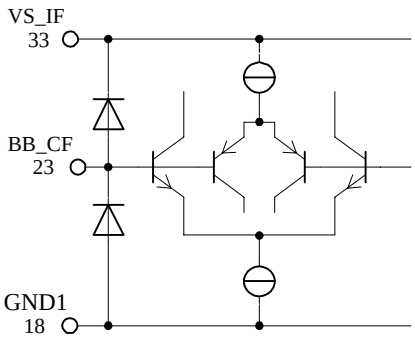
Pin Description (continued)

Pin	Symbol	Function	Configuration
7	VS_PLL	PLL supply voltage	
8	VREG	Aux. voltage-regulator output	
9	REG_CTRL	Aux. voltage-regulator control output	
10	VS_UNREG	Aux. voltage-regulator supply voltage	
11	GND_CP	Charge-pump ground	
12	VS_CP	Charge-pump supply voltage	
13	CP	Charge-pump output	

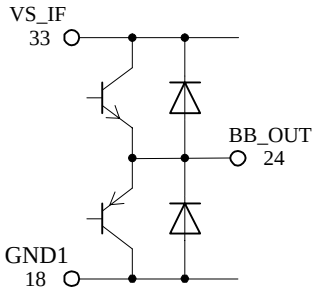
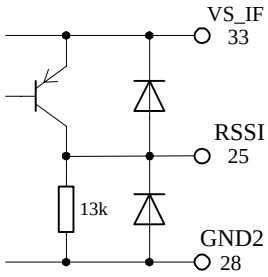
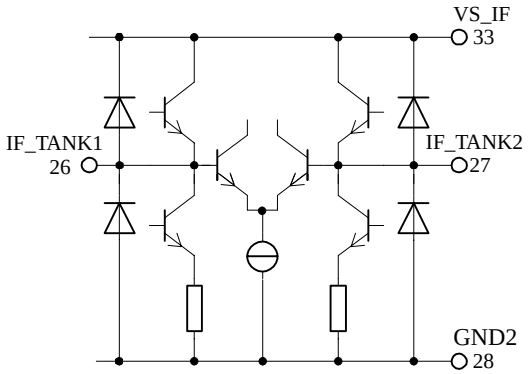
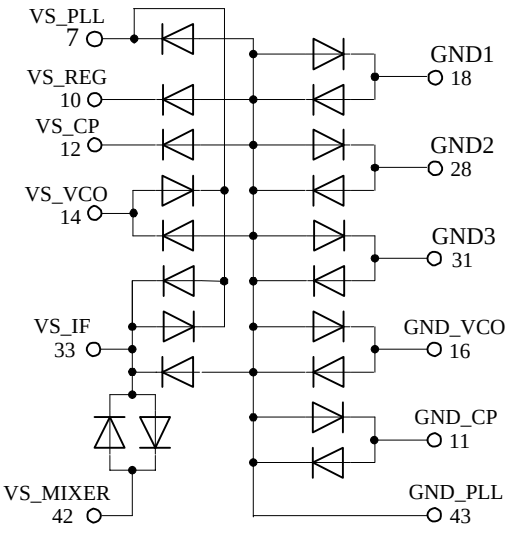
Pin Description (continued)

Pin	Symbol	Function	Configuration
14	VS_VCO	VCO voltage-regulator supply voltage	
15	VREG_VCO	VCO voltage-regulator control output	
16	GND_VCO	VCO ground	
17	VTUNE	VCO tuning voltage input	
18	GND1	Ground	

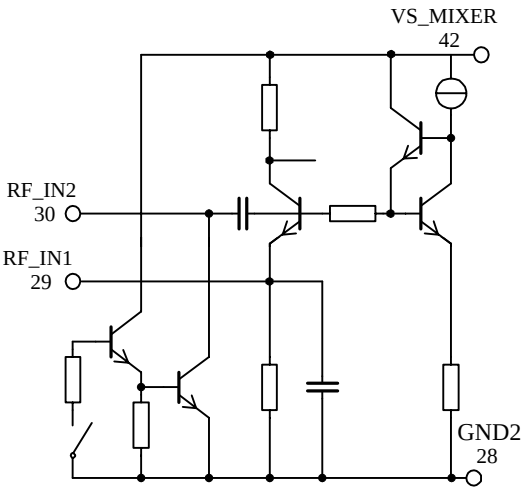
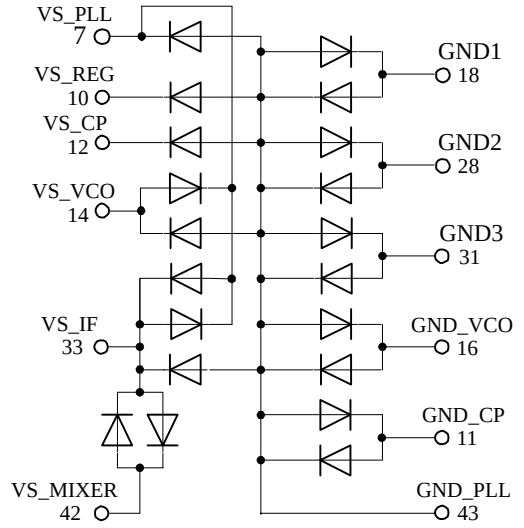
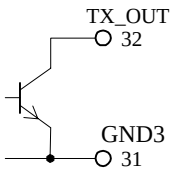
Pin Description (continued)

Pin	Symbol	Function	Configuration
19	DEMOD_TANK1	Demodulator tank circuit	
20	DEMOD_TANK2	Demodulator tank circuit	
21	DEMOD_OUT	Demodulator output	
22	BG_BLOCK	Decoupling PIN for VCO_REG	
23	BB_CF	Baseband filter corner-frequency control input	

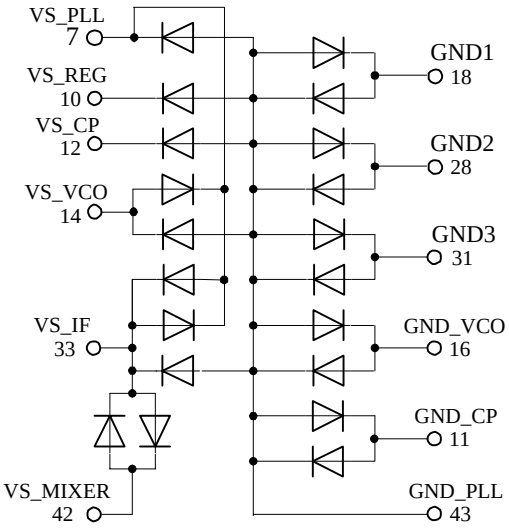
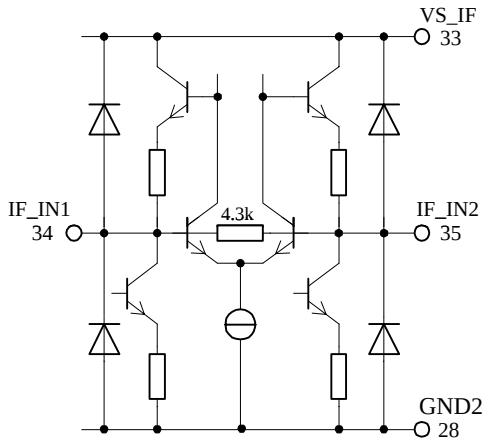
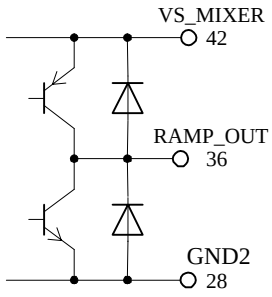
Pin Description (continued)

Pin	Symbol	Function	Configuration
24	BB_OUT	Baseband filter output	
25	RSSI	Received signal-strength indicator output	
26	IF_TANK1	IF tank circuit	
27	IF_TANK2	IF tank circuit	
28	GND2	Ground	

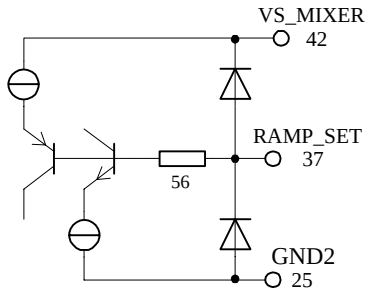
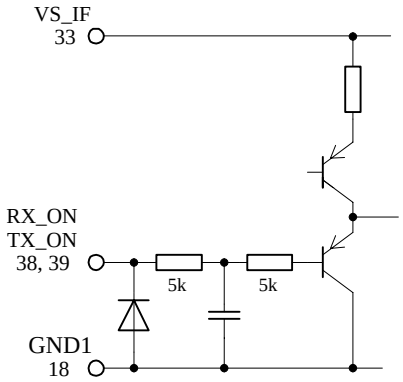
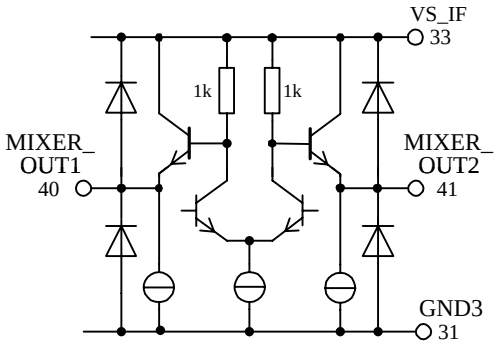
Pin Description (continued)

Pin	Symbol	Function	Configuration
29	RF_IN1	Decoupling pin for RF input	
30	RF_IN2	RF input of image reject mixer	
31	GND3	Ground	
32	TX_OUT	TX driver amplifier output for PA	

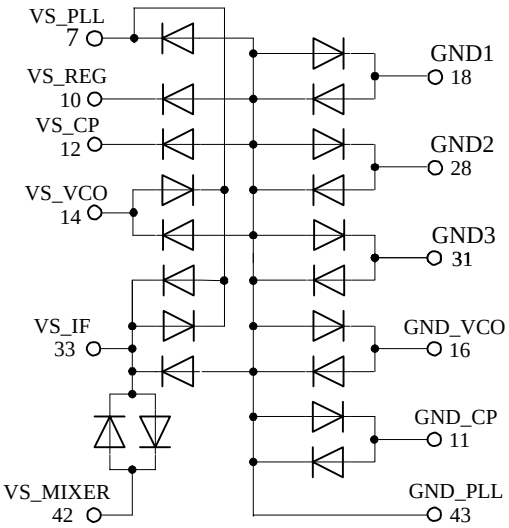
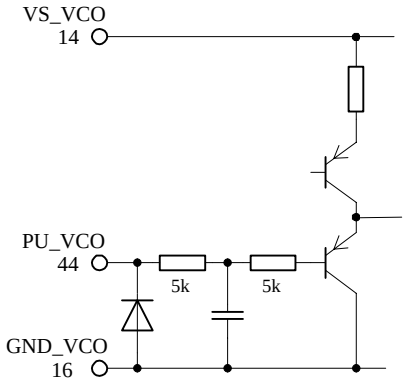
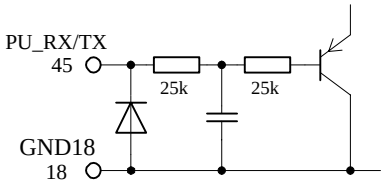
Pin Description (continued)

Pin	Symbol	Function	Configuration
33	VS_IF	IF amplifier supply voltage	
34	IF_IN1	IF input of IF amplifier	
35	IF_IN2	IF input of IF amplifier	
36	RAMP_OUT	Ramp-generator output for PA power ramping	

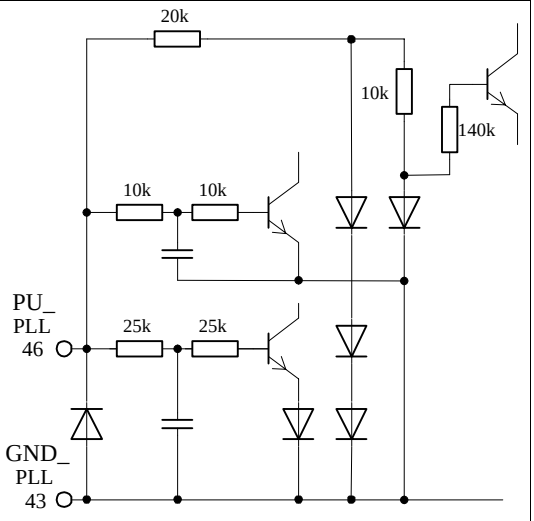
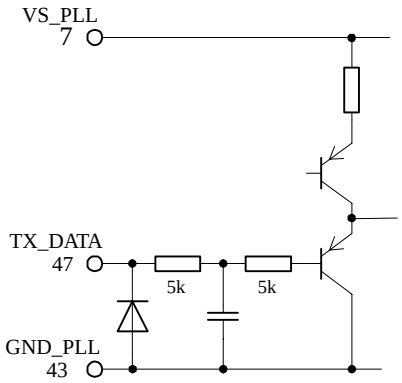
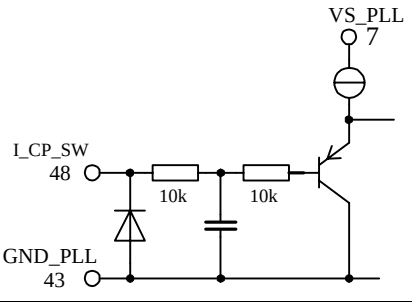
Pin Description (continued)

Pin	Symbol	Function	Configuration
37	RAMP_SET	Slew-rate setting of ramping signal	
38	RX_ON	RX control input	
39	TX_ON	TX control input	
40	MIXER_OUT1	Mixer output to SAW filter	
41	MIXER_OUT2	Mixer output to SAW filter	

Pin Description (continued)

Pin	Symbol	Function	Configuration
42	VS_MIXER	Mixer supply voltage	
43	GND_PLL	PLL ground	
44	PU_VCO	VCO power-up input	
45	PU_RX/TX	RX/TX power-up input	

Pin Description (continued)

Pin	Symbol	Function	Configuration
46	PU_PLL	PLL power-up input	
47	TX_DATA	TX data input of Gaussian filter and modulation-compensation circuit	
48	I_CP_SW	Charge-pump current switch	

Functional Description

Receiver

The RF signal at RF_IN is fed to an image rejection mixer IR_MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 111 MHz. The IF amplifiers IF_AMP1 and IF_AMP2 with an external IF_TANK and an integrated RSSI function feeds the signal to the demodulator DEMOD working at $f = f_{IF}/2$ (=55.5 MHz) and finally to an integrated baseband filter BB. For demodulator tuning in production an integrated 5-bit digital-to-analog (D/A) converter is provided to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian Filter GF and fed to the fully integrated VCO operating at twice the output frequency. After modulation the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX_DRIVER. This bus-controlled driver amplifier supplies typical +3 dBm output power at TX_OUT. A ramp-signal generator RAMP_GEN, provides a ramp signal at RAMP_OUT for the external power amplifier, is integrated. The slope of the ramp signal is controlled by a capacitor at the RAMP_SET pin.

Synthesizer

The IR_MIXER, the TX_DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). An 3-bit digital-to-analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD (f_{PD} = 1.0 MHz). Unlimited multislot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

An integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

PLL Principle

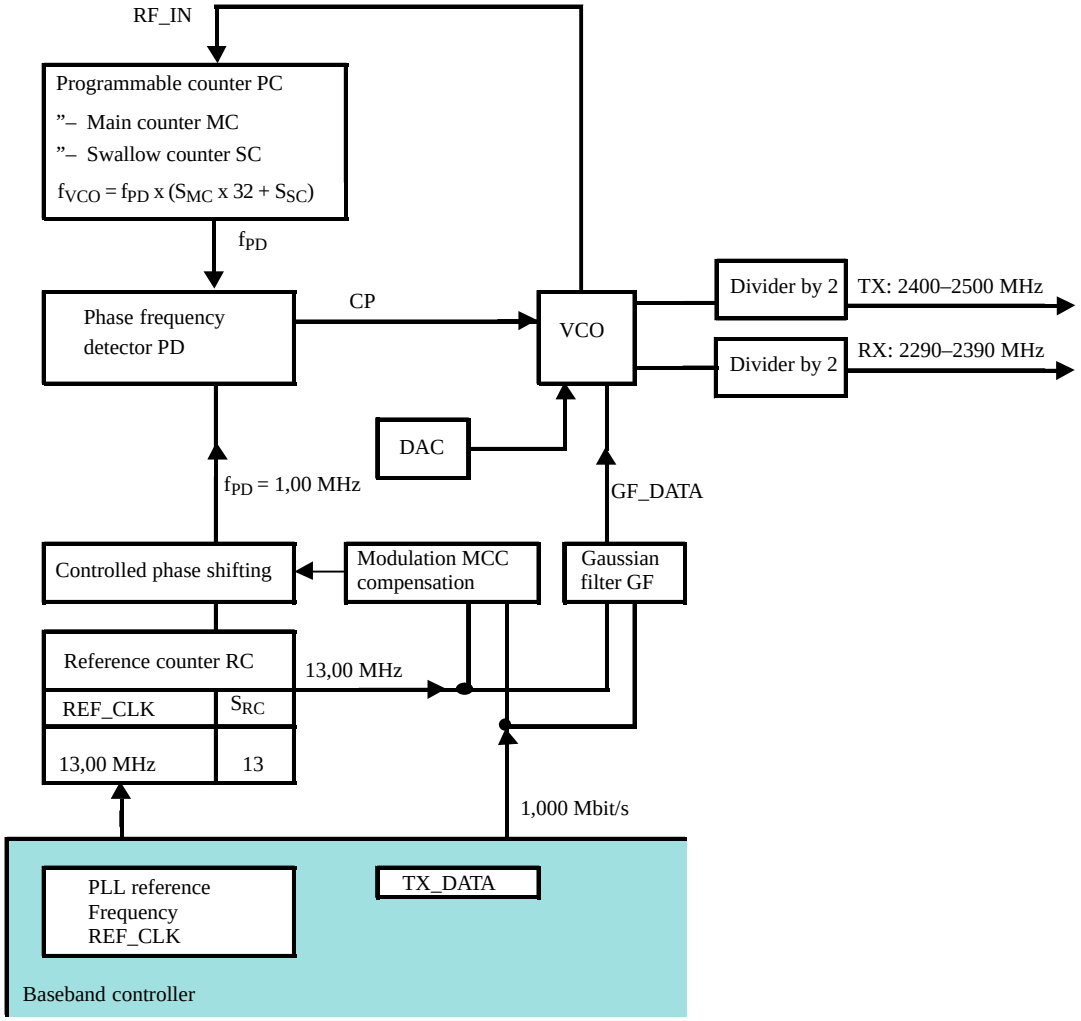


Figure 3. PLL principle

The following table shows the LO frequencies for RX and TX for the Bluetooth band.

Table 1 Table 1 LO frequencies

Mode	f_{if} /MHz	Channel	f_{ant}/MHz	f_{VCO}/MHz	S_{MC}	S_{SC}
TX		C0	2402	2402	75	2
		C1	2403	2403	75	3
		C2	2404	2404	75	4
		...	...	...	...	...
		C76	2478	2478	77	14
		C77	2479	2479	77	15
		C78	2480	2480	77	16
RX	111.00	C0	2402	2291	71	19
		C1	2403	2292	71	20
		C2	2404	2293	71	21
		...	...	...	...	...
		C76	2478	2367	73	31
		C77	2479	2368	74	0
		C78	2480	2369	74	1

Formula:

TX: $f_{ANT} = f_{VCO} = 1.00\ MHz \times (32 \times S_{MC} + S_{SC})$
RX: $f_{ANT} = f_{VCO} = 1.00\ MHz \times (32 \times S_{MC} + S_{SC}) + f_{IF}$

Table 2 Maximum programmable LO frequencies for RX and TX

	f_{IF} [MHz]	f_{RX} [MHz]	f_{TX} [MHz]	S_{MC}	S_{SC}
min	111.0	2159.0	2048.0	64	0
max	111.0	2670.0	2559.0	79	31

Control Signals

Table 3

Signal	Function
I_CP_SW	Switches the charge-pump current between two different states.
PU_REG	Activates AUX voltage regulator supplying the complete transceiver.
PU_VCO	Activates VCO voltage regulator which supplies only the VCO.
PU_RX/TX	Activates RX/TX switch.
PU_PLL	Activates PLL circuits: PC, PD, CP, RC
RX_ON	Activates RX circuits: BBF, DEMOD, IF AMP, IR MIXER
TX_ON	Activates TX circuits: TX-DRIVER, RAMP GEN. Starts RAMP SIGNAL at RAMP OUT.
Data Word 1 Bit D10	Activates GF in TX mode.
Data Word 1 Bit D9	Activates MCC in TX mode.

Table 4

Mode	TX Mode	RX Mode	RSSI Only
I_CP_SW	0	0	0
PU_REG	1	1	1
PU_VCO	1	1	1
PU_RX/TX	1	1	1
PU_PLL	1	1	1
RX_ON	0	1	1
TX_ON	1	0	1
BB filter	OFF	ON	OFF
Demodulator	OFF	ON	OFF
IF amplifiers and RSSI	OFF	ON	ON
IR mixer	OFF	ON	ON
RX switch	OFF	ON	ON
TX switch	ON	OFF	OFF
TX driver	ON	OFF	OFF
Ramp generator	ON	OFF	OFF
Programmable counter	ON	ON	ON
Voltage-controlled oscillator	ON	ON	ON
Gaussian filter	ON	OFF	OFF
Phase detector / charge pump	ON	ON	ON
Modulation compensation circuit	ON	OFF	OFF
Reference counter	ON	ON	ON
Typ. current consumption / mA @ V_S = 3.2 V	58	64	62

Serial Programming Bus

The transceiver is programmed by the 3-wire bus (CLOCK, DATA and ENABLE).
After setting enable signal to low condition, on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. After enable returning to high condition the programmed information is loaded into the addressed latches, according to the address bit condition (last bit). Additional leading bits are ignored and there is no check made how many pulses arrived during enable-low condition. During enable low condition the bus current is increased to speed up the bus logic.
The programming of the transceiver is separated into two data words. Data word 1 controls mainly the channel information together with settings, which are closely related with the channel. Data word 2 holds setup information, which is adjusted during production.

Data Word 1

MSB																						LSB
Data bits																						Address bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
MC				SC					VS	PA		GF	MCC	GFCS			VCO-DAC				CPCS		1

Data Word 2

Data bits											Address bit
E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	A0
DEMOD-/ RAMP-DAC					MCCS			TEST			0

Data Word 1 Programs

PLL Settings

With the Main Counter bits D19 – D22

MC (Main Counter)							
			D22	D21	D20	D19	S_{MS}
1	0	0	0	0	0	0	64
1	0	0	0	0	0	1	65
1	0	0	...	...	...	...	...
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

With the Swallow Counter bits D14 – D18

SC (Swallow Counter)					
D18	D17	D16	D15	D14	S_{SC} *)
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	... **)
1	1	0	1	1	30
1	1	1	1	0	31

* $S_{SC} = [D14] \times 2^0 + [D15] \times 2^1 + ... [D18] \times 2^4$
** $S_{PGD} = 32 \times S_{MC} + S_{SC}$

VCO Select (RX/TX Mode)

With bit D13

Used to select the suitable VCO in TX- or RX mode

D13	VS (VCO Select)
0	RX-VCO
1	TX-VCO

Output Power Settings

With bits D11 – D12

PA (Output Power Settings)		
D12	D11	PA
0	0	–21 dBm
0	1	–11 dBm
1	0	–4 dBm
1	1	+3 dBm

Gaussian Filter on/off

With bit D10

GF is used only in TX mode

D10	GF (Gaussian Filter)
0	OFF
1	ON

Modulation Compensation Circuit on/off

With bit D9

MCC is used only in TX mode

D9	MCC (Modulation Compensation Circuit)
0	OFF
1	ON

GFCS Adjustment

With bits D6 – D8

Only in TX mode effective for setting the frequency deviation of the modulation

GFCS (Gaussian Filtered Settings)			
D8	D7	D6	GFCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

VCO – DAC Adjustment

With bits D2 – D5

Used to pretune the VCO frequency in case of production tolerances of the device. Tuning voltage in locked condition should be around 1.5 V at room temperature. This gives margin for ambient temperature changes.

Pretune DAC Voltage (Internal Connection)				
D5	D4	D3	D2	Δf_{VCO}
0	0	0	0	–5%
0	0	0	1	...
0	0	1	0	...
0	0	1	1	...
0	1	0	0	...
0	1	0	1	...
0	1	1	0	...
0	1	1	1	0.0%
...	...	...	...	...
1	1	0	1	...
1	1	1	0	...
1	1	1	1	+5%

CPCS Adjustment

With bits D0 – D1

Used to adjust the charge pup current. this can be used to compensate the change of the tuning sensitivity over frequency and device tolerances.

CPCS (Charge-Pump Current Settings)		
D1	D0	CPCS
1	0	80%
1	1	90%
0	0	100%
0	1	110%

Data Word 2 Programs

DEMOD-DAC Adjustment for RX Mode

With bits E6 – E10

Only in RX mode effective. Used to tune the demodulator center frequency and allows to compensate tolerances of external components and the T2901.

Demod DAC Voltage (Internal Connection)					
E10	**E9**	**E8**	**E7**	**E6**	**$F_{IFcenter}$**
0	0	0	0	0	–5%
0	0	0	0	1	...
0	0	0	1	0	...
					...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	5%

RAMP-DAC Adjustment for TX Mode

With bits E6 – E10

Only in TX mode effective. used to tune the power pf the external PA nd allows to compensate tolerances of external components and the T2901.

RAMP DAC Voltage (@ Pin 36 RAMP_OUT)					
E10	**E9**	**E8**	**E7**	**E6**	**V_{RAMP_OUT}**
0	0	0	0	0	1.1 V
0	0	0	0	1	...
0	0	0	1	0	...
					...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	2 V

MCCS Adjustment

With bits E3 – E5

Only in TX mode effective. Adjusts the modulation compensation circuit for closed loop modulation. this adjustment is done with a test sequence of a long stream of ’1’ – ’0’. the correct setting is achieved, if the modulation is not affected by the PLL.

MCCS (Modulation Compensation Settings)			
E5	**E4**	**E3**	**MCCS**
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

Test Mode Settings

With bits E0 – E2

In normal operation Lock detect output is used. All other settings are for test only.

Test Output Pin (@ Pin LD)			
E2	**E1**	**E0**	**Signal at lock detect and PLL mode**
0	0	0	Lock detect mode
0	0	1	PC out divided by two and CP active (phase changed)
0	1	0	RC out divided by two and CP active (phase changed)
0	1	1	MCCTEST (REF_CLK divided by 1664)
1	0	0	CP tristate only
1	0	1	PC out divided by two and CP high impedance
1	1	0	RC out divided by two and CP high impedance
1	1	1	GFTEST (REF_CLK divided by 4)

3-Wire Bus Protocol Timing Diagram

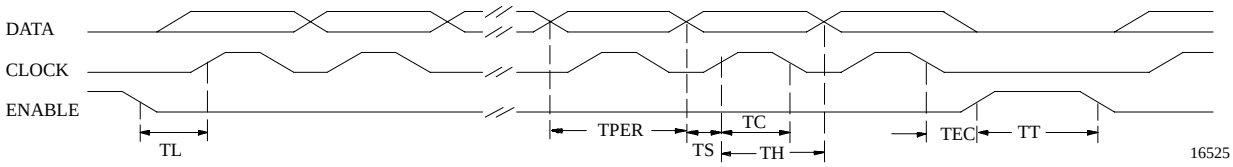
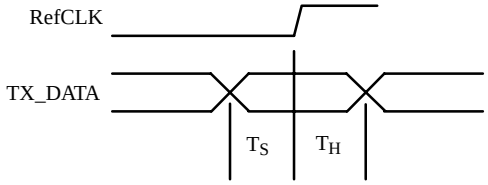


Figure 4. 3-wire bus protocol timing diagram

Description	Symbol	Min. Value	Unit
Clock period	TPER	1/ (6.5 MHz)	µs
Set time data to clock	TS	60	ns
Hold time data to clock	TH	60	ns
Clock pulse width	TC	1/ (13 MHz)	µs
Set time enable to clock	TL	3/ (13 MHz)	µs
Hold time enable to clock	TEC	0	ns
Time between two protocols	TT	3/ (13 MHz)	µs

TX DATA Timing



Set-up time TX DATA	TS	35 ns
Hold time TX DATA	TH	t.b.d.

Figure 5. TX DATA timing

Absolute Maximum Ratings

All voltages are referred to GND (Pins 11, 16, 18, 28, 31 and 43).

Parameter		Symbol	Min.	Max.	Unit
Supply voltage regulator	Pin 10	V_{S_UNREG}	3.2	5.5	V
Supply voltage	Pins 7, 12, 14, 33 and 42	V_S	3.0	5.5	V
Logic input voltage	Pins 1, 2, 3, 38, 39, 44, 45, 46, 47, 48	V_{IN}	– 0.3	V_S	V
Junction temperature		T_{jmax}		125	°C
Storage temperature		T_{stg}	–40	125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	30	K/W

Operating Range

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage regulator	Pin 10	V_{S_UNREG}	3.2	3.6	5.5	V
Regulated supply voltage	Pin 14	V_{S_VCO}	3.0			V
Supply voltage	Pins 7,12, 33 and 42	V_S	3.0	3.0	5.5	V
Ambient temperature		T_{amb}	–25		+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified) : V_{S_UNREG} = 3.2 V, T_{amb} = 25°C.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Receiver						
IR mixer	**Pins 29, 30, 40 and 41**					
Input impedance	@ 2.4 GHz Pin 30	Z_{in}		22 – j7		Ω
Input matching	Pin 30	$VSWR_{in}$		<2:1		
Image rejection ratio	Pins 40 and 41	IRR		20		dB
DSB noise figure	Pins 40 and 41	NFDSB= NFSSB		12		dB
Conversion gain	R_{load} = 400 Ω (differential)	G_{conv}		17		dB
Output interception point	Pins 40 and 41	OIP3		10		dBm
Output impedance	@ 111 MHz (unbalanced) Pins 40 and 41	Z_{out}		77–j3		Ω
IF amplifier	**Pins 26, 27, 34 and 35**					
Input impedance	@ 111 MHz (unbalanced) Pins 34 and 35	Z_{in}		182–j183		Ω
Lower cut-off frequency		fl_{3dB}		40		MHz
Upper cut-off frequency		fu_{3dB}		320		MHz
Power gain		G_p		75		dB
Bandwidth of external tank circuit	Pins 26 and 27	BW_{3dB}		10		MHz
Noise figure		NF		12		dB
RSSI	**Pins 25, 34 and 35**					
RSSI sensitivity	at IF_IN1, IF_IN2 Pins 34 and 35	P_{min}		20		dBµV
RSSI compression	at IF_IN1, IF_IN2 Pins 34 and 35	P_{max}		100		dBµV
RSSI dynamic range		DR		80		dB
RSSI resolution	Slope of the RSSI has to be steady	Acc		±2		dB
RSSI rise time	P_{in} = 30 to 100 dBµV, Pin 25	t_r		1		µs
RSSI fall time	P_{in} = 100 to 30 dBµV, Pin 25	t_f		1		µs

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_{S_UNREG} = 3.2 V, T_{amb} = 25°C.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Quiescent output voltage	@ P_{in} <20 dBµV at IF_IN1, IF_IN2, Pin 25	V_{out}		0.45		V
Maximum output voltage	@ P_{in} =100 dBµV at IF_IN1, IF_IN2, Pin 25	V_{out}		2.25		V
FM demodulator	**Pins 19, 20 and 21**					
Co-channel rejection ratio	Pin = –75 dBm at IR-mixer input	CCRR		10		dB
Sensitivity	Quality factor of external tank circuit approx. 20, $f_{res} = f_{IF}/2$ Pin 21	S		0.6		V/MHz
Amplitude of recovered signal	Nominal deviation of signal ± 160 kHz, Pin 21	A		200		mV_{pp}
Output voltage DC range	Pin 21	$FMout_{DC}$	0.4		V_s–0.4	V
Output impedance	Pin 21	Z_{out}		13		kΩ
Baseband filter	**Pins 23 and 24**					
3 dB bandwidth	C_{ext} = 56 pF Pin 24	PGBW		1.4		MHz
Output voltage DC range	Pin 24	V_{out}	1		Vs–1	V
Transmitter / PLL						
VCOs (internal 2 x f_{osc})						
Tuning range RX–VCO	@ f_{IF} = 111 MHz	$f_{VCO,RX}$	2289		2389	MHz
Tuning range TX–VCO		$f_{VCO,TX}$	2400		2500	MHz
Tuning gain		G_{tune}		30		MHz/V
Frequency control voltage range	Pin 17	V_{tune}	0.4		2.8	V
Phase noise	@ 500 kHz offset Pin 21	N_{VCO}		–105		dBc/Hz
Phase noise, wideband	@ 2 MHz offset Pin 21	N_{VCO}		–120		dBc/Hz
DAC for VCO pretune (internally connected, 3-bit bus programming bus protocol D2 – D5)						
VCO_DAC range	(see bus protocol D2 – D5)			±5		%
PLL						
Scaling factor prescaler		S_{PSC}		32/33		
Scaling factor main counter		S_{MC}	64		79	
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC-coupled sinewave @ 20 ppm accuracy, Pin 4	f_{REF_CLK}		13		MHz
External reference input voltage	AC-coupled sinewave, Pin 4	V_{REF_CLK}	50		250	mV_{RMS}
Scaling factor reference counter	Pin 4	S_{RC}		13		

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_{S_UNREG} = 3.2 V, T_{amb} = 25°C.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Charge pump	**Pin 13**					
Output current 1	$V_{I\_CP\_SW}$ = "0" $V_{CP} = V_{VS\_CP} / 2$	I_{CP_1}		±1		mA
Output current 2	$V_{I\_CP\_SW}$ = "1" $V_{CP} = V_{VS\_CP} / 2$	I_{CP_5}		±5		mA
Current scaling factor	I_{CP} = CPCS x I_{CP_TYP} (see bus protocol D0 – D1)	CPCS	80		110	%
Leakage current		I_L		± 100		pA
Gaussian transmit filter (Gaussian shape B x T = 0.5)						
TX data filter clock	7 taps in filter	f_{TXFCLK}		6.5		MHz
Frequency deviation		G_{FFM_nom}		±160		%
Frequency deviation scaling	$GF_{FM} = GF_{FM\_nom}$ x GFCS (see bus protocol D6 to D8)	GFCS	60		130	%
Modulation compensation						
Oversampling		OVS		1		
Digital sum variation		DSV	–256		+254	
Current scaling factor	(see bus protocol E3 – E5)	MCCS	60		130	%
TX driver	**Pin 32**					
Maximum output power	@ L = 5.6 nH Pin 32 (see bus protocol D11 – D12)	P_{TX}		3		dBm
Minimum output power	@ L = 5.6 nH Pin 32 (see bus protocol D11 – D12)	P_{TX}		–21		dBm
RF leakage	In RX mode	Pleak	–47			dBm
Output impedance	@ L = 5.6 pF, 2.5 GHz, Pin 32	Z_{OUT}		13+j40		Ω
Ramp generator	**Pin 36 and 37**					
Minimum output voltage		V_{min}		0.2		V
Maximum output voltage	(see bus protocol E6 – E10)	V_{max}	1.1		2.0	V
Rise time	Cramp = 270 pF at Pin 37	t_r		5		µs
Fall time	Cramp = 270 pF at Pin 37	t_f		5		µs
Lock detect and test mode output	**Pin 5**					
Lock detect output, test mode output	locked = '1', unlocked = '0' (test modes, see bus protocol E0 ... E2)	LD				
Leakage current at loked	V_{OH} = 3.3 V Pin 5	I_L			5	µA
Saturation voltage at unloked	I_{OL} = 0.5 mA Pin 5	V_{SL}			0.4	V
Auxiliary regulator	**Pins 8, 9 and 10**					
Output voltage	V_{S_UNREG} = 2.3 V Pin 8	V_{REG}	2.9	3.0	3.1	V

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_{S_UNREG} = 3.2 V, T_{amb} = 25°C.

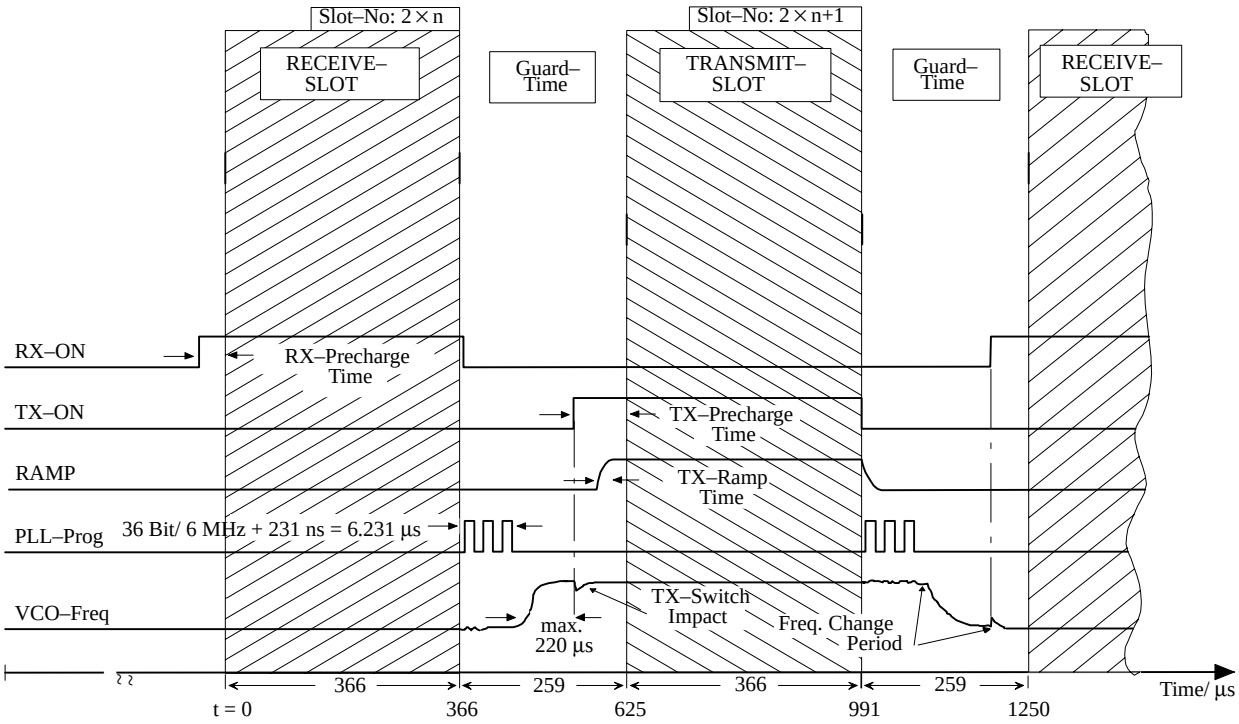
Parameter	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
VCO regulator	**Pins 14, 15 and 16**						
Output voltage	V_{S_VCO} = 3.0 V	Pin 15	V_{REG_vco}	2.6	2.7	2.8	V
3-wire bus	**Pins 1, 2 and 3**						
Clock		Pin 1	f_{Clock}			6	MHz
Logic input levels (CLOCK, DATA, ENABLE, RX_ON, TX_ON, PU_VCO, TX_DATA, I_CP_SW) Pins 1, 2, 3, 4, 38, 39, 47 and 48							
High input level	=‘1’		V_{iH}	1.5			V
Low input level	=‘0’		V_{iL}			0.5	V
High input current	=‘1’		I_{iH}	–5		5	µA
Low input current	=‘0’		I_{iL}	–5		5	µA
Standby control	**Pins 6, 45 and 46**						
Voltage for high input level PU_REG = ‘1’ PU_RX/TX = ‘1’ PU_PLL = ‘1’		Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}	2.0			V
Voltage for low input level PU_REG = ‘0’ PU_RX/TX = ‘0’ PU_PLL = ‘0’		Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}			0.7	V
Input current for high input level PU_REG = ‘1’ PU_RX/TX = ‘1’ PU_PLL = ‘1’	V_{PU_xxxx} = 3 V	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}	20 20 100	30 30 125	40 40 150	µA µA µA
	V_{PU_xxxx} = 5.5 V	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}	60 60 200	80 80 300	100 100 400	µA µA µA
Input current for low input level PU_REG = ‘0’ PU_RX/TX = ‘0’ PU_PLL = ‘0’	V_{PU_xxxx} = 0 V	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}			0.1 0.1 0.1	µA µA µA
	V_{PU_xxxx} = 0.5 V	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}			1 1 1	µA µA µA
Settling time standby to active operation	Switched from V_{PU_xxxx} = ‘0’ to V_{PU_xxxx} = ‘1’		t_{SSA}		< 10		µs
Settling time active operation to standby	Switched from V_{PU_xxxx} = ‘1’ to V_{PU_xxxx} = ‘0’		t_{SAS}		< 2		µs
Power supply	**Pins 7, 10, 12, 14, 33 and 42**						
Total supply current RX mode			I_S		64		mA
Total supply current RSSI mode			I_S		62		mA

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_{S_UNREG} = 3.2 V, T_{amb} = 25°C.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Total supply current TX mode		I_S		58		mA
Total supply current standby mode 1	PU_REG =‘0’ PU_VCO =‘0’ PU_PLL =‘0’ PU_RX/TX =‘0’ RX_ON =‘0’ TX_ON =‘0’	I_S		1		µA
Total supply current standby mode 2	PU_REG =‘1’ PU_VCO =‘1’ PU_PLL =‘1’ PU_RX/TX =‘1’ RX_ON =‘0’ TX_ON =‘0’	I_S		42		µA
Standby current CP	V_{VS_CP} = 3 V, PLL in lock condition Pin 13	I_{CP}		1		µA

Bluetooth RX/TX Timing Diagram



Typical Application Circuit

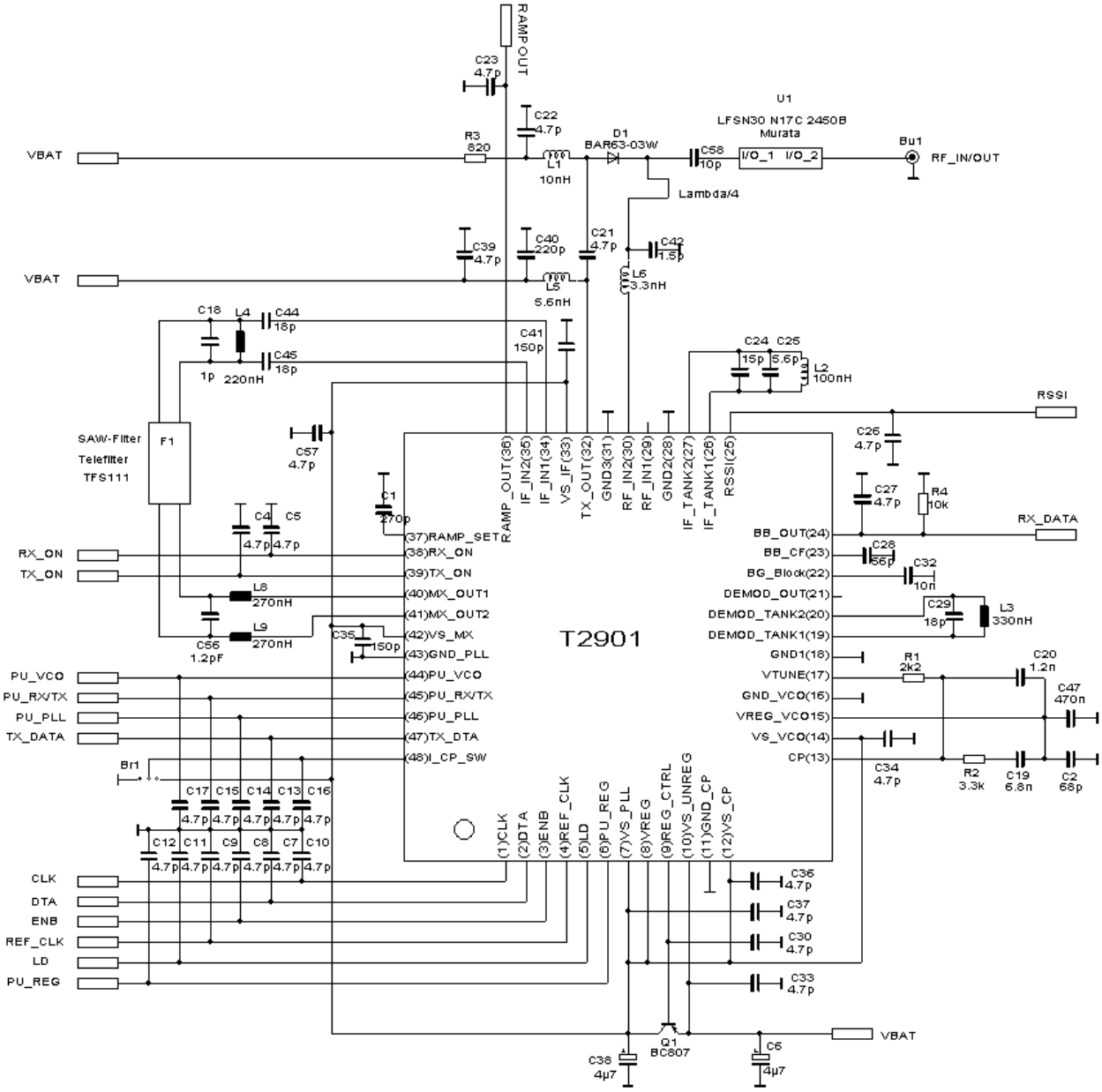
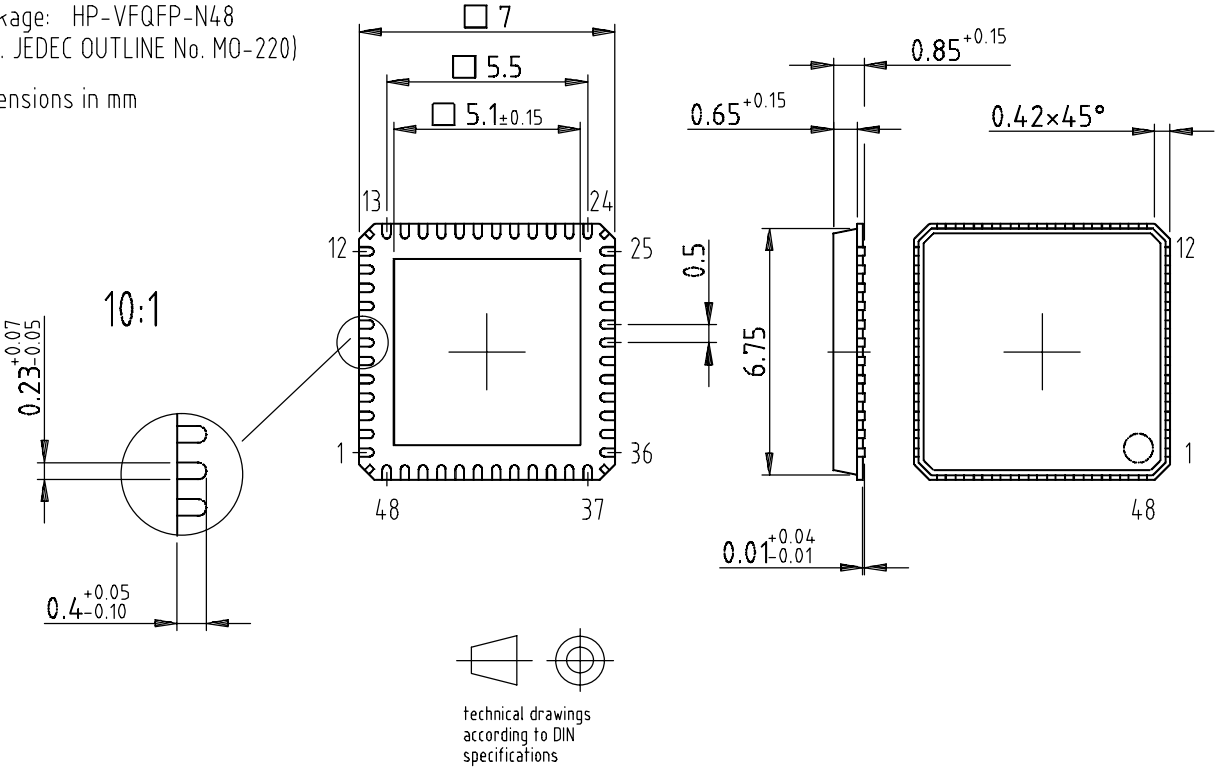


Figure 6. Application circuit

Package Information

Package: HP-VFQFP-N48
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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