# TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP
# TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP
# FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

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- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **1 A Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions**
- **Dropout Voltage Down to 230 mV at 1 A (TPS76850)**
- **Ultralow 85 µA Typical Quiescent Current**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open Drain Power Good (See TPS767xx for Power-On Reset With 200-ms Delay Option)**
- **20-Pin TSSOP (PWP)PowerPAD™ Package**
- **Thermal Shutdown Protection**

**PWP PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| GND/HSINK | 1 | 20 | GND/HSINK |
| GND/HSINK | 2 | 19 | GND/HSINK |
| GND | 3 | 18 | NC |
| NC | 4 | 17 | NC |
| $\overline{EN}$ | 5 | 16 | PG |
| IN | 6 | 15 | FB/NC |
| IN | 7 | 14 | OUT |
| NC | 8 | 13 | OUT |
| GND/HSINK | 9 | 12 | GND/HSINK |
| GND/HSINK | 10 | 11 | GND/HSINK |

NC – No internal connection

## description

This device is designed to have a fast transient response and be stable with 10-µF low ESR capacitors. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 µA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 µA at $T_J$ = 25°C.

Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS768xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS768xx family is available in a 20-pin PWP package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

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**TEXAS INSTRUMENTS**

**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP**
**TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP**
**FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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## description (continued)



**TPS76833 DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE**



**LOAD TRANSIENT RESPONSE**
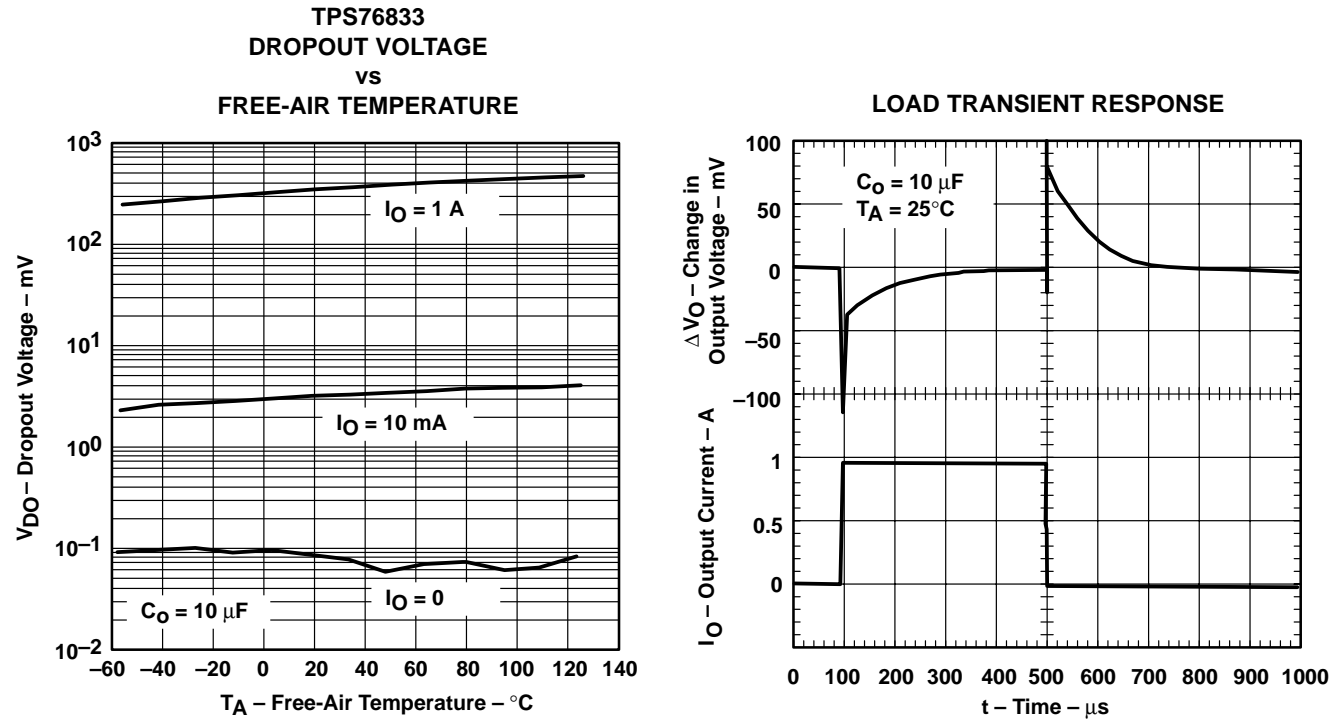
**ORDERING INFORMATION**

| $T_J$ | OUTPUT VOLTAGE (V) TYP | PACKAGE | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| −40°C to 125°C | 5.0 | TSSOP - PWP | Tape and reel | TPS76850QPWPREP | 76850EP |
| | 3.3 | | | TPS76833QPWPREP | 76833EP |
| | 3.0 | | | TPS76830QPWPREP† | 76830EP† |
| | 2.8 | | | TPS76828QPWPREP† | 76828EP† |
| | 2.7 | | | TPS76827QPWPREP† | 76827EP† |
| | 2.5 | | | TPS76825QPWPREP | 76825EP |
| | 1.8 | | | TPS76818QPWPREP | 76818EP |
| | 1.5 | | | TPS76815QPWPREP | 76815EP |
| | Adjustable 1.2 V to 5.5 V | | | TPS76801QPWPREP | 76801EP |

† This device is Product Preview.
The TPS76801 is programmable using an external resistor divider (see application information). The PWP package is available taped and reeled. Note R suffix to the device type (e.g., TPS76801QPWPREP).
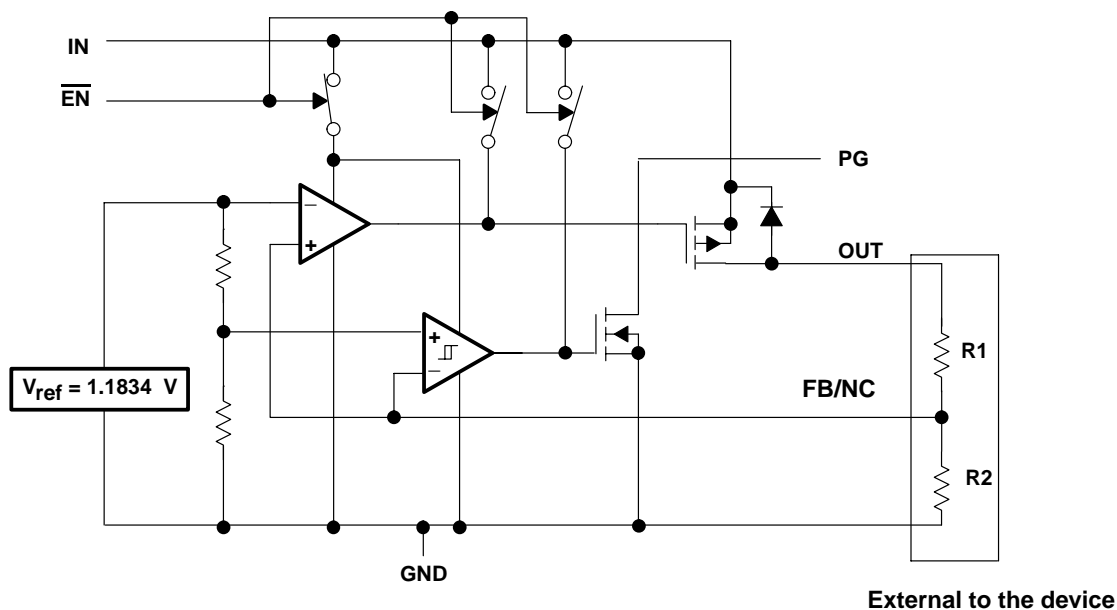
TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

## description (continued)
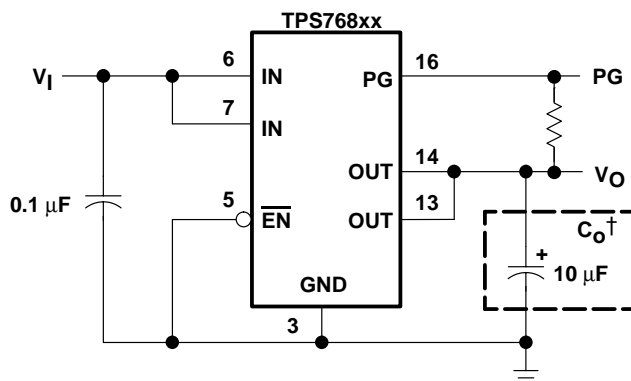


† See application information section for capacitor selection details.

**Figure 1. Typical Application Configuration (For Fixed Output Options)**
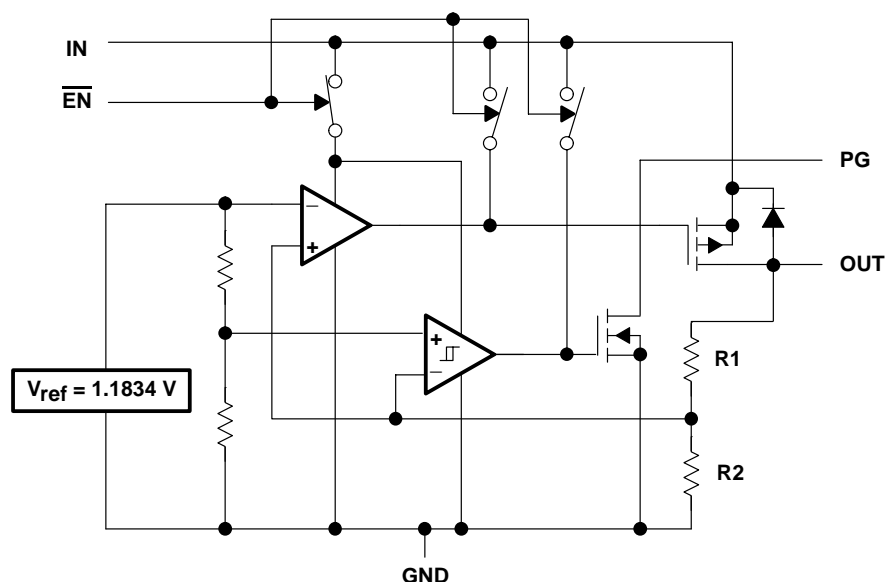
## functional block diagram—adjustable version

## TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP
## TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP
## FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

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### functional block diagram—fixed-voltage version



## Terminal Functions

### PWP Package

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND/HSINK | 1 | | Ground/heatsink |
| GND/HSINK | 2 | | Ground/heatsink |
| GND | 3 | | LDO ground |
| NC | 4 | | No connect |
| EN | 5 | I | Enable input |
| IN | 6 | I | Input |
| IN | 7 | I | Input |
| NC | 8 | | No connect |
| GND/HSINK | 9 | | Ground/heatsink |
| GND/HSINK | 10 | | Ground/heatsink |
| GND/HSINK | 11 | | Ground/heatsink |
| GND/HSINK | 12 | | Ground/heatsink |
| OUT | 13 | O | Regulated output voltage |
| OUT | 14 | O | Regulated output voltage |
| FB/NC | 15 | I | Feedback input voltage for adjustable device (no connect for fixed options) |
| PG | 16 | O | PG output |
| NC | 17 | | No connect |
| NC | 18 | | No connect |
| GND/HSINK | 19 | | Ground/heatsink |
| GND/HSINK | 20 | | Ground/heatsink |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range[‡], $V_I$ ........................................................ −0.3 V to 13.5 V
Voltage range at $\overline{EN}$ ................................................... −0.3 V to $V_I$ + 0.3 V
Maximum PG voltage ...................................................................... 16.5 V
Peak output current ......................................................... Internally limited
Continuous total power dissipation ................................... See dissipation rating tables
Output voltage, $V_O$ (OUT, FB) ......................................................... 7 V
Operating virtual junction temperature range, $T_J$ .................................... −40°C to 125°C
Storage temperature range, $T_{stg}$ ............................................ −65°C to 150°C
ESD rating, HBM ...................................................................... 2 kV

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

| PACKAGE | AIR FLOW (CFM) | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---------|----------------|---------------------------|-------------------------------------|---------------------------|---------------------------|
| PWP[§] | 0 | 2.9 W | 23.5 mW/°C | 1.9 W | 1.5 W |
| | 300 | 4.3 W | 34.6 mW/°C | 2.8 W | 2.2 W |
| PWP[¶] | 0 | 3 W | 23.8 mW/°C | 1.9 W | 1.5 W |
| | 300 | 7.2 W | 57.9 mW/°C | 4.6 W | 3.8 W |

[§] This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

[¶] This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| Input voltage, $V_I$[#] | 2.7 | 10 | V |
| Output voltage range, $V_O$ | 1.2 | 5.5 | V |
| Output current, $I_O$ (see Note 1) | 0 | 1.0 | A |
| Operating virtual junction temperature, $T_J$ (see Note 1) | −40 | 125 | °C |

[#] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

**electrical characteristics over recommended operating free-air temperature range,**
$V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ $\mu$F (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output voltage (10 $\mu$A to 1 A load) (see Note 2) | TPS76801 | 5.5 V $\geq V_O \geq$ 1.5 V, | $T_J$ = 25°C | | $V_O$ | | V |
| | | 5.5 V $\geq V_O \geq$ 1.5 V, | $T_J$ = –40°C to 125°C | 0.98$V_O$ | | 1.02$V_O$ | |
| | TPS76815 | $T_J$ = 25°C, | 2.7 V < $V_{IN}$ < 10 V | | 1.5 | | |
| | | $T_J$ = –40°C to 125°C, | 2.7 V < $V_{IN}$ < 10 V | 1.470 | | 1.530 | |
| | TPS76818 | $T_J$ = 25°C, | 2.8 V < $V_{IN}$ < 10 V | | 1.8 | | |
| | | $T_J$ = –40°C to 125°C, | 2.8 V < $V_{IN}$ < 10 V | 1.764 | | 1.836 | |
| | TPS76825 | $T_J$ = 25°C, | 3.5 V < $V_{IN}$ < 10 V | | 2.5 | | |
| | | $T_J$ = –40°C to 125°C, | 3.5 V < $V_{IN}$ < 10 V | 2.450 | | 2.550 | |
| | TPS76827 | $T_J$ = 25°C, | 3.7 V < $V_{IN}$ < 10 V | | 2.7 | | |
| | | $T_J$ = –40°C to 125°C, | 3.7 V < $V_{IN}$ < 10 V | 2.646 | | 2.754 | |
| | TPS76828 | $T_J$ = 25°C, | 3.8 V < $V_{IN}$ < 10 V | | 2.8 | | |
| | | $T_J$ = –40°C to 125°C, | 3.8 V < $V_{IN}$ < 10 V | 2.744 | | 2.856 | |
| | TPS76830 | $T_J$ = 25°C, | 4 V < $V_{IN}$ < 10 V | | 3.0 | | |
| | | $T_J$ = –40°C to 125°C, | 4 V < $V_{IN}$ < 10 V | 2.940 | | 3.060 | |
| | TPS76833 | $T_J$ = 25°C, | 4.3 V < $V_{IN}$ < 10 V | | 3.3 | | |
| | | $T_J$ = –40°C to 125°C, | 4.3 V < $V_{IN}$ < 10 V | 3.234 | | 3.366 | |
| | TPS76850 | $T_J$ = 25°C, | 6 V < $V_{IN}$ < 10 V | | 5.0 | | |
| | | $T_J$ = –40°C to 125°C, | 6 V < $V_{IN}$ < 10 V | 4.900 | | 5.100 | |
| Quiescent current (GND current) $\overline{EN}$ = 0V, (see Note 2) | | 10 $\mu$A < $I_O$ < 1 A, | $T_J$ = 25°C | | 85 | | $\mu$A |
| | | $I_O$ = 1 A, | $T_J$ = –40°C to 125°C | | | 125 | |
| Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3) | | $V_O$ + 1 V < $V_I \leq$ 10 V, | $T_J$ = 25°C | | 0.01 | | %/V |
| Load regulation | | | | | 3 | | mV |
| Output noise voltage (TPS76818) | | BW = 200 Hz to 100 kHz, $C_O$ = 10 $\mu$F, $I_C$ = 1 A, | $T_J$ = 25°C | | 55 | | $\mu$Vrms |
| Output current limit | | $V_O$ = 0 V | | | 1.7 | 2 | A |
| Thermal shutdown junction temperature | | | | | 150 | | °C |
| Standby current | | $\overline{EN} = V_I$, 2.7 V < $V_I$ < 10 V | $T_J$ = 25°C, | | 1 | | $\mu$A |
| | | $\overline{EN} = V_I$, 2.7 V < $V_I$ < 10 V | $T_J$ = –40°C to 125°C | | | 10 | $\mu$A |
| FB input current | TPS76801 | FB = 1.5 V | | | 2 | | nA |
| High level enable input voltage | | | | 1.7 | | | V |
| Low level enable input voltage | | | | | | 0.9 | V |
| Power supply ripple rejection (see Note 2) | | f = 1 KHz, $C_O$ = 10 $\mu$F, $T_J$ = 25°C | | | 60 | | dB |

NOTES: 2. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.
     3. If $V_O \leq$ 1.8 V then $V_{Imax}$ = 10 V, $V_{Imin}$ = 2.7 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \geq$ 2.5 V then $V_{Imax}$ = 10 V, $V_{Imin}$ = $V_O$ + 1 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP**
**TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP**
**FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**
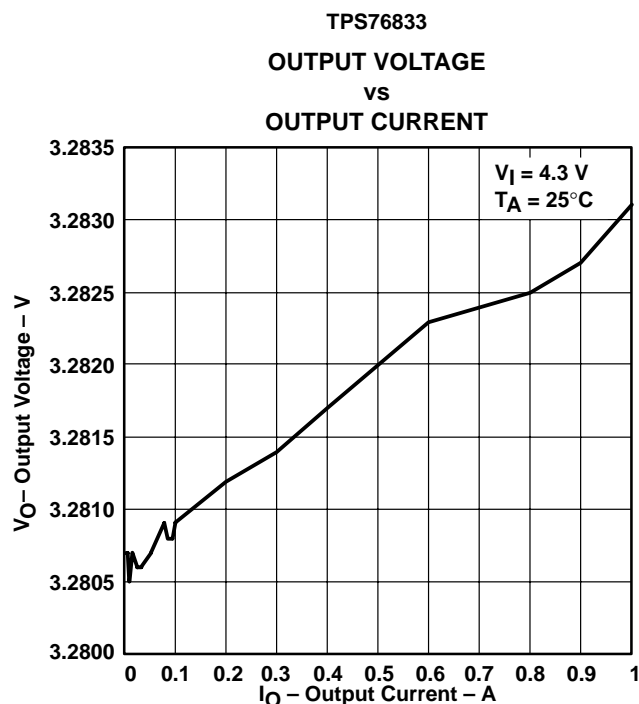
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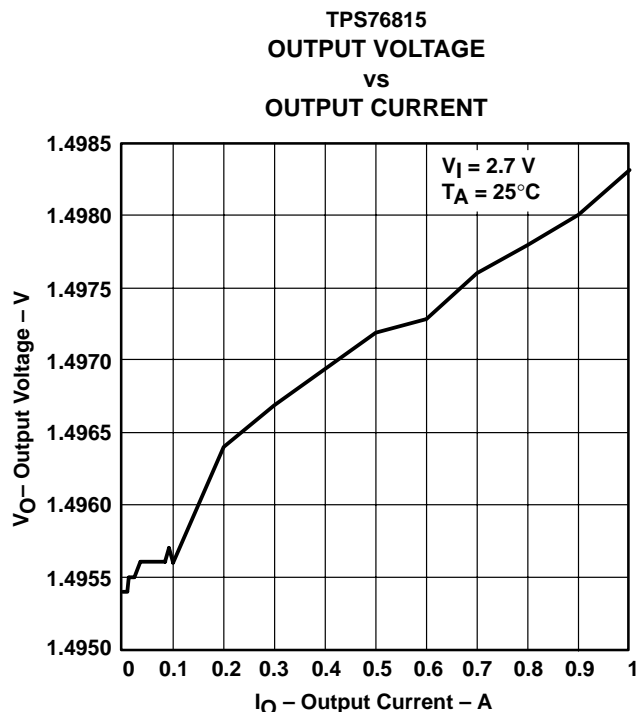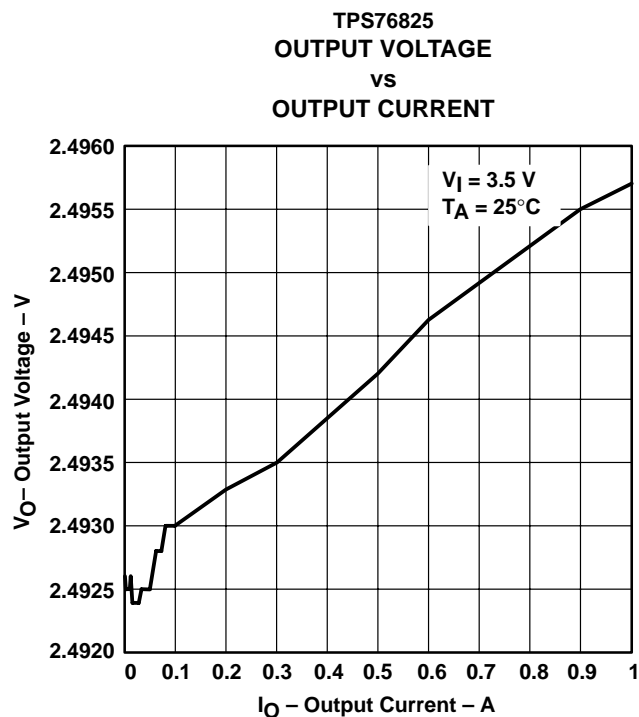
**electrical characteristics over recommended operating free-air temperature range,**
$V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ $\mu$F (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PG | Minimum input voltage for valid PG | $I_{O(PG)} = 300$ $\mu$A | | | 1.1 | | V |
| | Trip threshold voltage | $V_O$ decreasing | | 92 | | 98 | %$V_O$ |
| | Hysteresis voltage | Measured at $V_O$ | | | 0.5 | | %$V_O$ |
| | Output low voltage | $V_I = 2.7$ V, | $I_{O(PG)} = 1$ mA | | 0.15 | 0.4 | V |
| | Leakage current | $V_{(PG)} = 5$ V | | | | 1 | $\mu$A |
| Input current ($\overline{EN}$) | | $\overline{EN} = 0$ V | | −1 | 0 | 1 | $\mu$A |
| | | $\overline{EN} = V_I$ | | −1 | | 1 | |
| Dropout voltage (see Note 4) | TPS76828 | $I_O = 1$ A, | $T_J = 25°C$ | | 500 | | mV |
| | | $I_O = 1$ A, | $T_J = −40°C$ to $125°C$ | | | 825 | |
| | TPS76830 | $I_O = 1$ A, | $T_J = 25°C$ | | 450 | | |
| | | $I_O = 1$ A, | $T_J = −40°C$ to $125°C$ | | | 675 | |
| | TPS76833 | $I_O = 1$ A, | $T_J = 25°C$ | | 350 | | |
| | | $I_O = 1$ A, | $T_J = −40°C$ to $125°C$ | | | 575 | |
| | TPS76850 | $I_O = 1$ A, | $T_J = 25°C$ | | 230 | | |
| | | $I_O = 1$ A, | $T_J = −40°C$ to $125°C$ | | | 380 | |

NOTE 4:   IN voltage equals $V_O(typ) − 100$ mV; TPS76801 output voltage set to 3.3 V nominal with external resistor divider. TPS76815, TPS76818, TPS76825, and TPS76827 dropout voltage limited by input voltage range limitations (i.e., TPS76830  input voltage needs to drop to 2.9 V for purpose of this test).

## TYPICAL CHARACTERISTICS

### Table of Graphs

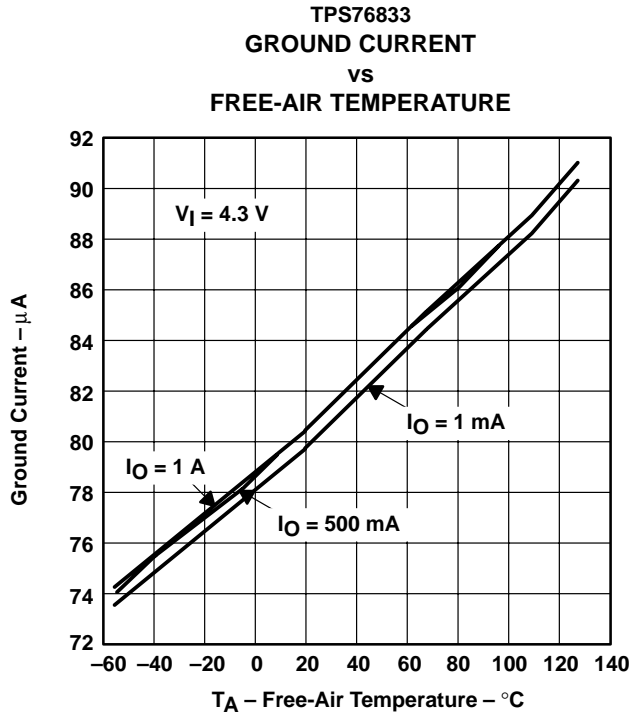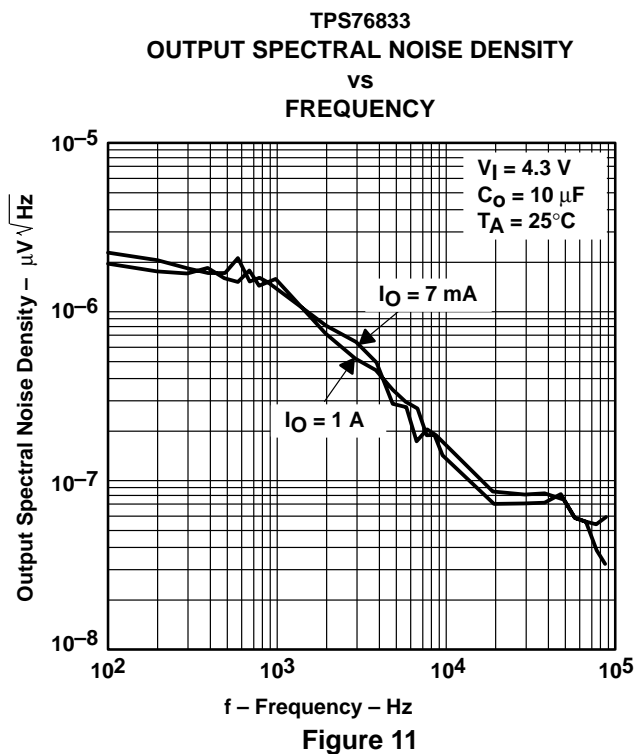| | | | FIGURE |
|---|---|---|---|
| $V_O$ | Output voltage | vs Output current | 2, 3, 4 |
| | | vs Free-air temperature | 5, 6, 7 |
| | Ground current | vs Free-air temperature | 8, 9 |
| | Power supply ripple rejection | vs Frequency | 10 |
| | Output spectral noise density | vs Frequency | 11 |
| | Input voltage (min) | vs Output voltage | 12 |
| $Z_O$ | Output impedance | vs Frequency | 13 |
| $V_{DO}$ | Dropout voltage | vs Free-air temperature | 14 |
| | Line transient response | | 15, 17 |
| | Load transient response | | 16, 18 |
| $V_O$ | Output voltage | vs Time | 19 |
| | Dropout voltage | vs Input voltage | 20 |
| | Equivalent series resistance (ESR) | vs Output current | 22 – 25 |

![Texas Instruments logo]

**TYPICAL CHARACTERISTICS**

TPS76833
OUTPUT VOLTAGE
vs
OUTPUT CURRENT



Figure 2

TPS76815
OUTPUT VOLTAGE
vs
OUTPUT CURRENT



Figure 3

TPS76825
OUTPUT VOLTAGE
vs
OUTPUT CURRENT



Figure 4

TPS76833
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE
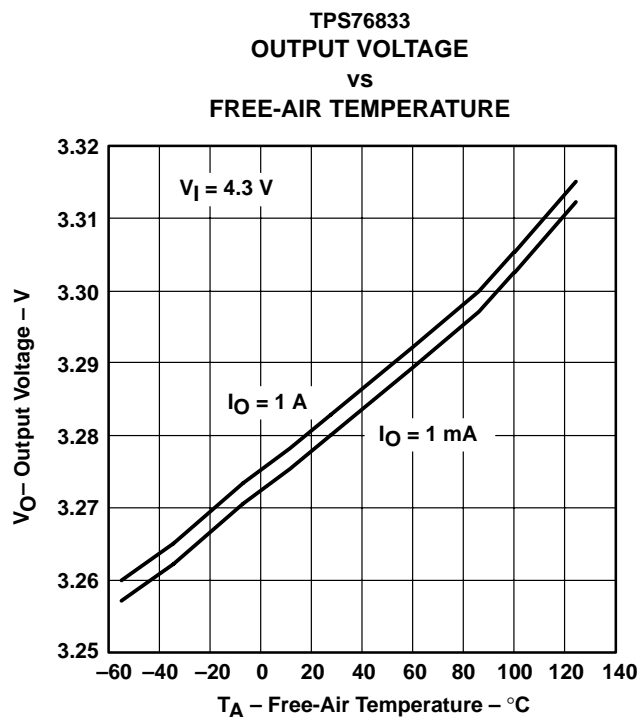


Figure 5

## TYPICAL CHARACTERISTICS

**TPS76815
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



Figure 6

**TPS76825
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



Figure 7

**TPS76833
GROUND CURRENT
vs
FREE-AIR TEMPERATURE**



Figure 8

TEXAS
INSTRUMENTS

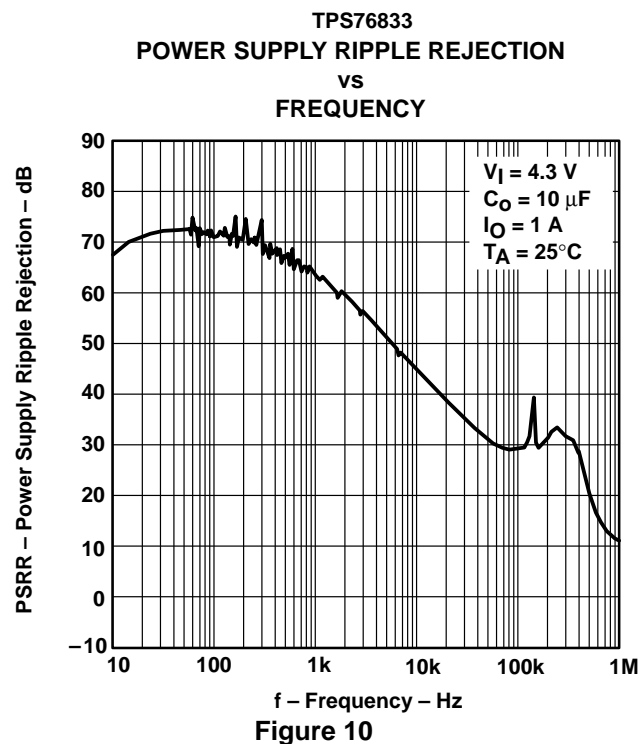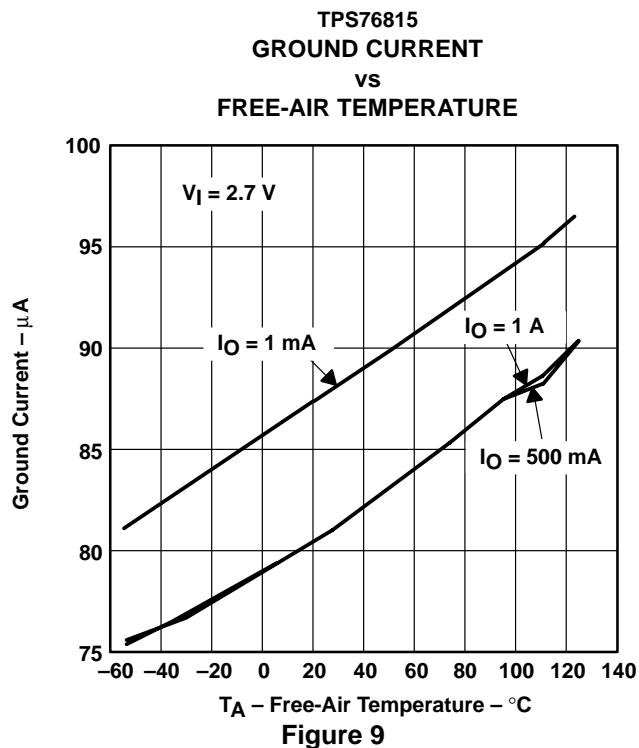**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP**
**TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP**
**FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**
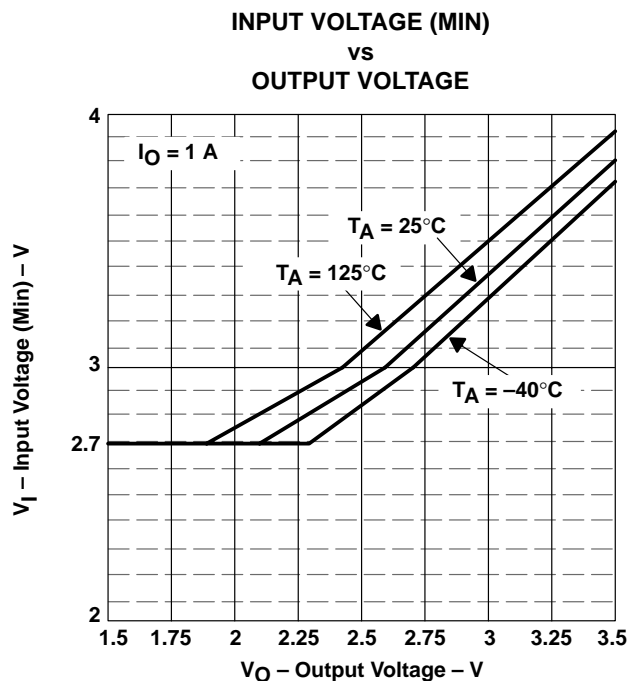
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## TYPICAL CHARACTERISTICS

**TPS76815**
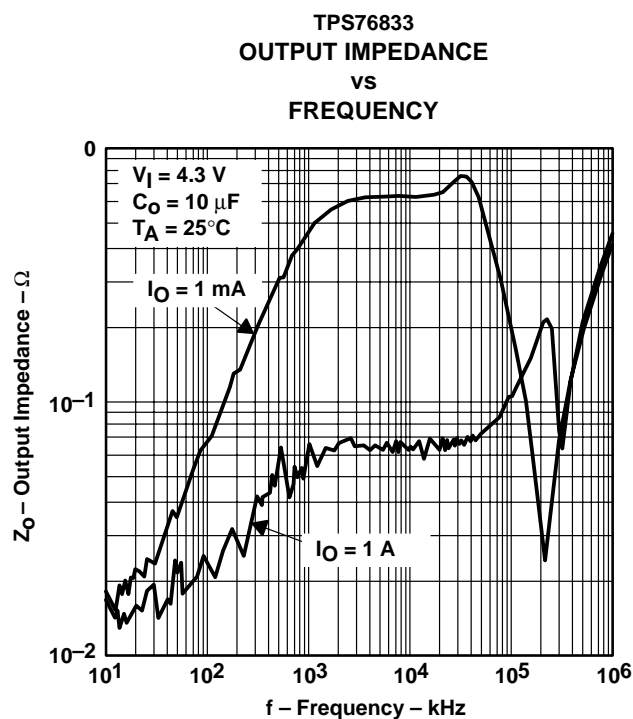**GROUND CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

**TPS76833**
**POWER SUPPLY RIPPLE REJECTION**
**vs**
**FREQUENCY**

**Figure 9**

**Figure 10**

**TPS76833**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**

**Figure 11**

TEXAS
INSTRUMENTS

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**TYPICAL CHARACTERISTICS**

INPUT VOLTAGE (MIN)
vs
OUTPUT VOLTAGE



**Figure 12**

TPS76833
OUTPUT IMPEDANCE
vs
FREQUENCY



**Figure 13**

TPS76833
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



**Figure 14**

## TYPICAL CHARACTERISTICS

TPS76815
LINE TRANSIENT RESPONSE



**Figure 15**

TPS76815
LOAD TRANSIENT RESPONSE



**Figure 16**

TPS76833
LINE TRANSIENT RESPONSE



**Figure 17**

TPS76833
LOAD TRANSIENT RESPONSE



**Figure 18**

TEXAS
INSTRUMENTS

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## TYPICAL CHARACTERISTICS

TPS76833
OUTPUT VOLTAGE
vs
TIME (AT STARTUP)

TPS76801
DROPOUT VOLTAGE
vs
INPUT VOLTAGE
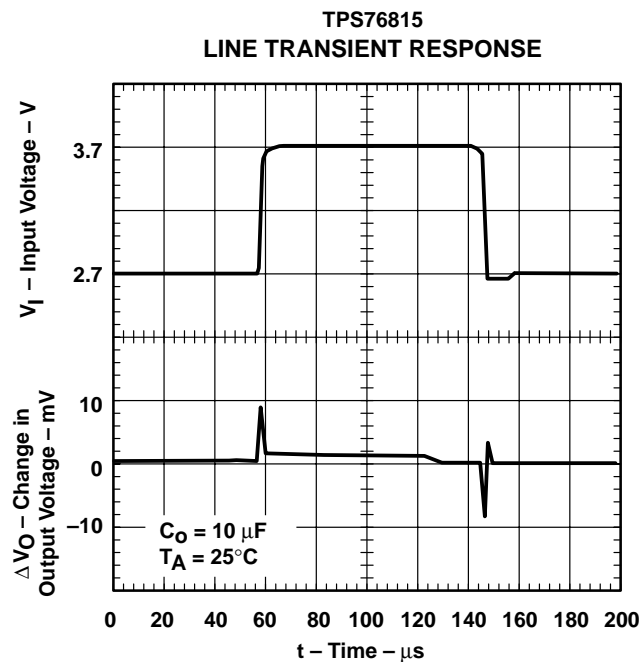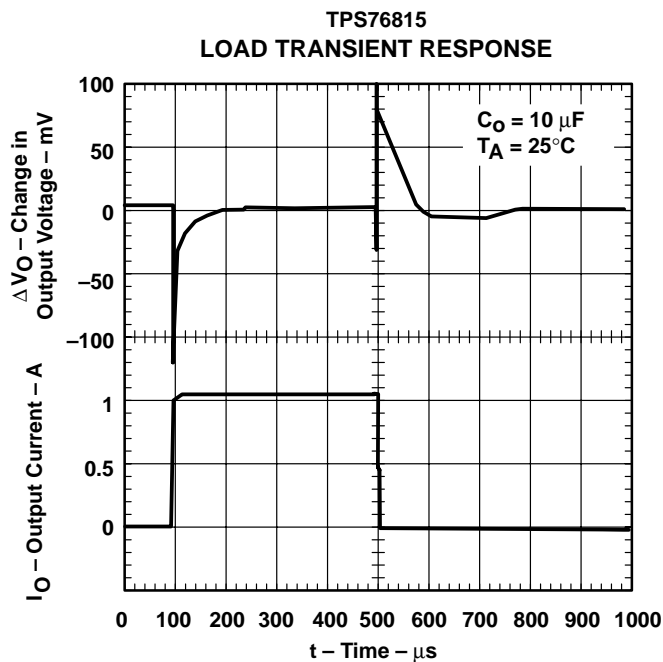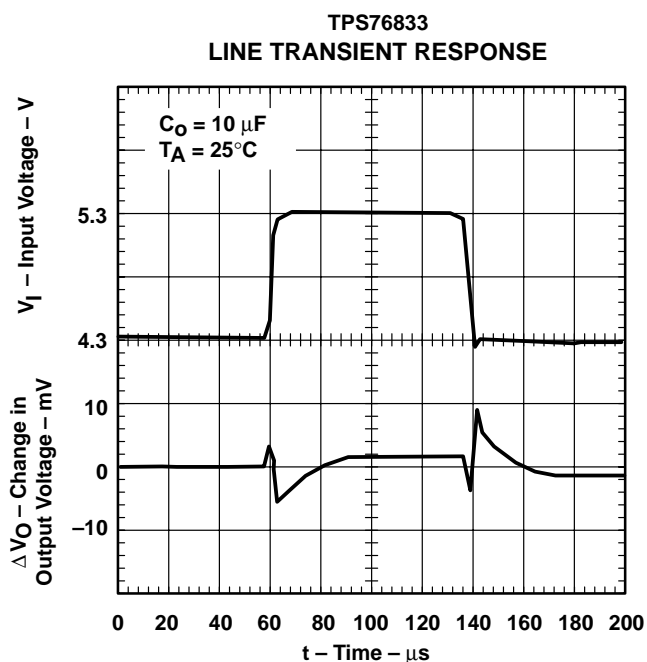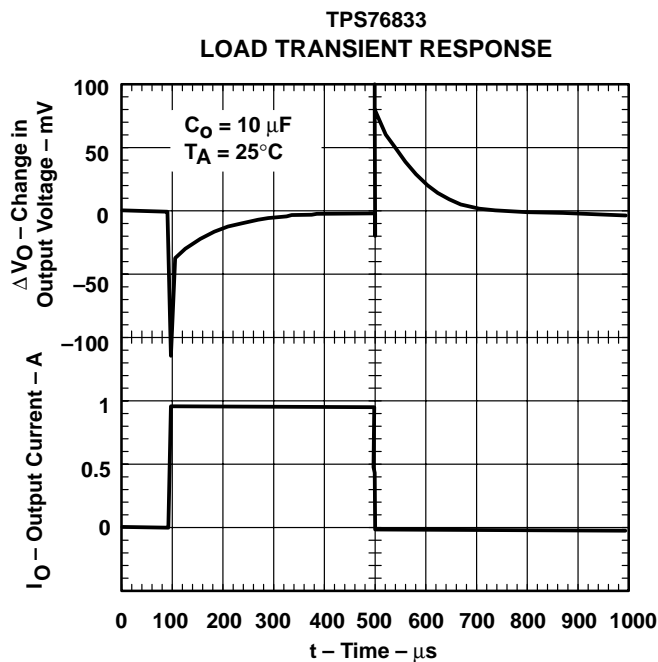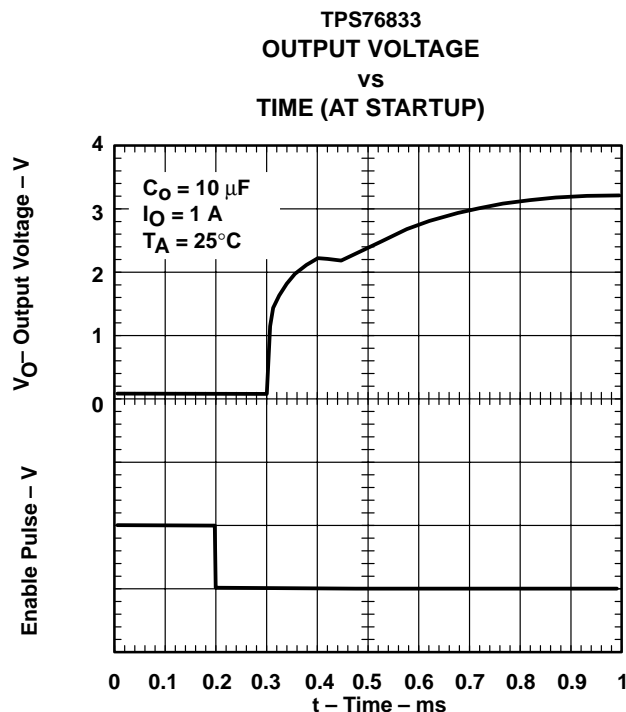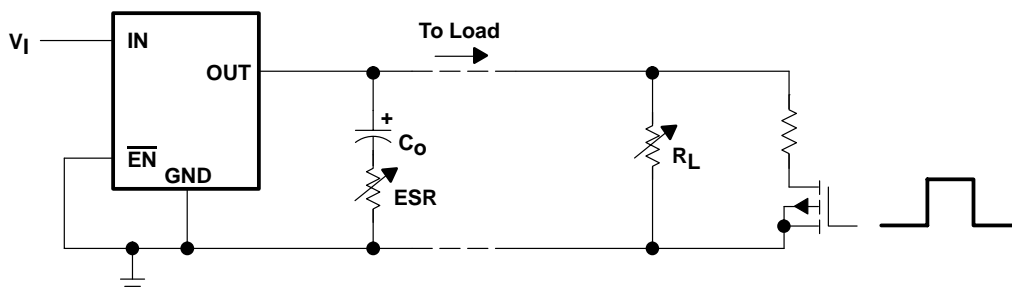
**Figure 19**

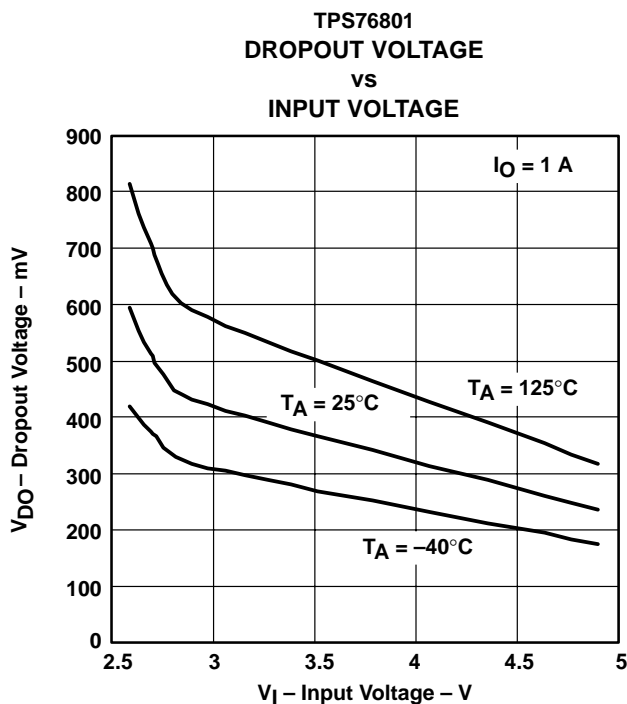**Figure 20**

**Figure 21. Test Circuit for Typical Regions of Stability (Figures 22 through 25) (Fixed Output Options)**
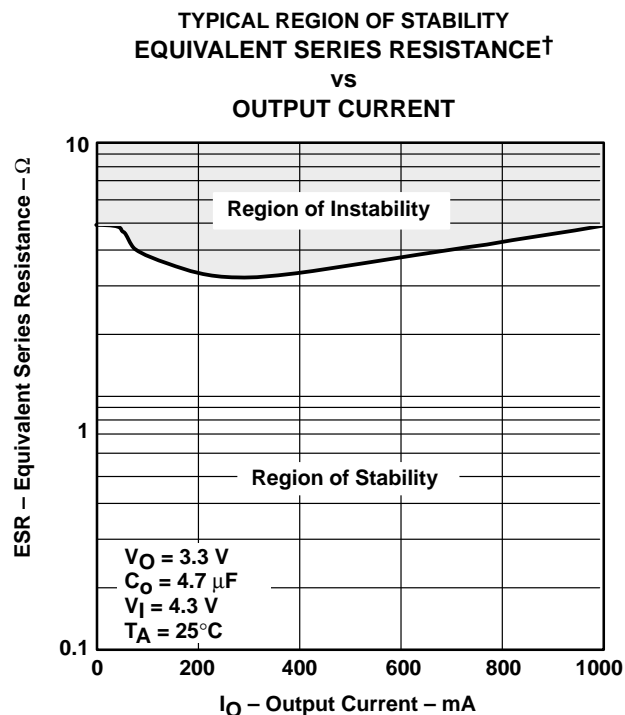
**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP**
**TPS76828-EP, TPS76830-EP TPS76833-EP, TPS76850-EP, TPS76801-EP**
**FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

SGLS011 – MARCH 2003

## TYPICAL CHARACTERISTICS

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

**Figure 22**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

**Figure 23**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

**Figure 24**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

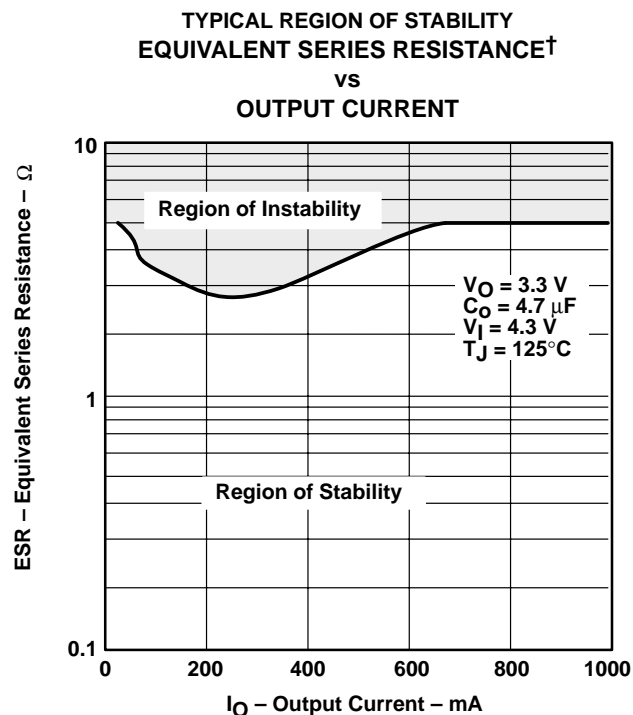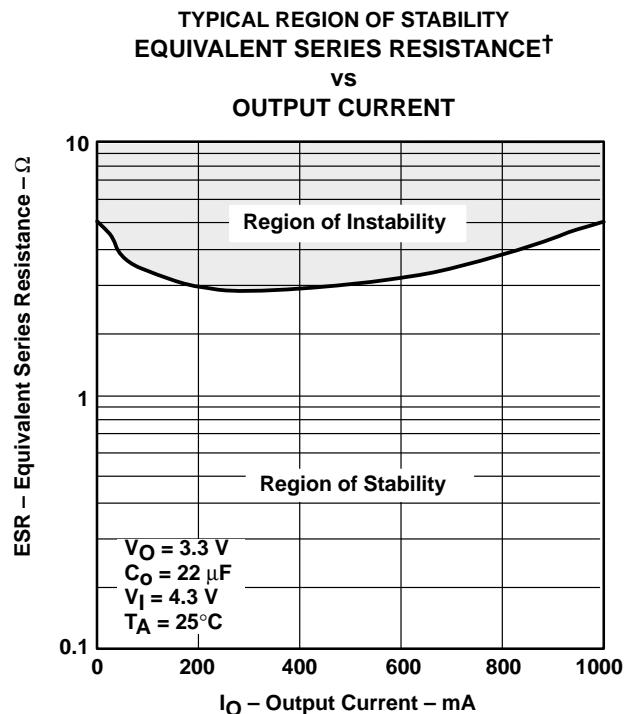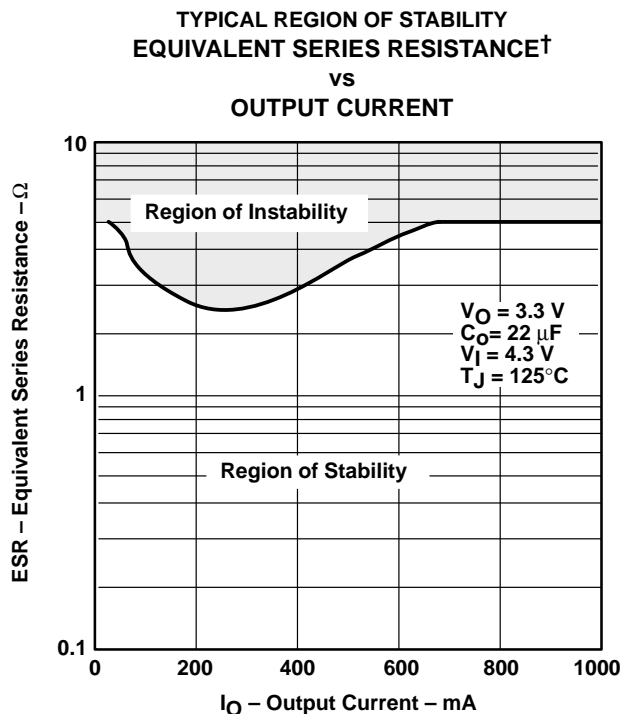**Figure 25**

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to $C_O$.

![Texas Instruments logo]

## APPLICATION INFORMATION

The TPS768xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and offers an adjustable device, the TPS76801 (adjustable from 1.2 V to 5.5 V).

### device operation

The TPS768xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS768xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in $\beta$ forces an increase in $I_B$ to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS768xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS768xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 $\mu$A. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

### minimum load requirements

The TPS768xx family is stable even at zero load; no minimum load is required for operation.

### FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 27. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

### external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 $\mu$F or larger) improves load transient response and noise rejection if the TPS768xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS768xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 $\mu$F and the ESR (equivalent series resistance) must be between 50 m$\Omega$ and 1.5 $\Omega$. Capacitor values 10 $\mu$F or larger are acceptable, provided the ESR is less than 1.5 $\Omega$. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 $\mu$F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

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## APPLICATION INFORMATION

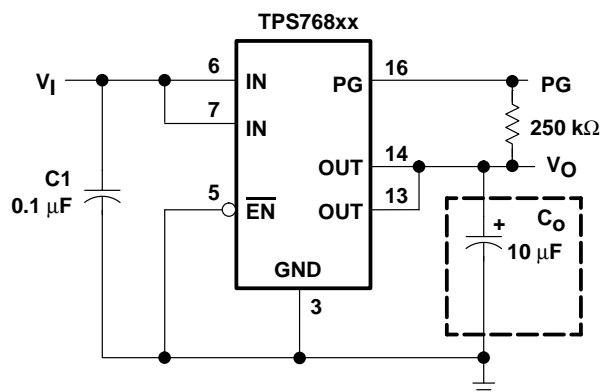### external capacitor requirements (continued)



**Figure 26. Typical Application Circuit (Fixed Versions)**

### programming the TPS76801 adjustable LDO regulator

The output voltage of the TPS76801 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \qquad (1)$$

Where:

$V_{ref}$ = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \qquad (2)$$
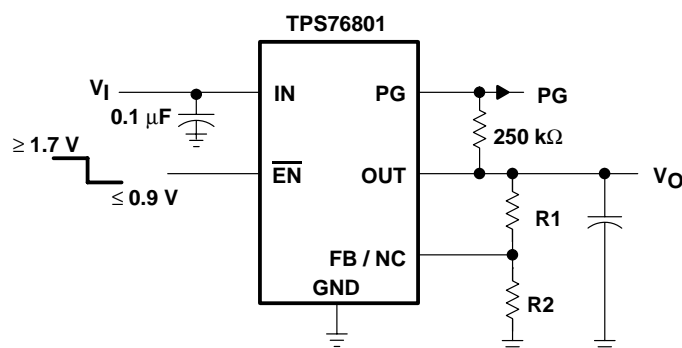


**OUTPUT VOLTAGE PROGRAMMING GUIDE**

| OUTPUT VOLTAGE | R1 | R2 | UNIT |
|---|---|---|---|
| 2.5 V | 33.2 | 30.1 | kΩ |
| 3.3 V | 53.6 | 30.1 | kΩ |
| 3.6 V | 61.9 | 30.1 | kΩ |
| 4.75 V | 90.8 | 30.1 | kΩ |

**Figure 27. TPS76801 Adjustable LDO Regulator Programming**

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## APPLICATION INFORMATION

**power-good indicator**

The TPS768xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

**regulator protection**

The TPS768xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS768xx also features internal current limiting and thermal protection. During normal operation, the TPS768xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

**power dissipation and junction temperature**

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

## MECHANICAL DATA

**PWP (R-PDSO-G\*\*)**                                              **PowerPAD™ PLASTIC SMALL-OUTLINE**

**20 PINS SHOWN**

| PINS \*\* | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|
| **A MAX** | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| **A MIN** | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

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NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusions.
        D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
           This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
        E. Falls within JEDEC MO-153

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**PWP (R-PDSO-G\*\*)**          **PowerPAD™ PLASTIC SMALL-OUTLINE**

**20 PINS SHOWN**

| | PINS ** | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| DIM | | | | | | |
| **A MAX** | | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| **A MIN** | | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4073225/F 10/98

NOTES:  A.  All linear dimensions are in millimeters.
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            This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
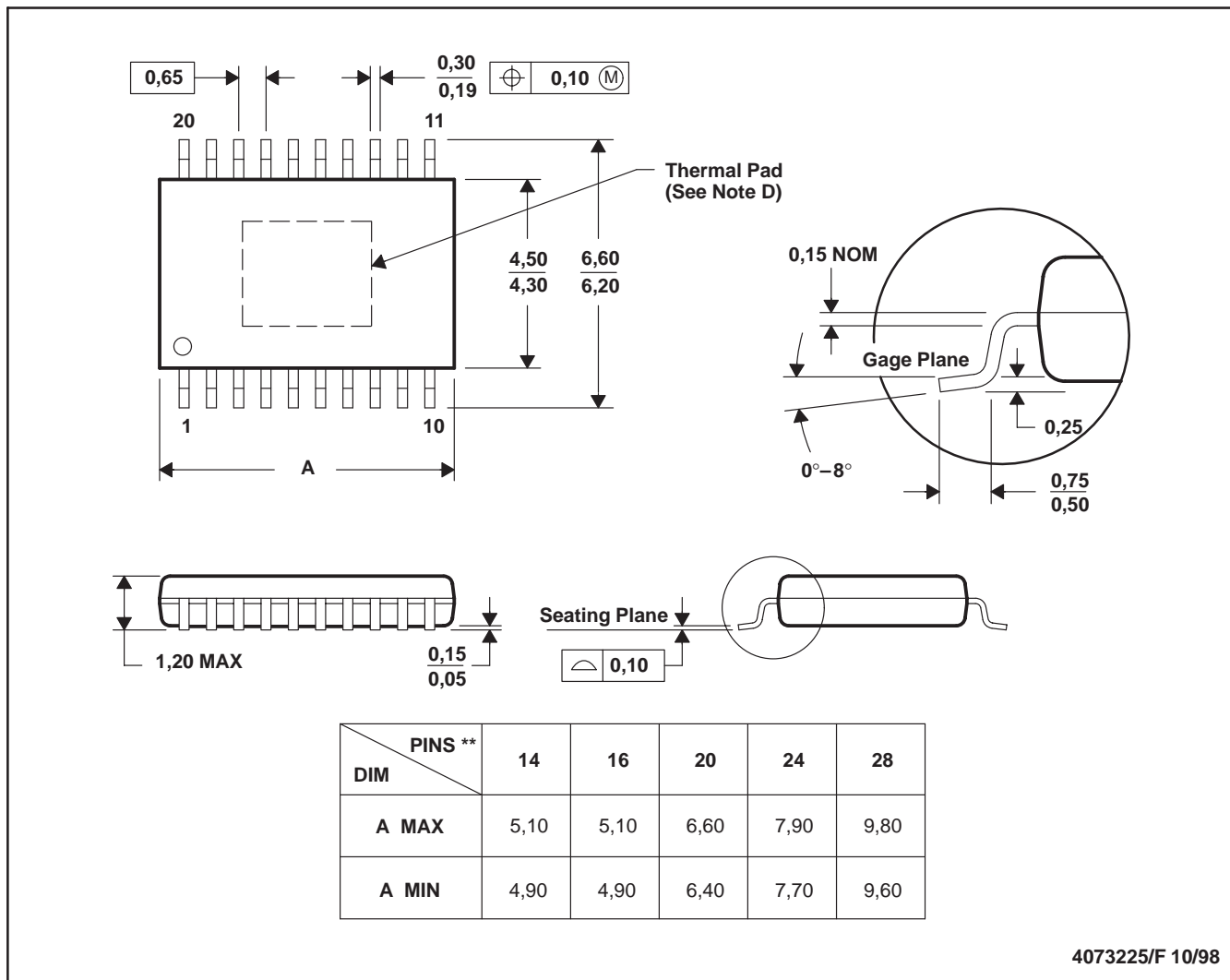        E.  Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265