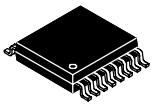


Actual Size
(5,1 mm x 4,9 mm)

SLUS534A – SEPTEMBER 2002 – REVISED FEBRUARY 2003

SINGLE-CELL LI OR DUAL CELL BOOST CONVERTER

FEATURES

- **Synchronous (96% Efficient) Boost Converter With 1000-mA Output Current From 1.8-V Input**
- **Available in a TSSOP-16 Package**
- **Device Quiescent Current . . 20-μA (Typ)**
- **Input Voltage Range . . 1.8-V to 5.5-V**
- **Adjustable Output Voltage Up to 5.5-V Fixed Output Voltage Options**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Low Battery Comparator**
- **Low EMI-Converter (Integrated Antiringing Switch)**
- **Load Disconnect During Shutdown**
- **Over-Temperature Protection**
- **EVM Available (TPS6103xEVM–208)**

APPLICATIONS

- **All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment**

DESCRIPTION

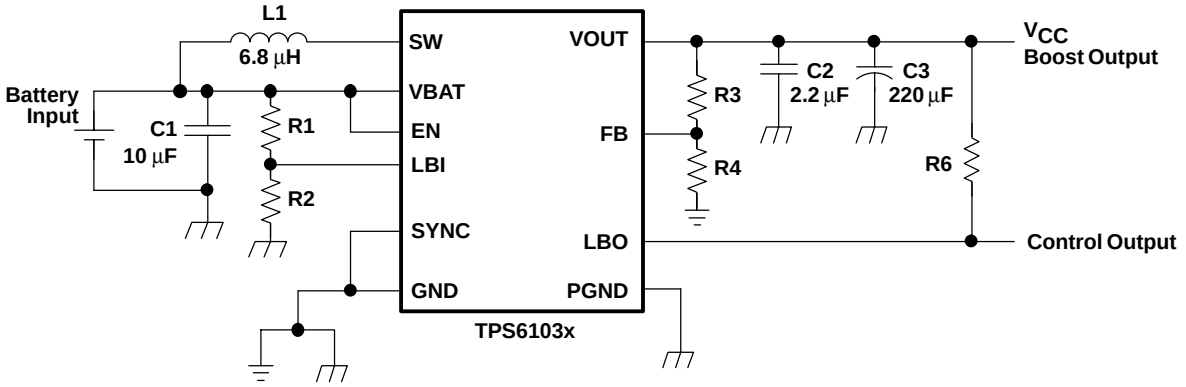
The TPS6103x devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer, or a two-cell alkaline, NiCd or NiMH battery and required supply currents up to or higher than 1 A. The converter generates a stable output voltage that is either adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 1 A at 5 V at a supply voltage down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. Boost switch and rectifier switch are connected internally to provide the lowest leakage inductance and best EMI behavior possible.

The maximum peak current in the boost switch is limited to a value of 4500 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electro-magnetic energy when the converter enters the discontinuous conduction mode.

The output voltage can be programmed by an external resistor divider or is fixed internally on the chip.

The device is packaged in a 16-pin TSSOP PowerPAD™ (16 PWP) package.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE	CODE
16-Pin TSSOP PowerPAD	PWP

AVAILABLE OUTPUT VOLTAGE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PART NUMBER(2)
–40°C to 85°C	Adjustable	TPS61030PWP
	3.3 V	TPS61031PWP
	5 V	TPS61032PWP

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The PW package is available taped and reeled. Add R suffix to device type (e.g., TPS61030PWPR) to order quantities of 2000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	TPS6103X
Input voltage range on LBI	–0.3 V to 3.6 V
Input voltage range on SW, VOUT, LBO, VBAT, SYNC, EN, FB	–0.3 V to 7 V
Operating free air temperature range T_A	–40°C to 85°C
Maximum junction temperature T_J	150°C
Storage temperature range T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT, V_I	1.8		5.5	V
Inductor, L	2.2	6.8		µH
Input capacitor, C_i		10		µF
Output capacitor, C_o	22	100		µF
Operating virtual junction temperature, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

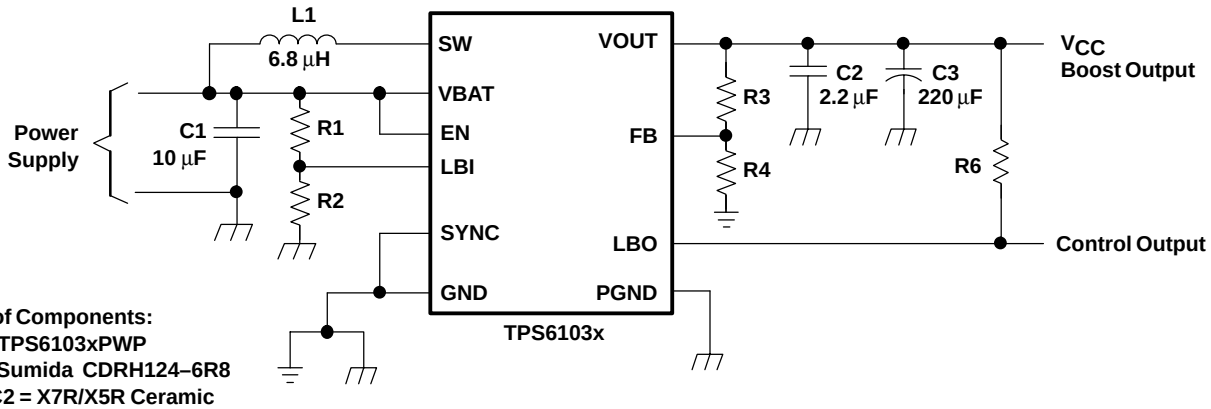
DC/DC STAGE

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range			1.8		5.5	V
V_O	TPS61030 output voltage range			1.8		5.5	V
V_{FB}	TPS61030 feedback voltage			490	500	510	mV
f	Oscillator frequency			500	600	700	kHz
	Frequency range for synchronization			500		700	kHz
I_{SW}	Switch current limit		VOUT= 5 V	3600	4000	4500	mA
	Start-up current limit				$0.4 \times I_{SW}$		mA
	SWN switch on resistance		VOUT= 5 V		55		mΩ
	SWP switch on resistance		VOUT= 5 V		55		mΩ
	Total accuracy					3%	
	Line regulation					0.6%	
	Load regulation					0.6%	
	Quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT =5 V		10	25	µA
		VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 5 V		10	20	µA
	Shutdown current		V_{EN} = 0 V, VBAT = 2.4 V		0.1	1	µA

CONTROL STAGE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Under voltage lockout threshold	V_{LBI} voltage decreasing		1.5		V
V_{IL}	LBI voltage threshold	V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis			10		mV
	LBI input current	EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage	V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current			100		µA
	LBO output leakage current	V_{LBO} = 7 V		0.01	0.1	µA
V_{IL}	EN, SYNC input low voltage				$0.2 \times$ VBAT	V
V_{IH}	EN, SYNC input high voltage		$0.8 \times$ VBAT			V
	EN, SYNC input current	Clamped on GND or VBAT		0.01	0.1	µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

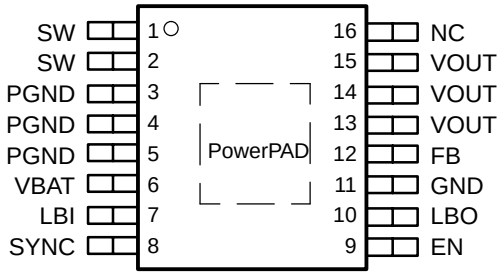
PARAMETER MEASUREMENT INFORMATION



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2 = X7R/X5R Ceramic
C3 = Low ESR Tantalum

PIN ASSIGNMENTS

PWP PACKAGE
(TOP VIEW)



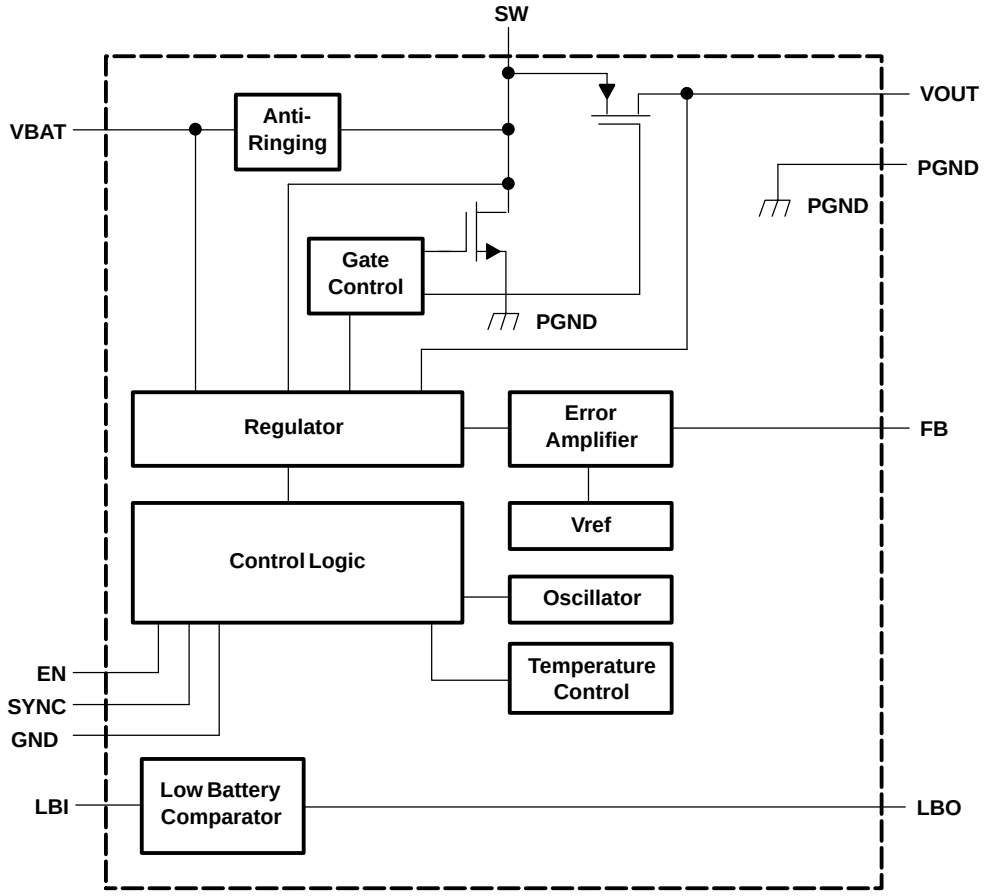
NC – No internal connection

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	9	I	Enable input. (1/VBAT enabled, 0/GND disabled)
FB	12	I	Voltage feedback of adjustable versions
GND	11	I/O	Control/logic ground
LBI	7	I	Low battery comparator input (comparator enabled with EN)
LBO	10	O	Low battery comparator output (open drain)
NC	16		Not connected
SYNC	8	I	Enable/disablepower save mode (1: VBAT disabled, 0: GND enabled, clock signal for synchronization)
SW	1, 2	I	Boost and rectifying switch input
PGND	3, 4, 5	I/O	Power ground
VBAT	6	I	Supply voltage
VOUT	13, 14, 15	O	DC/DC output
PowerPAD™			Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.

PowerPAD is a trademark of Texas Instruments.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DC/DC CONVERTER		FIGURE
Maximum output current	vs Input voltage	1, 2
Efficiency	vs Output current (TPS61030) (V_O = 2.5 V, V_I = 1.8 V, VSYNC = 0 V)	3
	vs Output current (TPS61031) (V_O = 3.3 V, V_I = 1.8 V, 2.4 V, VSYNC = 0 V)	4
	vs Output current (TPS61032) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V, VSYNC = 0 V)	5
	vs Input voltage (TPS61031) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	6
	vs Input voltage (TPS61032) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	7
Output voltage	vs Output current (TPS61031) (V_I = 2.4 V)	8
	vs Output current (TPS61032) (V_I = 3.3 V)	9
No-load supply current into VBAT	vs Input voltage (TPS61032)	10
No-load supply current into VOUT	vs Input voltage (TPS61032)	11
Minimum load resistance at start-up	vs Input voltage (TPS61032)	12
Waveforms	Output voltage in continuous mode (TPS61032)	13
	Output voltage in power save mode (TPS61032)	14
	Load transient response (TPS61032)	15
	Line transient response (TPS61032)	16
	DC/DC converter start-up after enable (TPS61032)	17

TPS61031
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

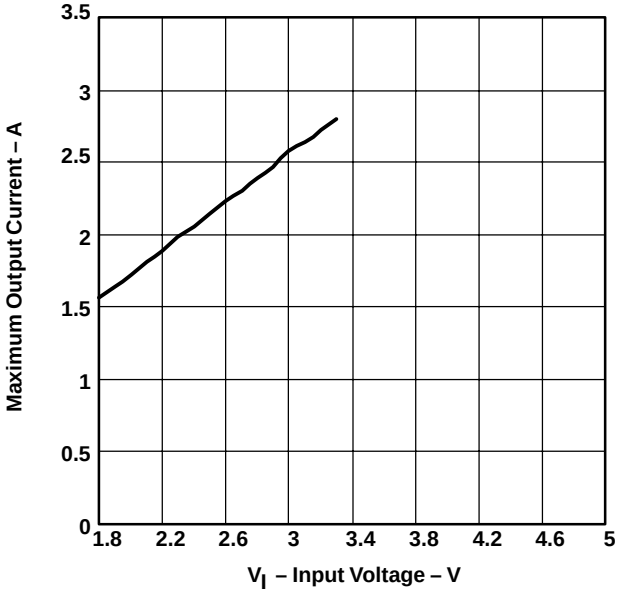


Figure 1

TPS61032
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

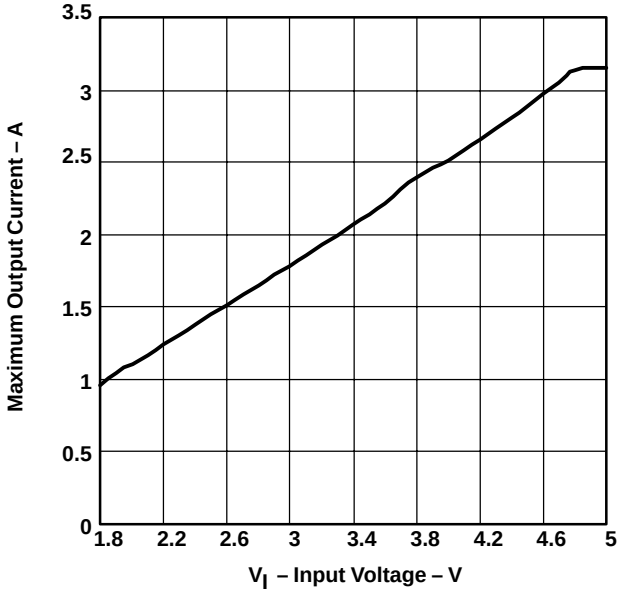


Figure 2

TPS61030
EFFICIENCY
vs
OUTPUT CURRENT

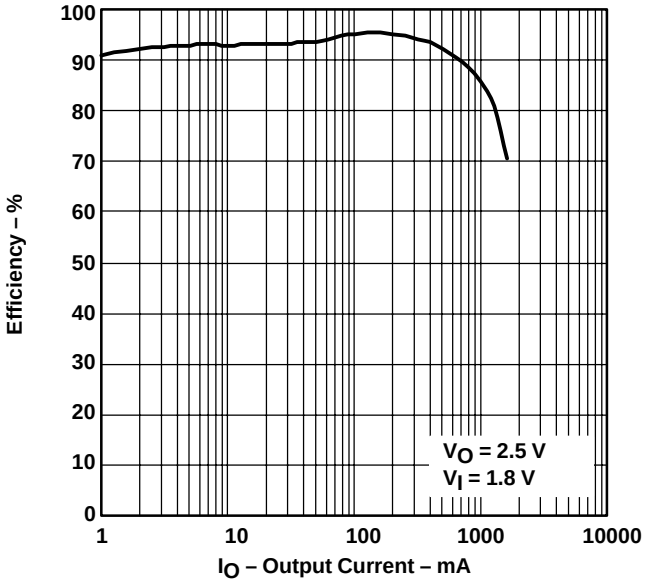


Figure 3

TPS61031
EFFICIENCY
vs
OUTPUT CURRENT

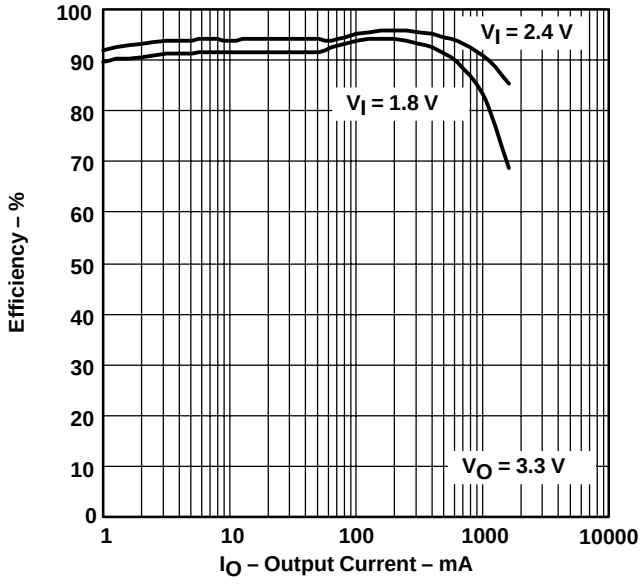


Figure 4

TPS61032
EFFICIENCY
vs
OUTPUT CURRENT

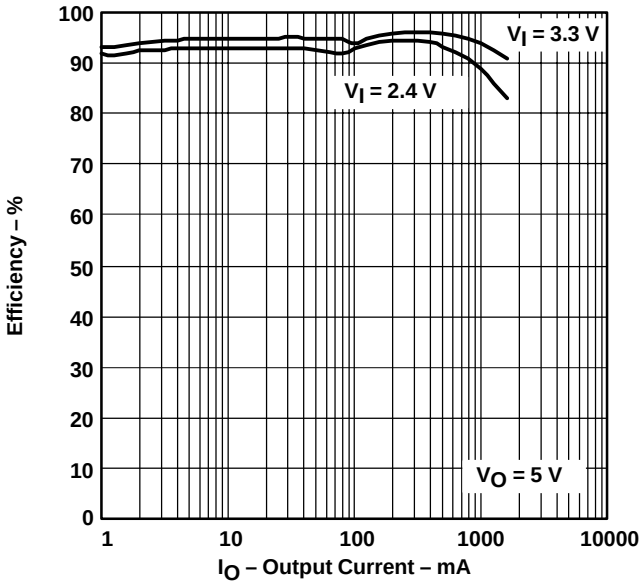


Figure 5

TPS61031
EFFICIENCY
vs
INPUT VOLTAGE

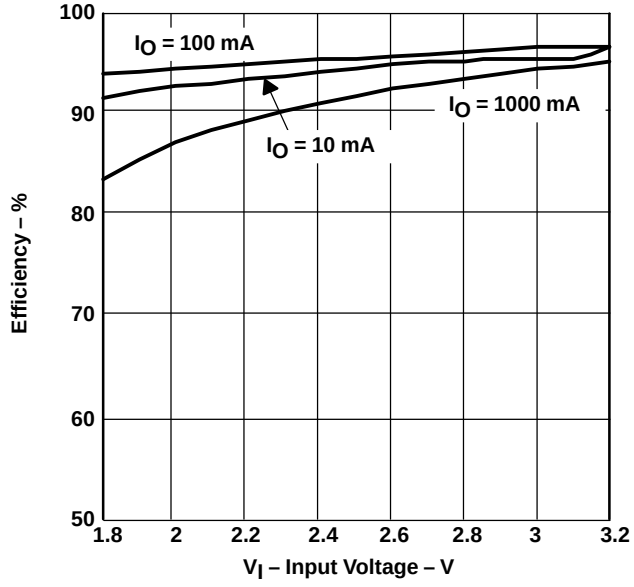


Figure 6

TPS61032
EFFICIENCY
vs
INPUT VOLTAGE

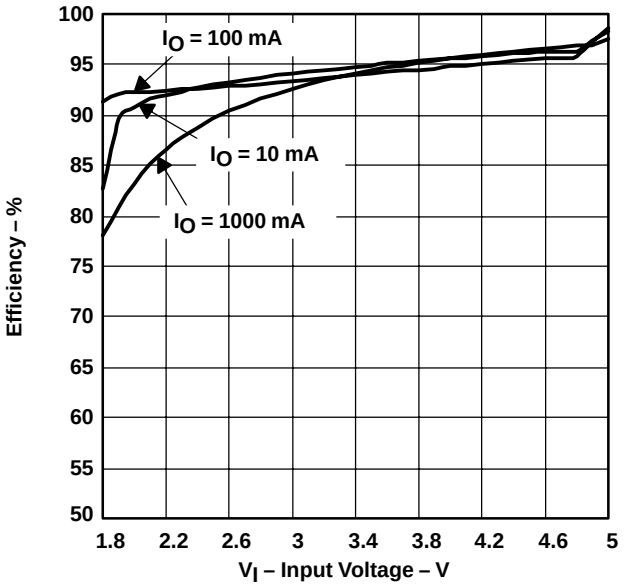


Figure 7

TPS61031
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

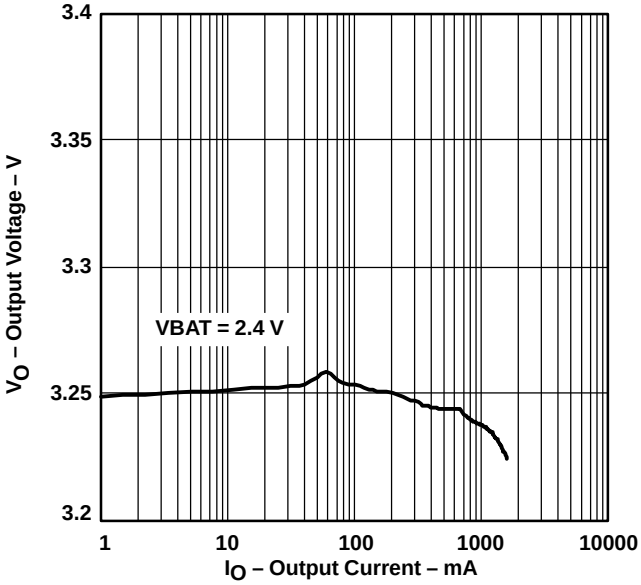


Figure 8

TPS61032
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

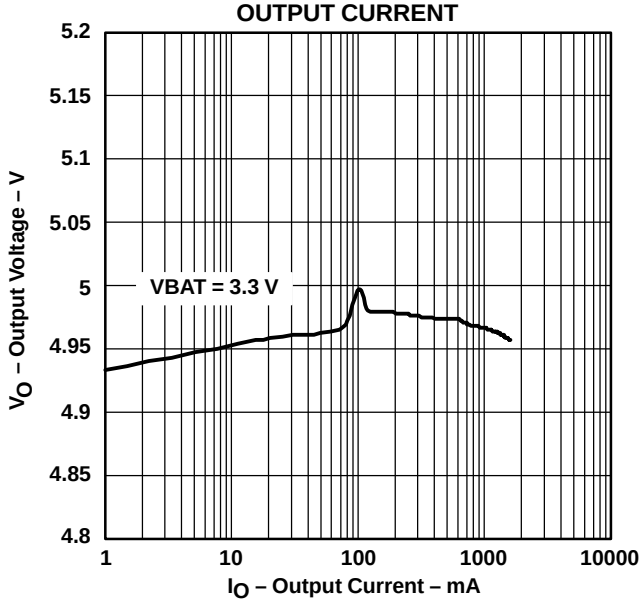


Figure 9

TPS61032
NO-LOAD SUPPLY CURRENT INTO VBAT
vs
INPUT VOLTAGE

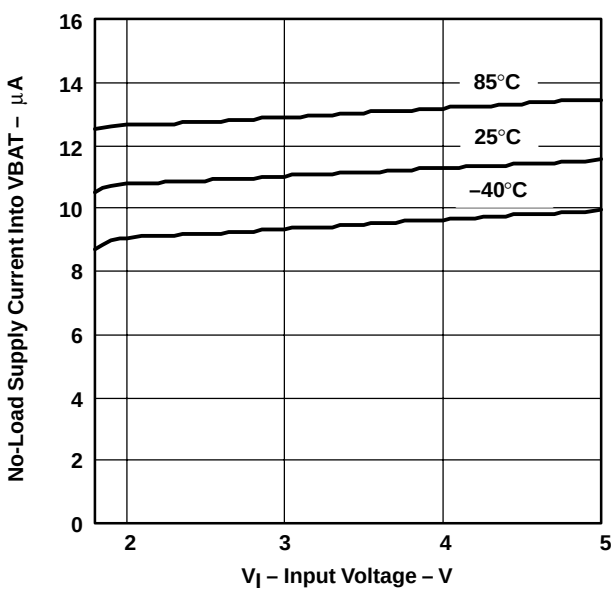


Figure 10

TPS61032
NO-LOAD SUPPLY CURRENT INTO VOUT
vs
INPUT VOLTAGE

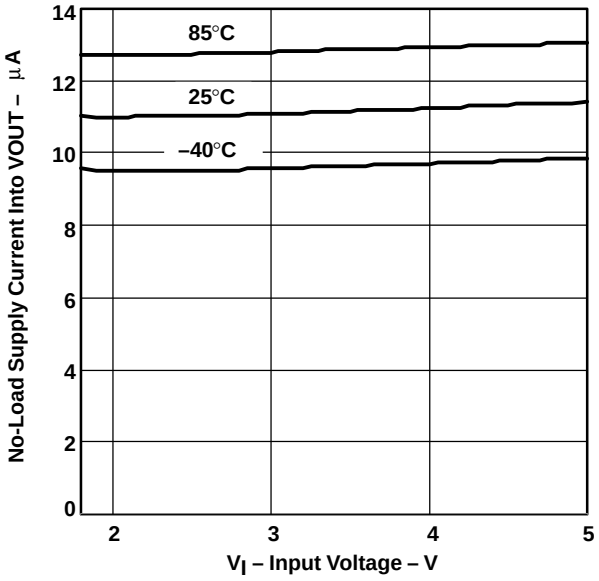


Figure 11

MINIMUM LOAD RESISTANCE AT START-UP
vs
INPUT VOLTAGE

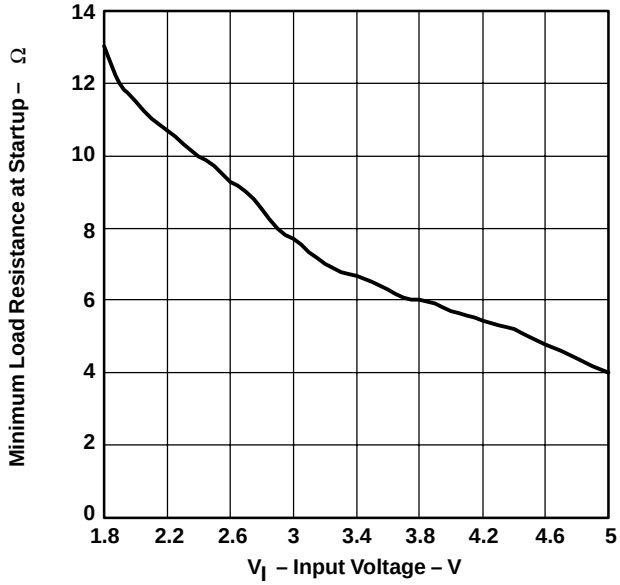


Figure 12

TPS61032
OUTPUT VOLTAGE IN CONTINUOUS MODE

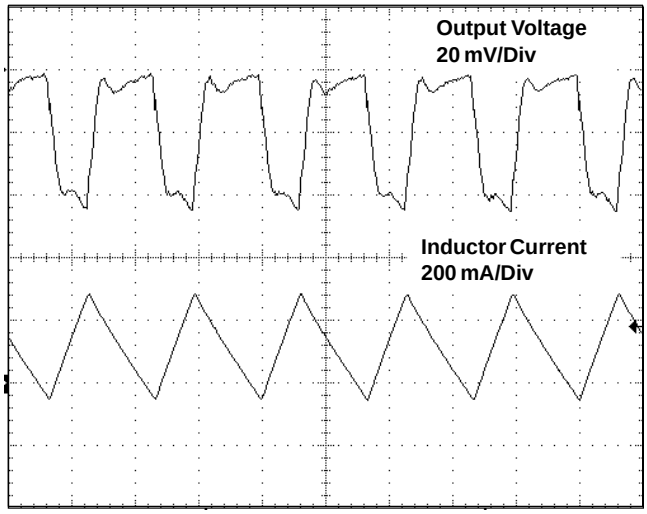


Figure 13

TPS61032
OUTPUT VOLTAGE IN POWER SAVE MODE

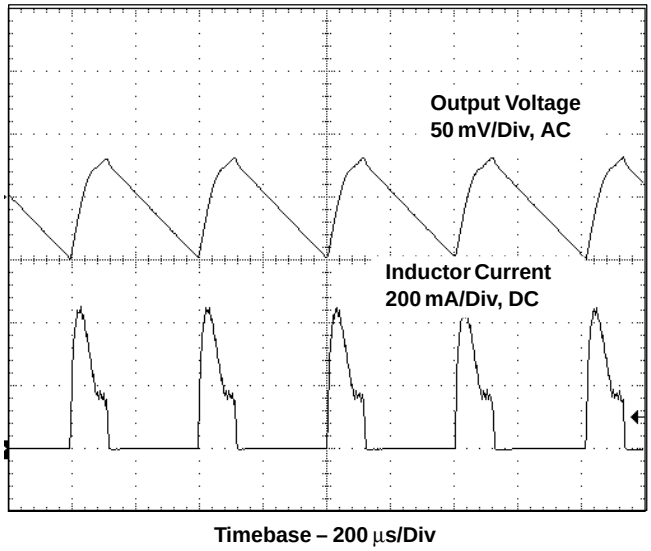


Figure 14

TPS61032
LOAD TRANSIENT RESPONSE

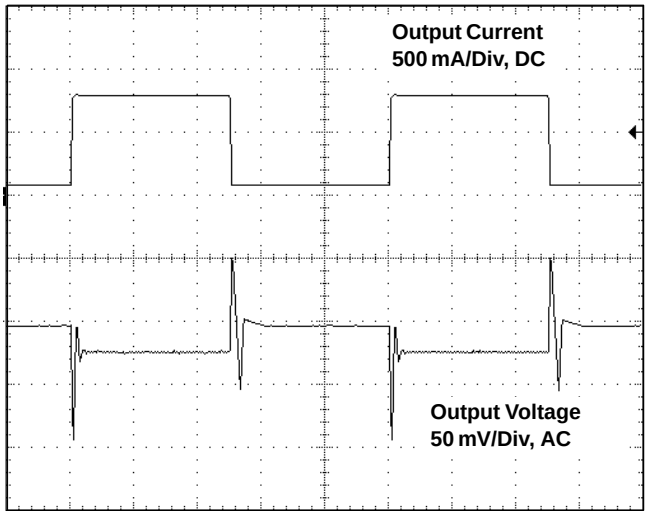


Figure 15

TPS61032
LINE TRANSIENT RESPONSE

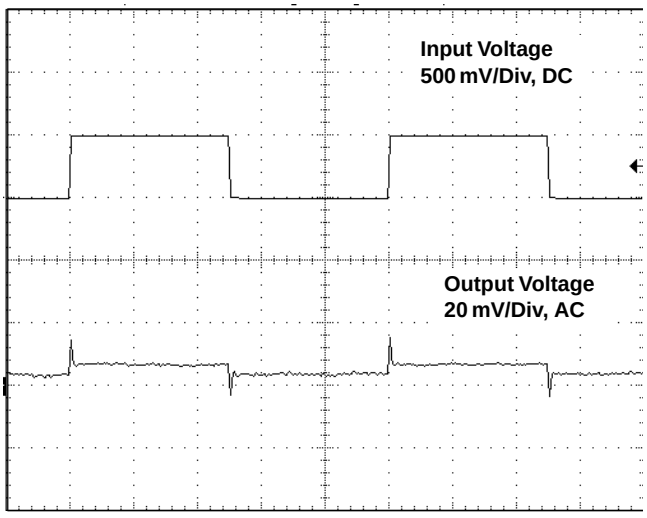


Figure 16

TPS61032
DC/DC CONVERTER START-UP AFTER ENABLE

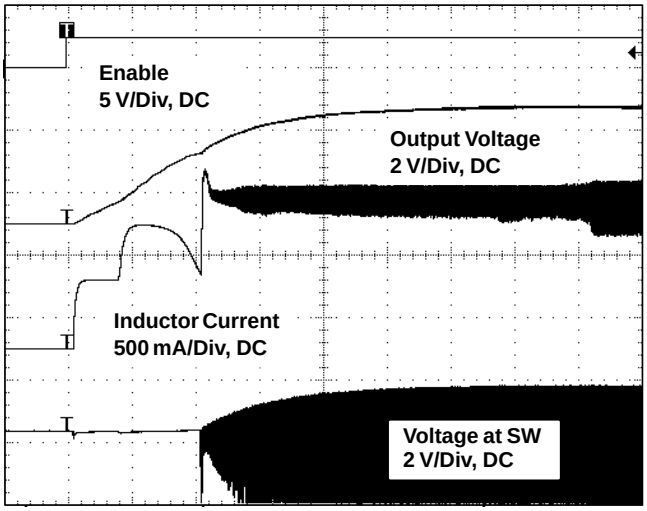


Figure 17

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6103x dc/dc converters are intended for systems powered by a dual-cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6103x is used.

Programming the Output Voltage

DC/DC Converter

The output voltage of the TPS61030 dc/dc converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μA, and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 kΩ, in order to set the divider current at 1 μA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using equation 1:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor is chosen for R3.

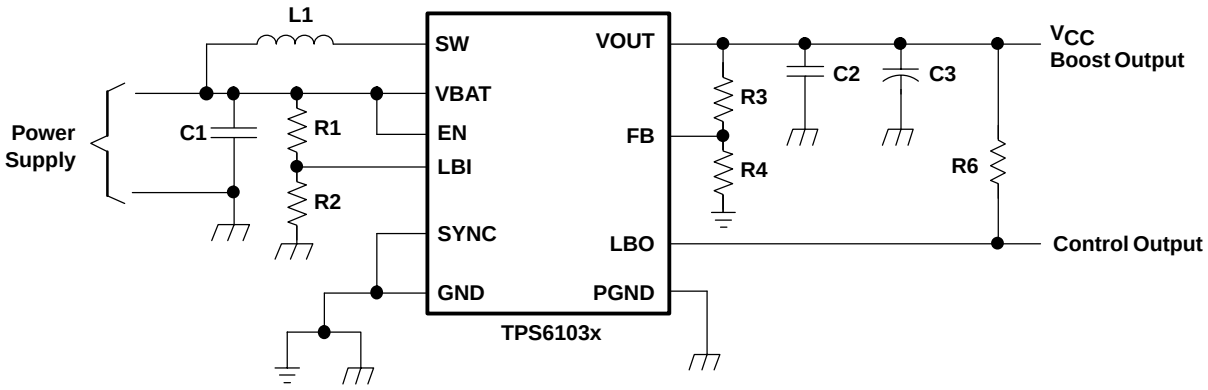


Figure 18. Typical Application Circuit for Adjustable Output Voltage Option

Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 μA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using equation 2.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1 \right) \quad (2)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs must not exceed the output voltage of the dc/dc converter. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6103x's switch is 5000 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using equation 3:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (3)$$

For example, for an output current of 1000 mA at 5 V, at least 3500 mA of average current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using equation 4:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \quad (4)$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., $10\% \times I_L$. In this example, the desired inductor has the value of 5.5 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 4. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6103x converters:

Table 1. List of Inductors

VENDOR	INDUCTOR SERIES
Sumida	CDRH124
	CDRH125
	CDRH104
Wurth Electronik	WE–PD type L
	WE–PD type XL
EPCOS	B82464G

Capacitor Selection

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

Output Capacitor DC/DC Converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using equation 5:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \quad (5)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 100 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using equation 6:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (6)$$

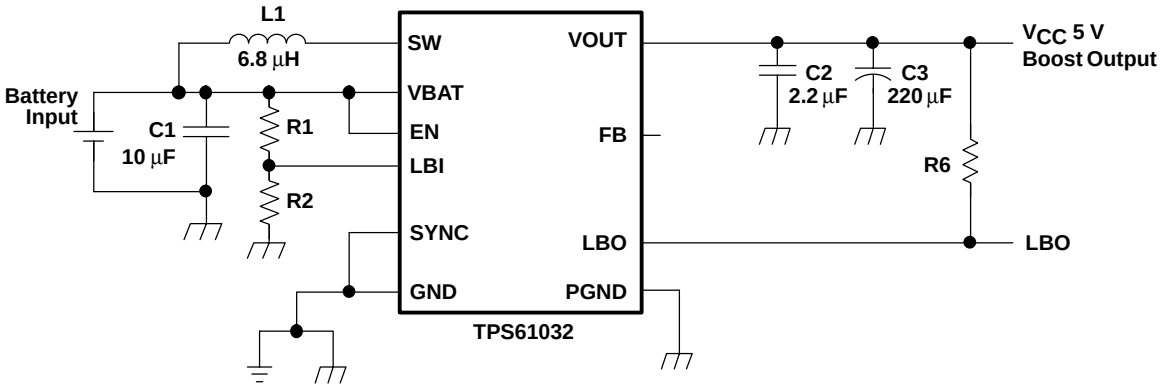
An additional ripple of 80 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 90 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, such as ceramics. So, tradeoffs have to be made between performance and costs of the converter circuit.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

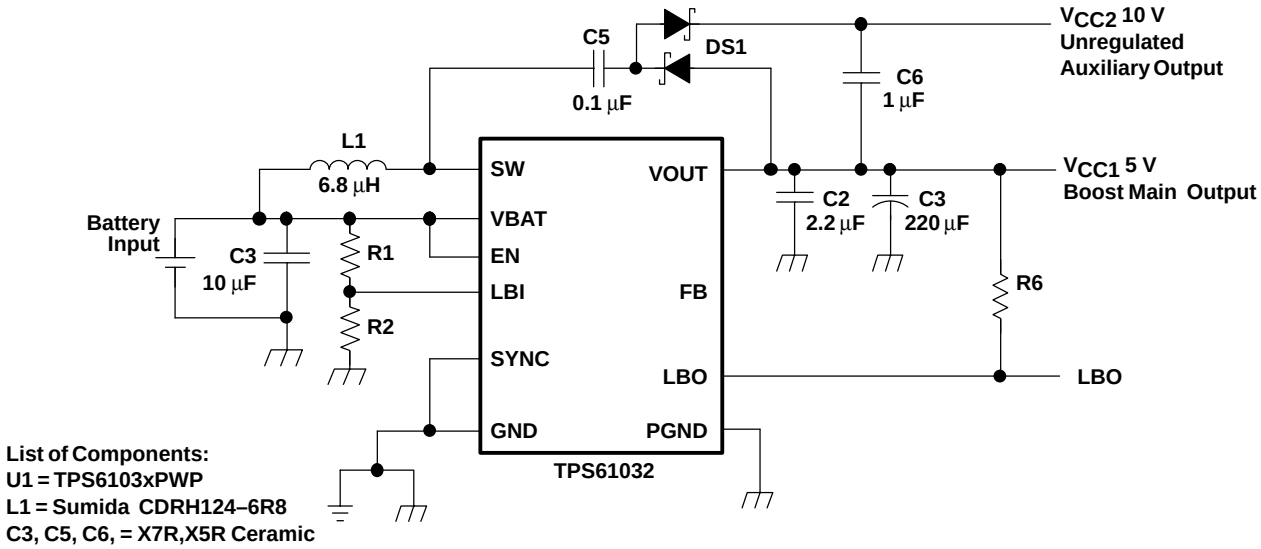
APPLICATION EXAMPLES



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2 = X7R,X5R Ceramic
C3 = Low ESR Tantalum

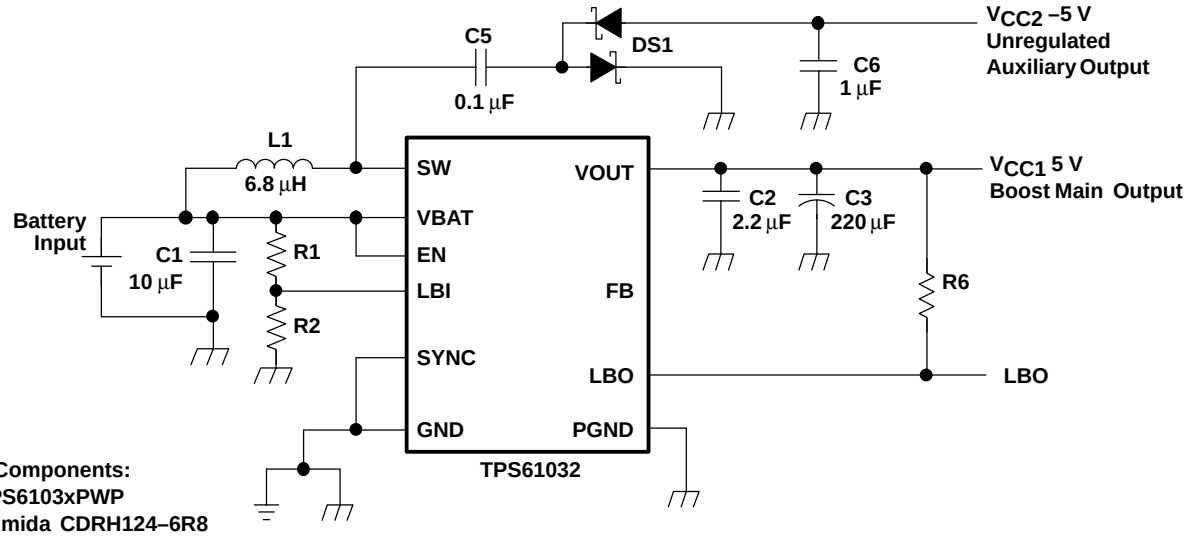
Figure 19. Power Supply Solution for Maximum Output Power

APPLICATION INFORMATION



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C3, C5, C6, = X7R,X5R Ceramic
C3 = Low ESR Tantalum
DS1 = BAT54S

Figure 20. Power Supply Solution With Auxiliary Positive Output Voltage



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2, C5, C6 = X7R,X5R Ceramic
C3 = Low ESR Tantalum
DS1 = BAT54S

Figure 21. Power Supply Solution With Auxiliary Negative Output Voltage

APPLICATION INFORMATION

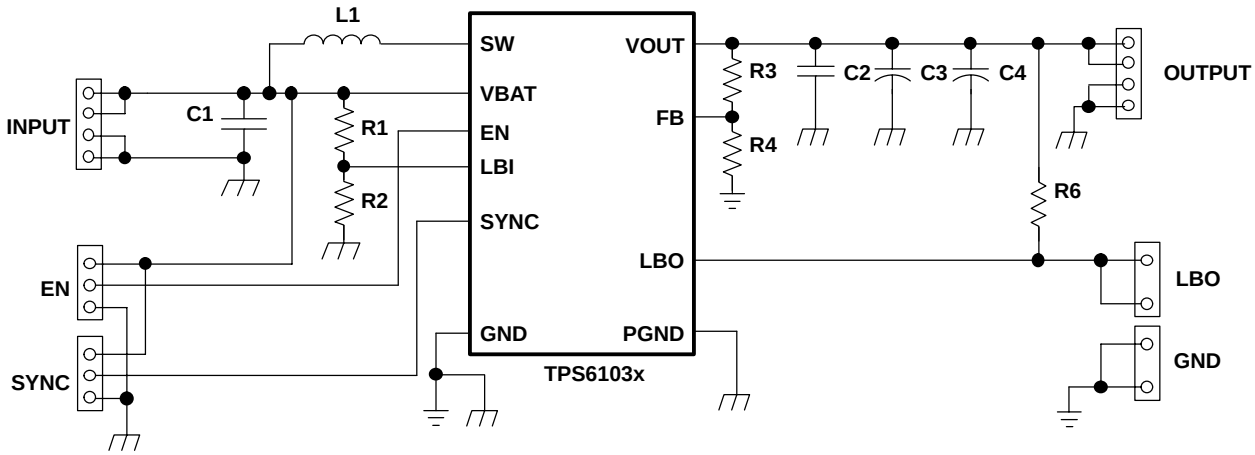


Figure 22. TPS6103x EVM-208 Circuit Diagram

DETAILED DESCRIPTION

SYNCHRONOUS RECTIFIER

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

CONTROLLER CIRCUIT

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 4000 mA.

An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

DEVICE ENABLE

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND.

In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

POWER SAVE MODE AND SYNCHRONIZATION

The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SYNC to VBAT.

Applying an external clock with a duty cycle between 30% and 70% at the SYNC pin forces the converter to operate at the applied clock frequency. The external frequency has to be in the range of about ±20% of the nominal internal frequency. Detailed values are shown in the electrical characteristic section of the data sheet.

LOW BATTERY DETECTOR CIRCUIT—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

LOW-EMI SWITCH

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

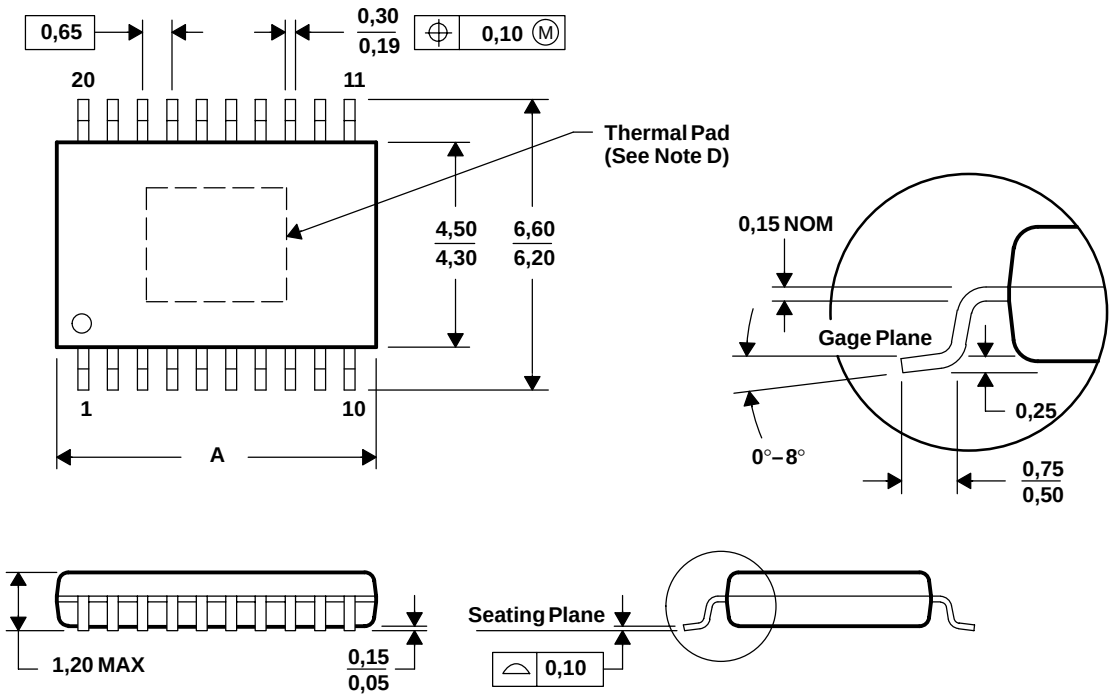
The maximum junction temperature (T_J) of the TPS6103x devices is 150°C. The thermal resistance of the 16-pin TSSOP PowerPAD package (PWP) is $R_{\theta JA}$ = 36.5 k/W, if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 1800 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150°C - 85°C}{36.5\ k/W} = 1800\ mW \quad (7)$$

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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