

DUAL-OUTPUT, SINGLE-CELL BOOST CONVERTER

FEATURES

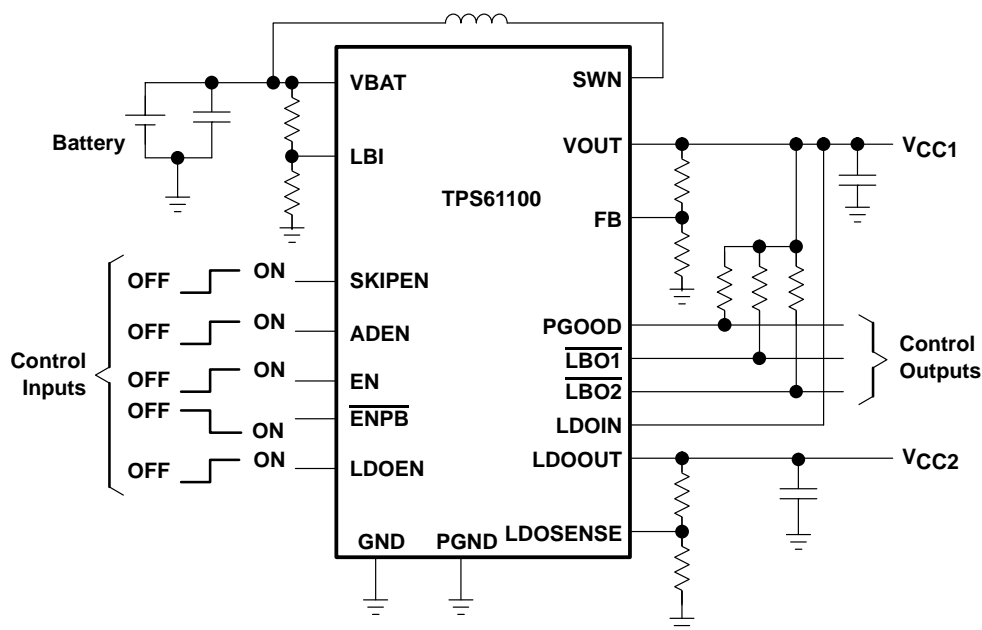
- Synchronous 95% Efficient Boost Converter
- Integrated 120 mA LDO for Second Output Voltage
- TSSOP-20 and QFN-24 Package
- 65 μ A (Typ) Total Device Quiescent Current
- 0.8 V to 3.3 V Input Voltage Range
- Adjustable Output Voltage up to 5.5 V and Fixed Output Voltage Options
- Power-Save Mode for Improved Efficiency at Low Output Power
- Battery Supervision
- Power Good Output
- Pushbutton Function for Start-Up

- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Auto Discharge Allows the Device to Discharge Output Capacitor During Shutdown
- Overtemperature Protection
- EVM Available (TPS6110XEVM-216)

APPLICATIONS

- All Single or Dual Cell Battery Operated Products Which Use Two System Voltages Like DSP C5X Applications
- Internet Audio Player, PDAs, Digital Still Cameras and Other Portable Equipment

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

DESCRIPTION

The TPS6110x devices provide a complete power supply solution for products powered by either one or two Alkaline, NiCd, or NiMH battery cells. The converter generates two stable output voltages that are either adjusted by an external resistor divider or fixed internally on the chip. It stays in operation with supply voltages down to 0.8 V. The implemented boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency.

The maximum peak current in the boost switch is limited to a value of 1800 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. An auto discharge function allows discharging the output capacitors during shutdown mode. This is especially useful in microcontroller applications where the microcontroller or microprocessor should not remain active due to the stored voltage on the output capacitors. Programming the ADEN-pin disables this feature. A low-EMI mode is implemented to reduce ringing and in effect lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. A power good output at the boost stage provides additional control of cascaded power supply components.

The built-in LDO can be used for a second output voltage derived either from the boost output or directly from the battery. The output voltage of this LDO can be programmed by an external resistor divider or is fixed internally on the chip. The LDO can be enabled separately i.e., using the power good of the boost stage.

The device is packaged in a 20-pin TSSOP (20 PW) package or in a 24-pin QFN (24 RGE) package.

AVAILABLE PACKAGE OPTIONS

PACKAGE	CODE
20-Pin TSSOP	PW
24-Pin QFN	RGE

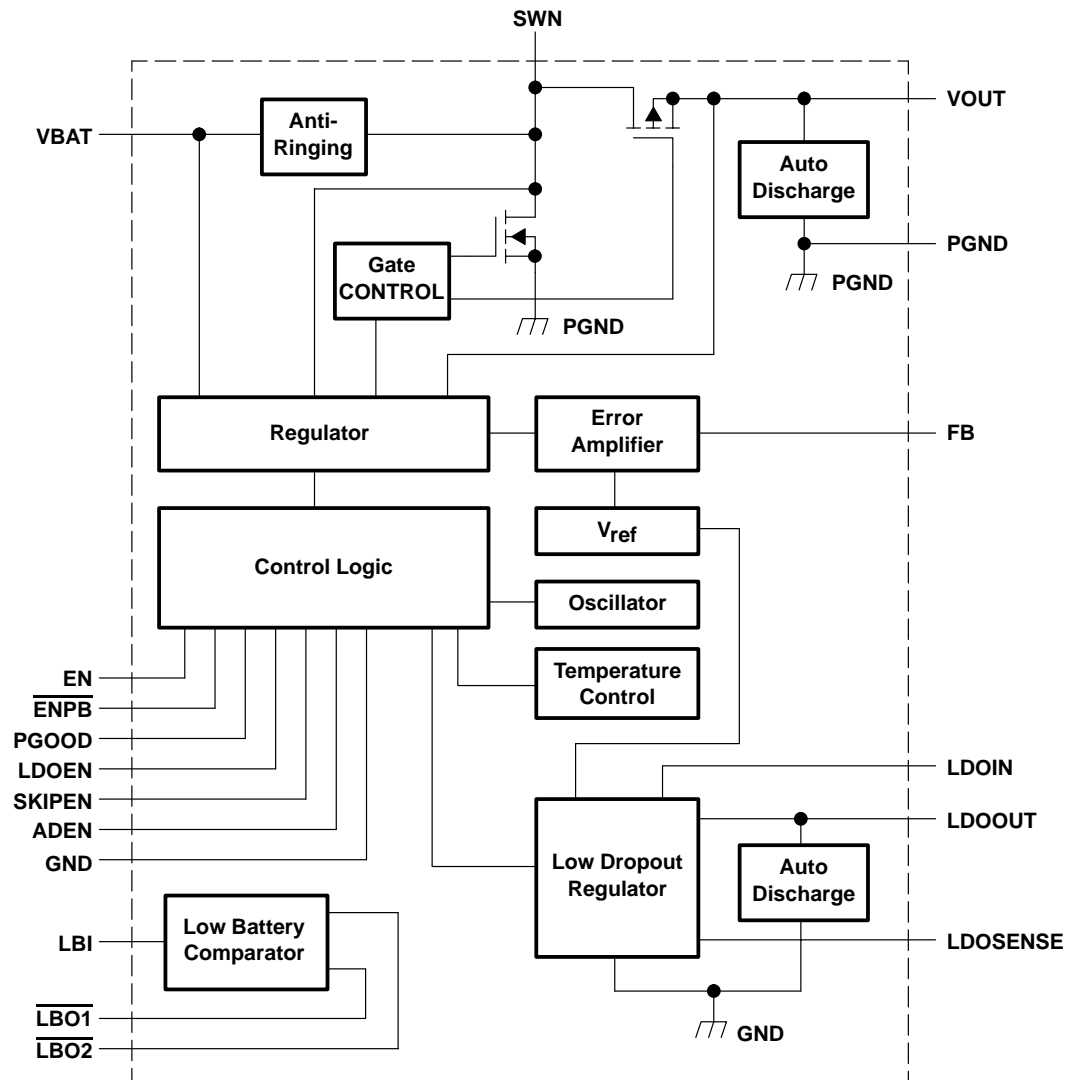
AVAILABLE OUTPUT VOLTAGE OPTIONS

T _A	OUTPUT VOLTAGE DC/DC	OUTPUT VOLTAGE LDO	PART NUMBER†	PART NUMBER†
–40°C to 85°C	Adjustable	Adjustable	TPS61100PW	TPS61100RGE
	3.3 V	Adjustable	TPS61103PW	TPS61103RGE
	3.3 V	1.5 V	TPS61106PW	TPS61106RGE
	3.3 V	1.8 V	TPS61107PW	TPS61107RGE

† The PW package is available taped and reeled. Add R suffix to device type (e.g., TPS61100PWR) to order quantities of 2000 devices per reel. The RGE package is only available in reels. Add R suffix to device type (e.g. TPS61100RGER) to order quantities of 3000 devices per reel.

‡ To check availability of the marked (‡) devices or other fixed output voltage versions contact factory.

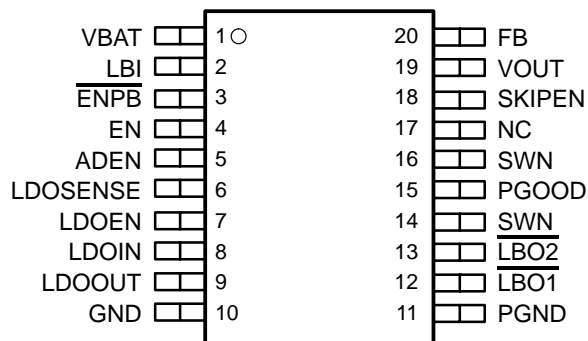
functional block diagram



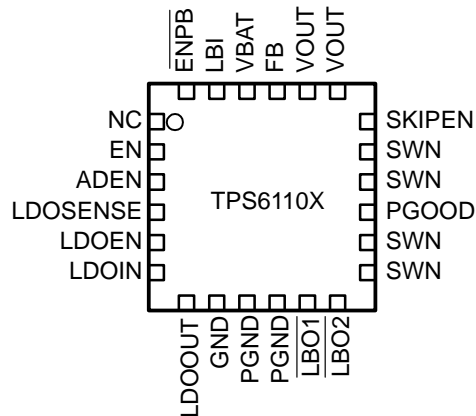
Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PW	RGE		
ADEN	5	3	I	Auto discharge enable (1/VBAT enabled, 0/GND disabled)
EN	4	2	I	Boost-enable input. (1/VBAT enabled, 0/GND disabled)
ENPB	3	24	I	Boost-enable input (pushbutton). (0/GND enabled. 1/VBAT disabled)
FB	20	21	I	Boost-voltage feedback of adjustable versions
GND	10	8	I/O	Control/logic ground
LBI	2	23	I	Low battery comparator input (comparator enabled with EN)
LBO1	12	11	O	Low battery comparator output 1 (open drain)
LBO2	13	12	O	Low battery comparator output 2 (open drain)
LDOEN	7	5	I	LDO-enable input (1/VBAT enabled, 0/GND disabled)
LDOOUT	9	7	O	LDO output
LDOIN	8	6	I	LDO input
LDOSENSE	6	4	I	LDO feedback for voltage adjustment, must be connected to LDOOUT at fixed output voltage versions
NC	17	1		No connection
PGND	11	9, 10	I/O	Power ground
PGOOD	15	15	O	Boost output power good (1 : good, 0 : failure) (open drain)
SKIPEN	18	18	I	Enable/disable Power save mode (1: VBAT enabled, 0: GND disabled)
SWN	14, 16	13, 14, 16, 17	I	Boost switch input
VBAT	1	22	I	Supply pin
VOUT	19	19, 20	O	Boost output

**PW PACKAGE
(TOP VIEW)**



**RGE PACKAGE
(TOP VIEW)**



NC – No internal connection

detailed description

synchronous rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 95%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

controller circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The nominal peak current limit is set to 1500 mA.

An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

device enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. It also can be enabled with a low signal on $\overline{\text{ENPB}}$. This forces the converter to start up as long as the low signal is applied. During this time EN must be set high to prevent the converter from going down into shutdown mode again. If EN is high, a negative signal on $\overline{\text{ENPB}}$ is ignored.

In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the synchronous rectifier section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 0.7 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 0.7 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

LDO enable

When the voltage is applied at VBAT, the LDO can be separately enabled and disabled by using the LDOEN pin in the same way as the EN pin at the dc/dc converter stage described above.

detailed description (continued)

power good

The PGOOD pin stays high impedance when the dc/dc converter delivers an output voltage within a defined voltage window. So it can be used to enable the converter after pushbutton start-up, or to enable any connected circuitry such as cascaded converters (LDO) or processor circuits.

power save mode

The SKIPEN pin can be used to select different operation modes. To enable power save, SKIPEN must be set high. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SKIPEN to GND.

auto discharge

The auto discharge function is needed in applications where the supply voltage of a microcontroller, microprocessor or memory has to be removed during shutdown in order to make sure that the system quickly goes in a defined state. The auto discharge function is enabled when the ADEN is set high. It is disabled when the ADEN is set to GND. When the auto discharge function is enabled, the output capacitor is discharged after the device is programmed in the shutdown mode. The output capacitor is discharged by an integrated switch of 400 Ω , hence the discharge time depends on the size of the output capacitor.

low battery detector circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, both LBO-pin are high-impedance. There are three programmed thresholds, 400 mV, 450 mV, and 500 mV. The outputs on $\overline{\text{LBO1}}$ and $\overline{\text{LBO2}}$ are shown as follows:

LBI INPUT (mV)	$\overline{\text{LBO1}}$	$\overline{\text{LBO2}}$
0–400	0	0
400–450	1	0
450–500	0	1
500–VBAT	1	1

1 means that the output stays at high-impedance and 0 means that the output goes active low. If there is only one LBO output needed, both outputs can be tied together. Then the switching threshold is at 500 mV at LBI.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI-pin. The resistive divider scales down the battery voltage to a voltage level of 400 mV (450 mV, 500 mV), which is then compared to the LBI threshold voltage. The LBI-pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI-threshold. If the low-battery detection circuit is not used, the LBI-pin should be connected to GND (or to VBAT) and the LBO-pin can be left unconnected. Do not let the LBI-pin float.

low-EMI switch

The device integrates a circuit that removes the ringing that typically appears on the SW-node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW-pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

detailed description (continued)

LDO

The built-in LDO can be used to generate a second output voltage derived from the dc/dc converter output, from the battery, or from another power source like an ac adapter or a USB power rail. The LDOSENSE input must be connected to LDOOUT at fixed output voltage versions.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Input voltage range on VBAT, LBI, SKIPEN, EN, $\overline{\text{ENPB}}$, ADEN, FB, LDOEN –0.3 V to 3.6 V
 Input voltage range on SWN, VOUT, LDOIN, LDOOUT, LDOSENSE, PGOOD, $\overline{\text{LBO1}}$, $\overline{\text{LBO2}}$ –0.3 V to 7 V
 Operating free air temperature range T_A –40°C to 85°C
 Maximum junction temperature T_J 150°C
 Storage temperature range T_{stg} –65°C to 150°C
 Lead temperature 1,6 mm (1/16 inch) from case for 10s 260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT, V_I	0.8		3.3	V
Boost—inductor, L	4.7	10		μH
Boost—input capacitor, C_i		10		μF
Boost—output capacitor, C_O	22	100		μF
LDO—input capacitor, C_i		1		μF
LDO—output capacitor, C_O	1	2.2		μF
Operating virtual junction temperature, T_J	–40		125	°C

electrical characteristics over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

boost stage

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(b)}$	Input voltage for start-up	$R_L > = 66 \Omega$ at $V_O = 3.3 \text{ V}$		0.85	1.1	V
	Input voltage once started		0.8		3.3	V
$V_{O(b)}$	Output voltage		1.5		5.5	V
Minimum possible output power		PW package, $V_{BAT} \geq 1.5 \text{ V}$		600		mW
V_{ref}	Reference voltage		485	500	515	mV
f	Oscillator frequency		320	500	800	kHz
Switch current limit		$V_O = 3.3 \text{ V}$	1200	1500	1800	mA
Startup current limit				610		mA
Boost switch on resistance		$V_O = 3.3 \text{ V}$		180	300	m Ω
Sync switch on resistance		$V_O = 3.3 \text{ V}$		180	300	m Ω
Total accuracy					3%	
Auto discharge switch resistance				400		Ω
Boost quiescent current	V _{BAT}	$I_O = 0 \text{ mA}$, $V_{EN} = V_{BAT} = 3.3 \text{ V}$, $V_O = 3.3 \text{ V}$, ENLDO = 0		25	40	μA
	V _{OUT}	$I_O = 0 \text{ mA}$, $V_{EN} = V_{BAT} = 3.3 \text{ V}$, $V_O = 3.3 \text{ V}$, ENLDO = 0		12	20	μA
Boost shutdown current		$V_{EN} = 0 \text{ V}$		0.5	5	μA

LDO stage

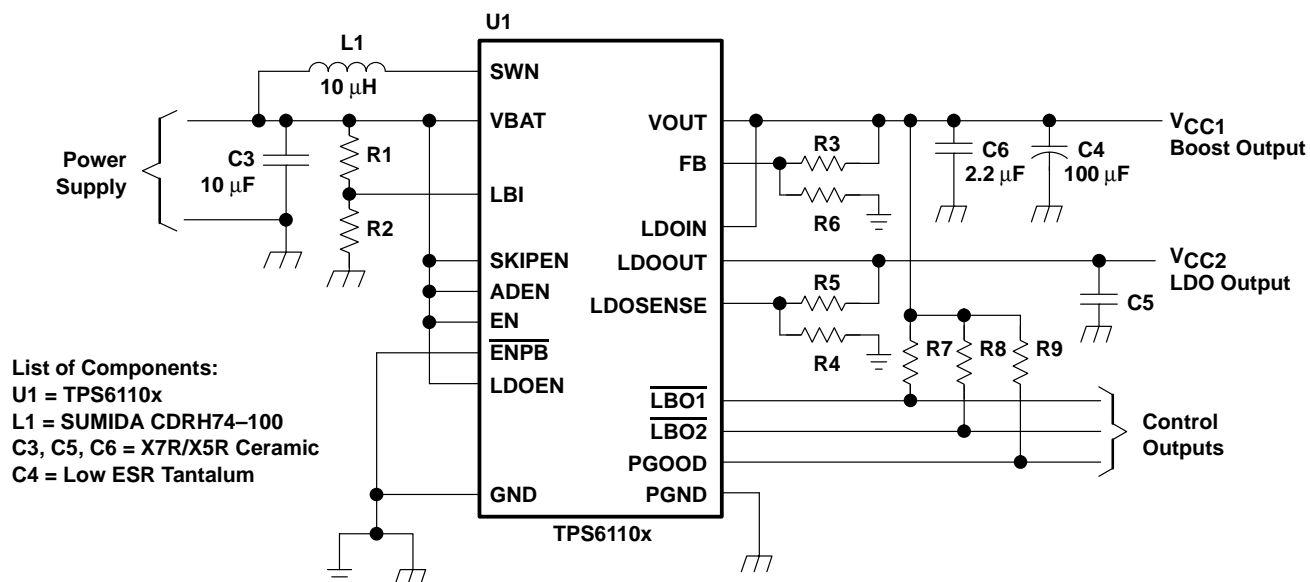
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _I (LDO)	Input voltage range		1.5		7	V
V _O (LDO)	Output voltage		0.9		3.6	V
I _O (LDO)	Output current	V _I ≥ 1.8 V	120	270		mA
		V _I <1.8 V	80			
LDO short circuit current limit					500	mA
Minimum voltage drop		V _I ≥ 1.8 V, I _O (LDO) = 120 mA			300	mV
Total accuracy		I _O ≥ 1 mA			±3%	
Line regulation		LDOIN change form 1.8 V to 2.6 V at 100 mA			0.6%	
Load regulation		Load change from 10% to 90%			0.6%	
Auto discharge switch resistance				400		Ω
LDO quiescent current	LDOIN	LDOIN = 7 V, VBAT = 1.2 V, EN = 0		27	40	μA
	VBAT			27	40	
LDO shutdown current				0.01	1	μA

electrical characteristics over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted) (continued)

control stage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL} LBI1 voltage threshold	V_{LBI} voltage decreasing	390	400	410	mV
LBI2 voltage threshold	V_{LBI} voltage decreasing	440	450	460	mV
LBI3 voltage threshold	V_{LBI} voltage decreasing	490	500	510	mV
LBI input hysteresis			10		mV
LBI input current	EN = Vbat or GND		0.01	0.1	μ A
$\overline{LBO1}$ output low voltage	$V_O = 3.3$ V $I_{OL} = 10$ μ A		0.04	0.4	V
$\overline{LBO1}$ output low current			10		μ A
$\overline{LBO1}$ output leakage current	$V_{LBO} = 3.3$ V		0.01	0.1	μ A
$\overline{LBO2}$ output low voltage	$V_O = 3.3$ V $I_{OL} = 10$ μ A		0.04	0.4	V
$\overline{LBO2}$ output low current			10		μ A
$\overline{LBO2}$ output leakage current	$V_{LBO} = 3.3$ V		0.01	0.1	μ A
V_{IL} EN, \overline{ENPB} , LDOEN, SKIPEN and ADEN input low voltage			$0.2 \times V_{BAT}$		
V_{IH} EN, \overline{ENPB} , LDOEN, SKIPEN and ADEN input high voltage		$0.8 \times V_{BAT}$			
EN, \overline{ENPB} , LDOEN, SKIPEN and ADEN input current	Clamped on GND or VBAT		0.01	0.1	μ A
Powergood threshold	$V_O = 3.3$ V	$0.9 \times V_O$	$0.92 \times V_O$	$0.95 \times V_O$	
Powergood delay			30		μ s
Powergood output low voltage	$V_O = 3.3$ V $I_{OL} = 10$ μ A		0.04	0.4	V
Powergood output low current			10		μ A
Powergood output leakage current			0.01	0.1	μ A
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table of Graphs

BOOST CONVERTER		FIGURE
Maximum output current	vs Input voltage for VOUT = 3.3 V, 5.0 V	1
	vs Input voltage for VOUT = 1.8 V, 2.5 V	2
Efficiency	vs Output current for VIN = 1.2 V, VOUT = 1.5 V	3
	vs Output current for VIN = 1.2 V, VOUT = 2.5 V	4
	vs Output current for VIN = 1.2 V, VOUT = 3.3 V	5
	vs Output current for VIN = 1.8 V, VOUT = 2.5 V	6
	vs Output current for VIN = 2.4 V, VOUT = 3.3 V	7
	vs Output current for VIN = 2.4 V, VOUT = 5.0 V	8
	vs Input voltage for Iout = 10 mA/100 mA/200 mA, VOUT = 3.3 V	9
Output voltage	vs Output current TPS61103/6	10
Minimum start-up supply voltage	vs Load resistance	11
No-load supply current into VBAT	vs Input voltage	12
No-load supply current into VOUT	vs Input voltage	13
Waveforms	Output voltage (ripple) in continuous mode Inductor current	14
	Output voltage (ripple) in power save mode Inductor current	15
	Load transient response for output current step of 40 mA to 120 mA	16
	Line transient response for supply voltage step from 1 V to 1.5 V at Iout = 100 mA	17
	Boost converter start-up after enable	18
LDO		
Maximum output current	vs Input voltage for VOUT = 2.5 V, 3.3 V	19
	vs Input voltage for VOUT = 1.5 V, 1.8 V	20
Output voltage	vs Output current TPS61106	21
Dropout voltage	vs Output current TPS61100 at 3.3 V TPS61106	22
No-load supply current into LDOIN	vs Input voltage	23
PSRR	vs Frequency	24
Waveforms	Load transient response for output current step of 20 mA to 100 mA	25
	Line transient response for supply voltage step from 1.8 V to 2.4 V at Iout = 100 mA	26
	LDO start-up after enable	27

TYPICAL CHARACTERISTICS

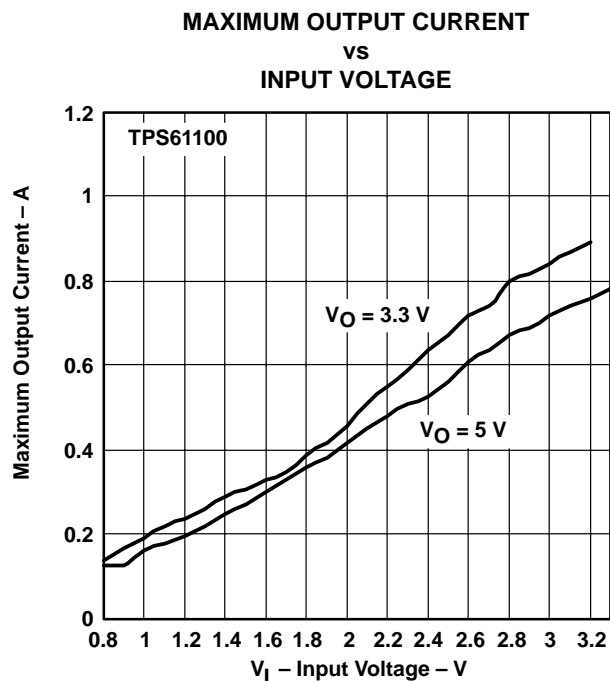


Figure 1

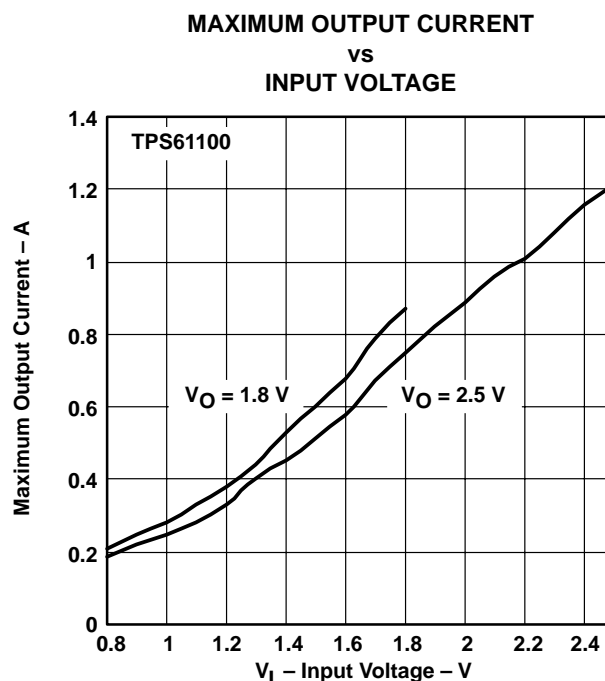


Figure 2

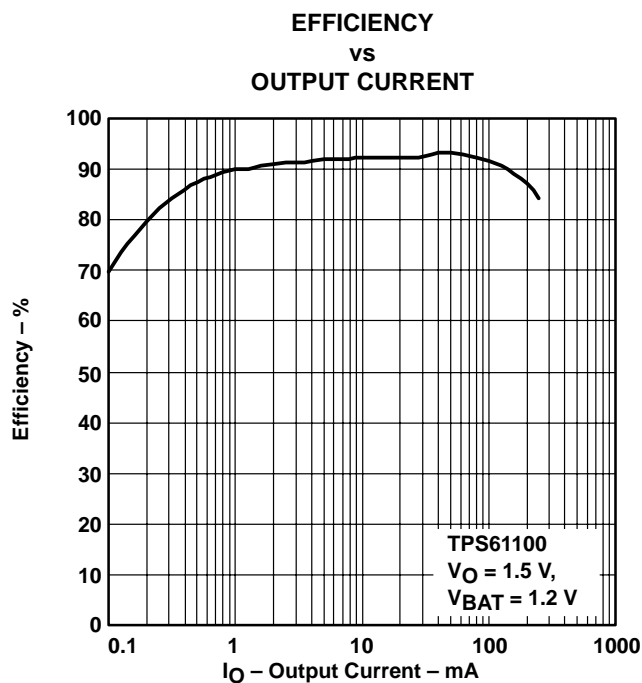


Figure 3

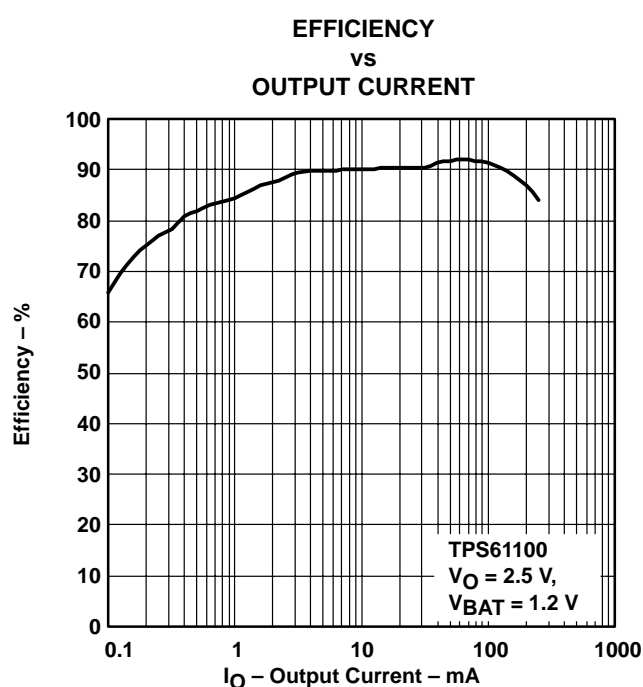


Figure 4

TYPICAL CHARACTERISTICS

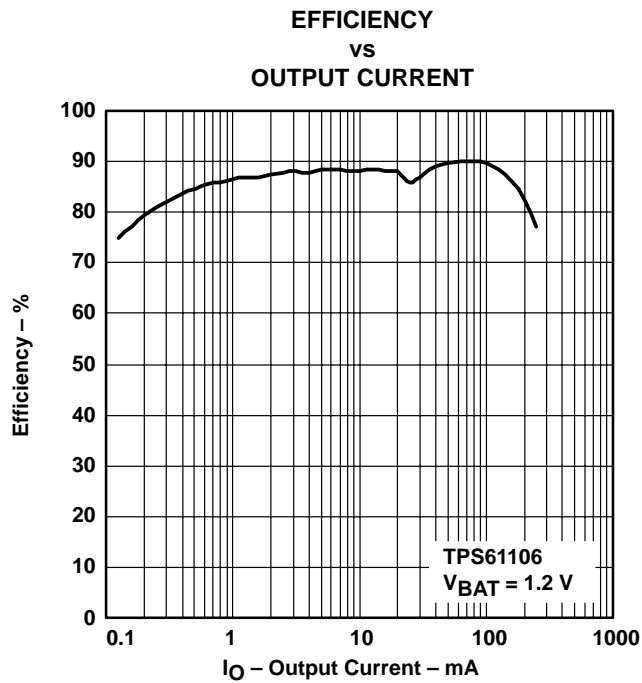


Figure 5

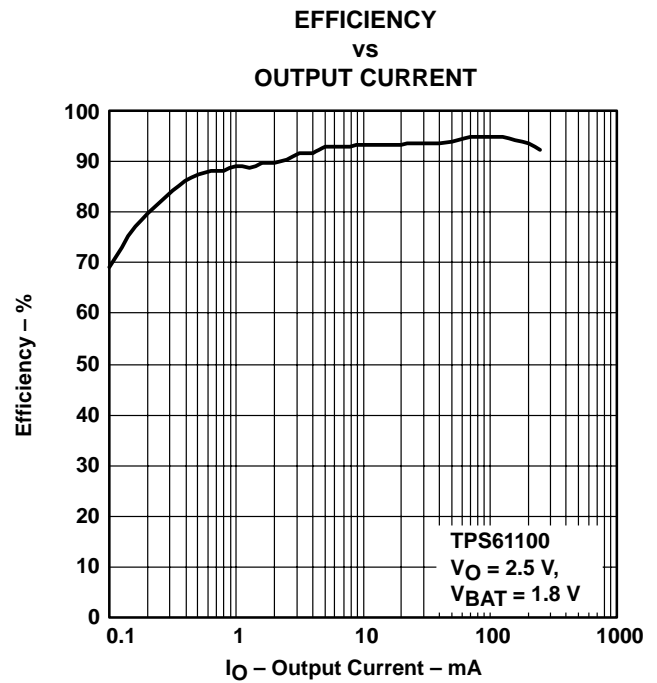


Figure 6

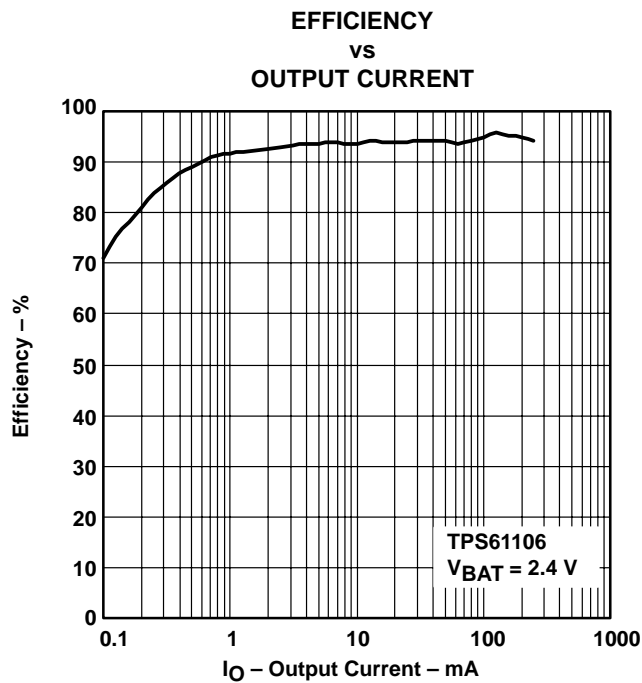


Figure 7

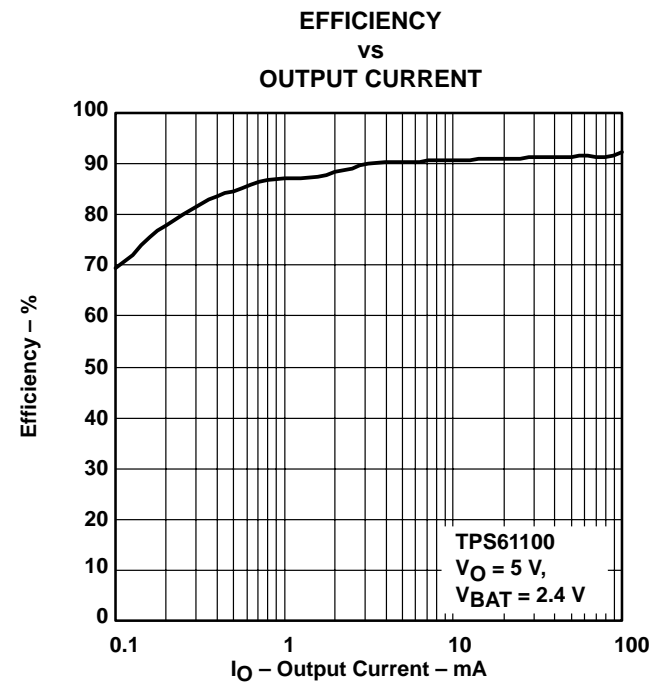


Figure 8

TYPICAL CHARACTERISTICS

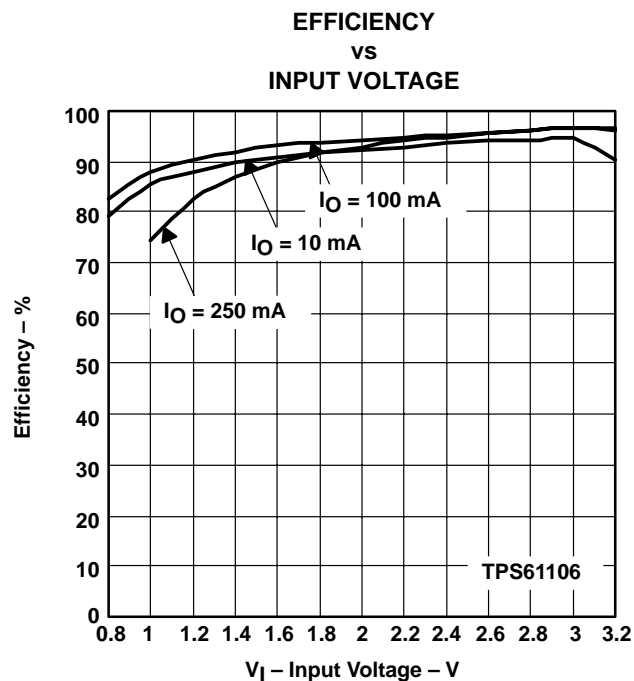


Figure 9

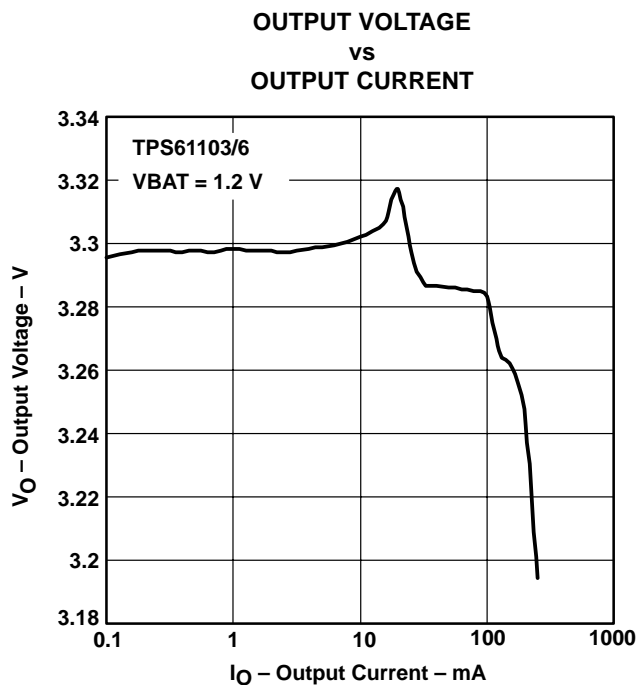


Figure 10

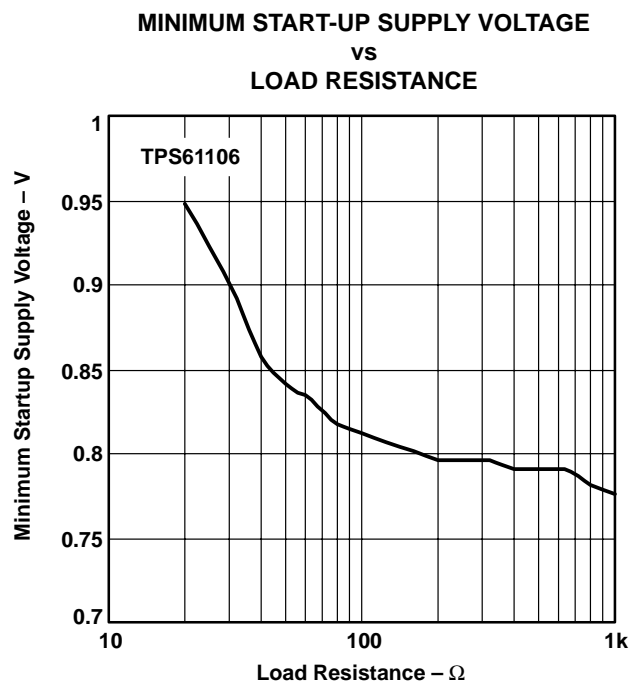


Figure 11

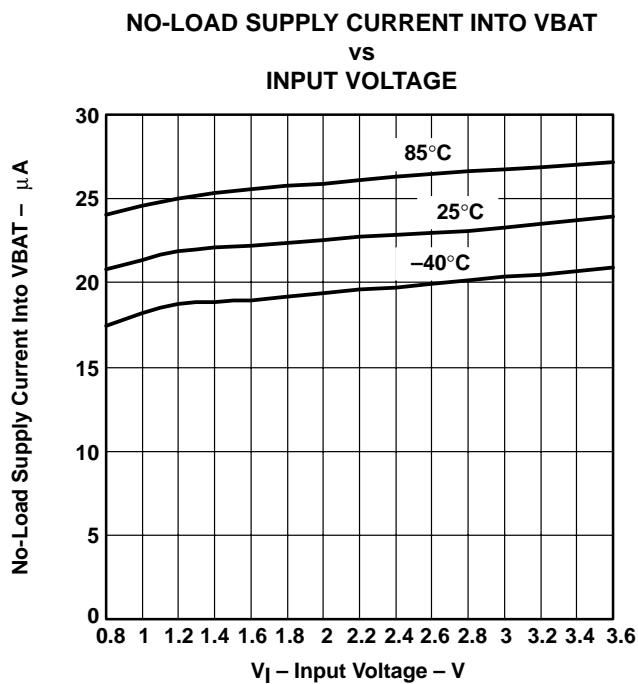


Figure 12

TYPICAL CHARACTERISTICS

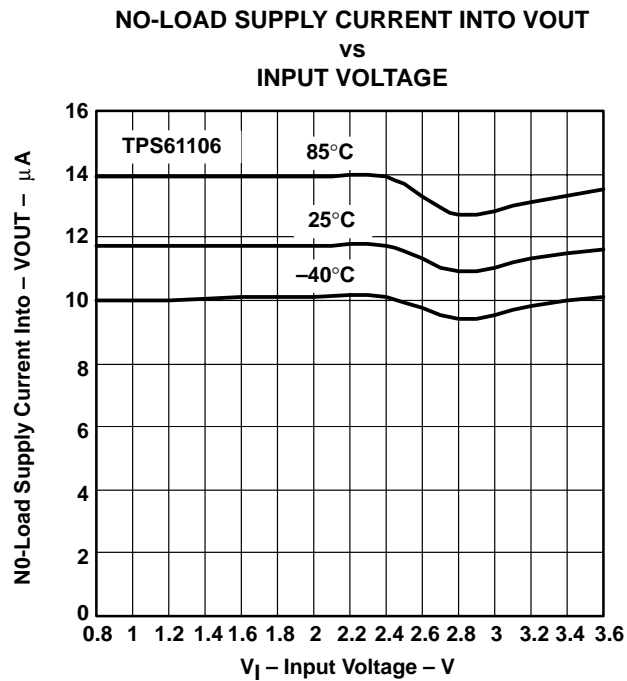


Figure 13

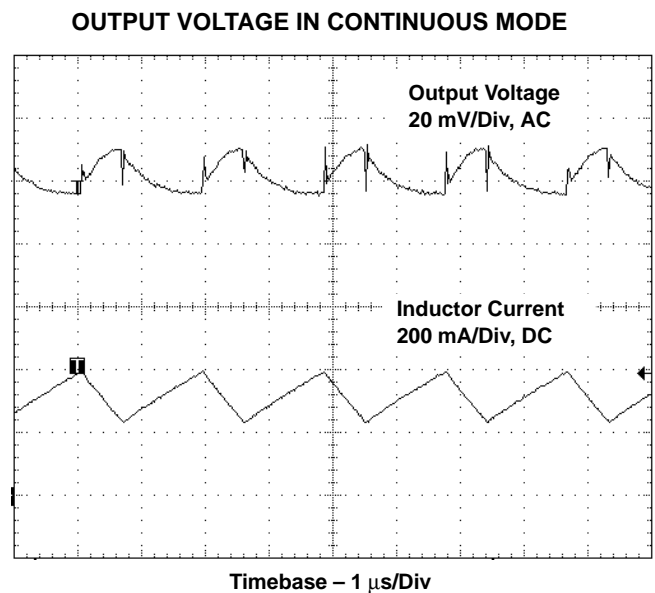


Figure 14

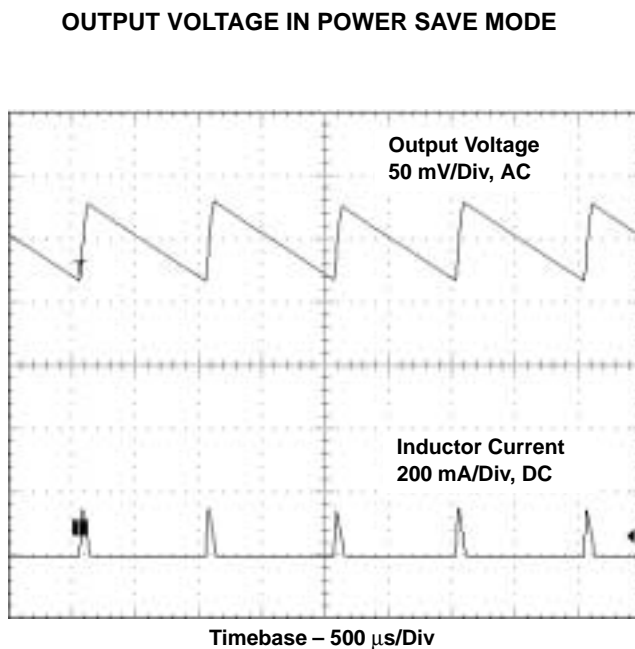


Figure 15

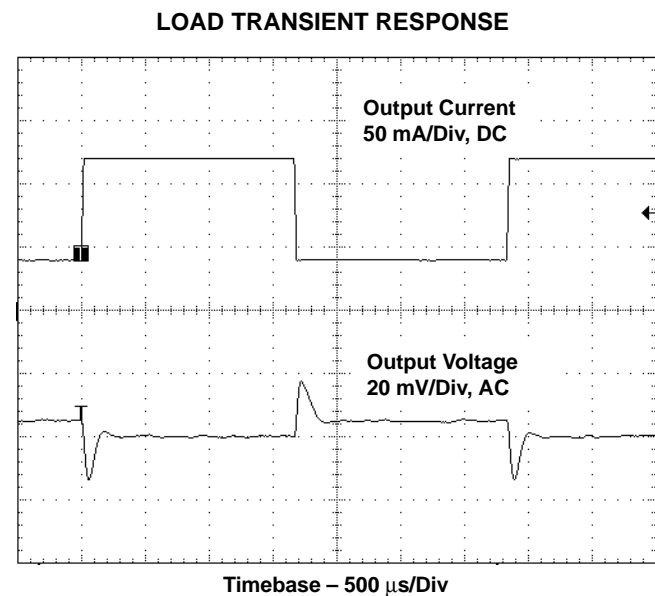


Figure 16

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

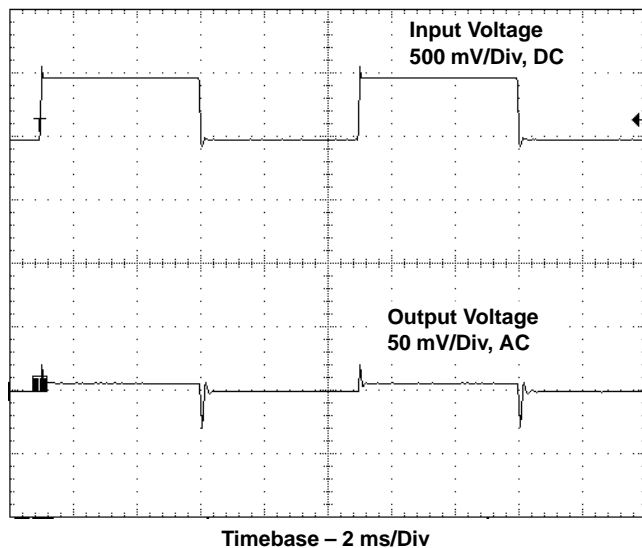


Figure 17

BOOST CONVERTER START-UP AFTER ENABLE

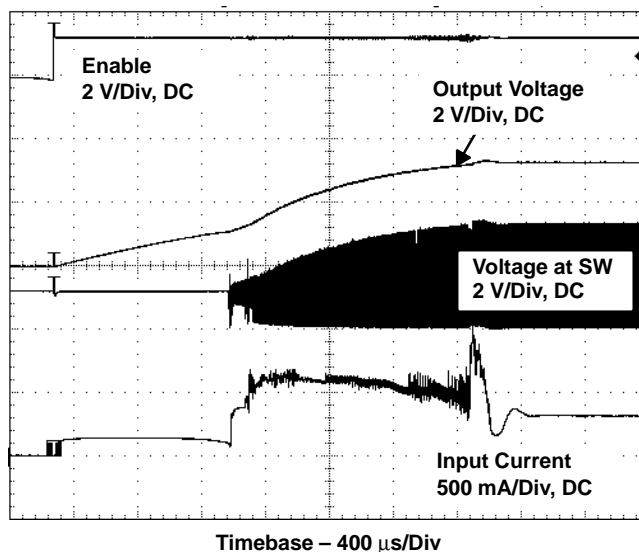


Figure 18

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

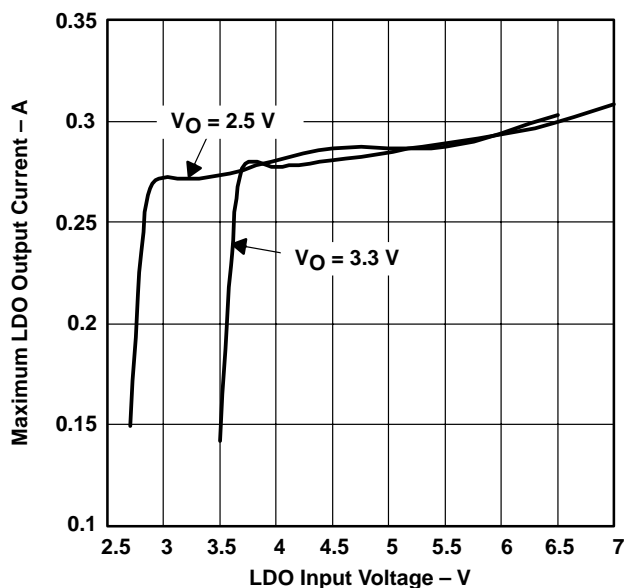


Figure 19

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

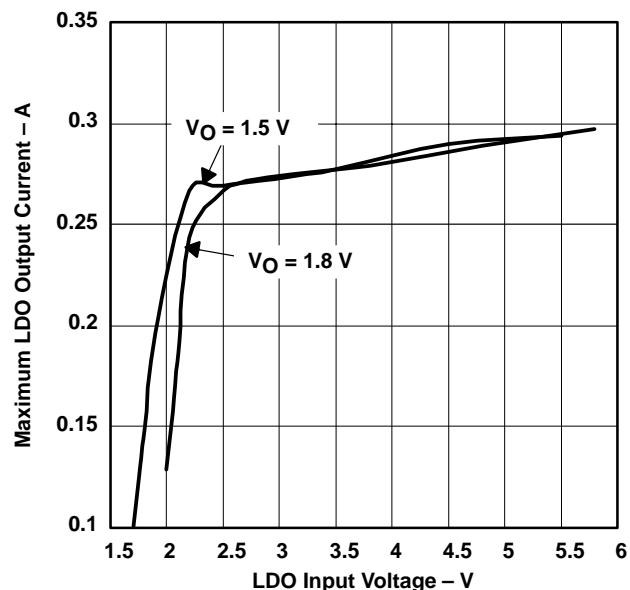


Figure 20

TYPICAL CHARACTERISTICS

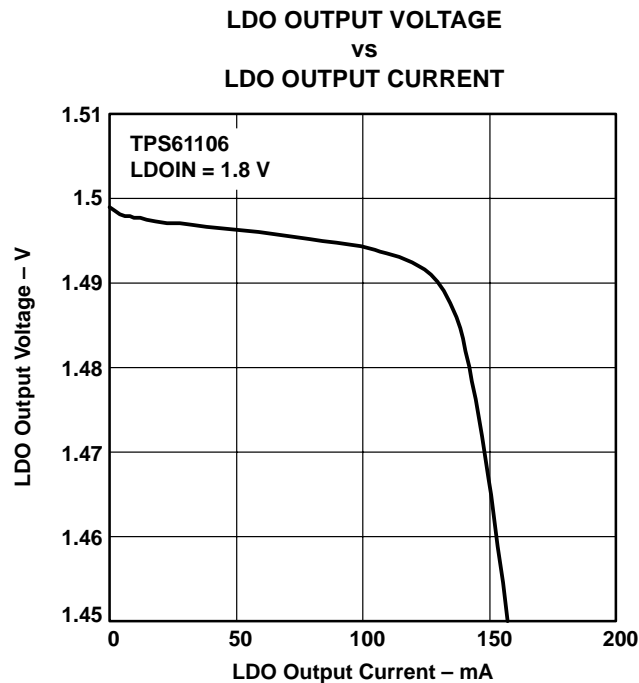


Figure 21

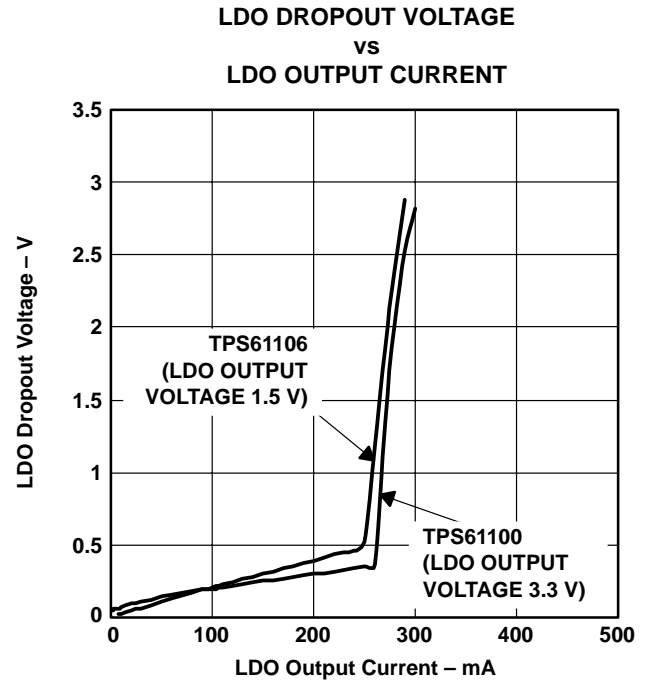


Figure 22

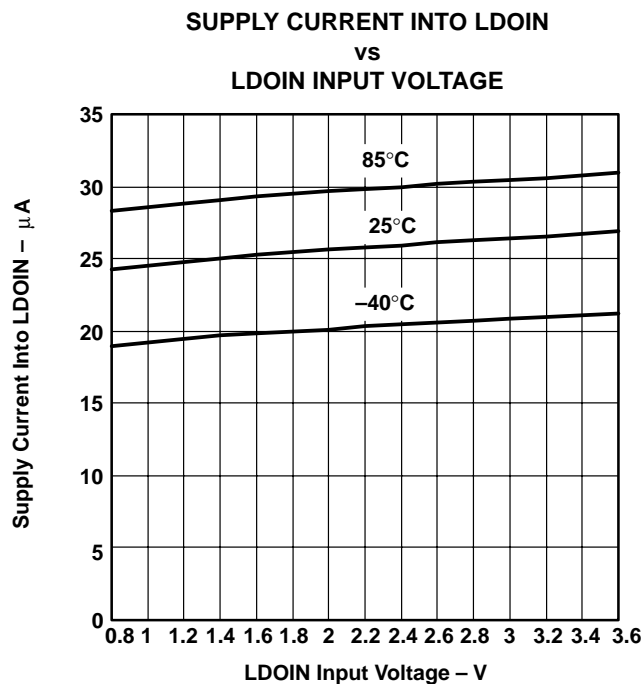


Figure 23

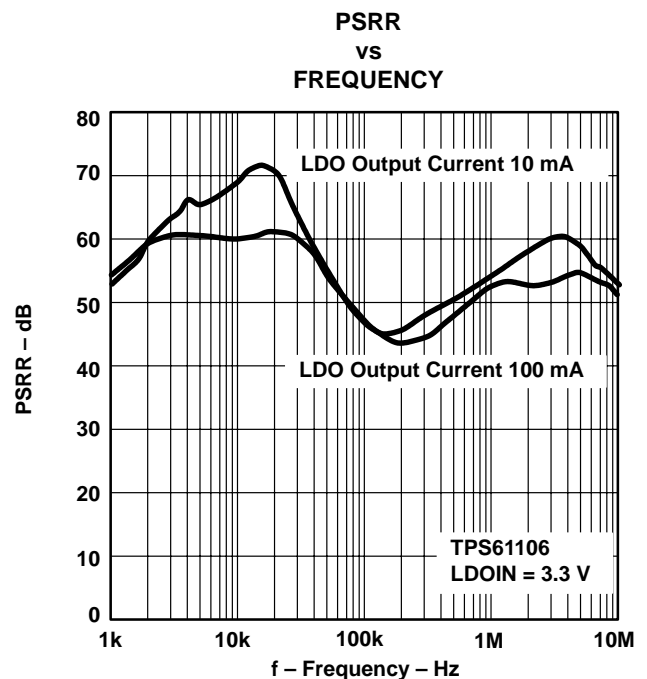


Figure 24

TYPICAL CHARACTERISTICS

LDO LOAD TRANSIENT RESPONSE

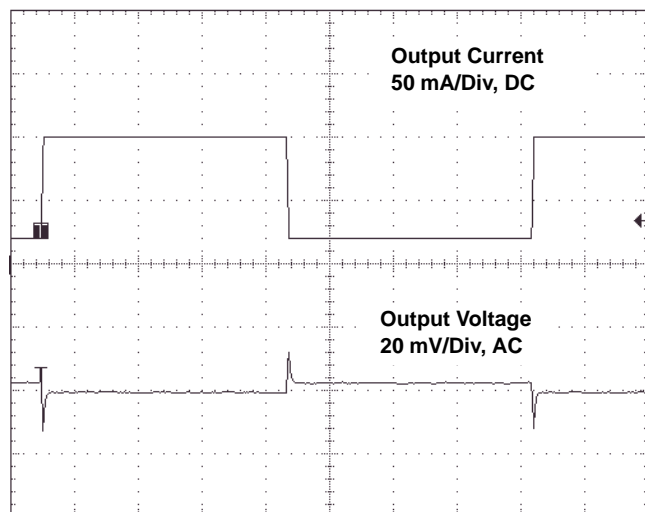


Figure 25

LDO LINE TRANSIENT RESPONSE

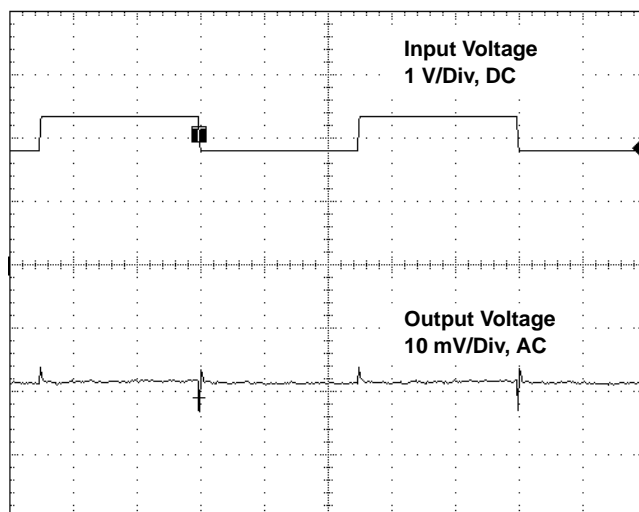


Figure 26

LDO START-UP AFTER ENABLE

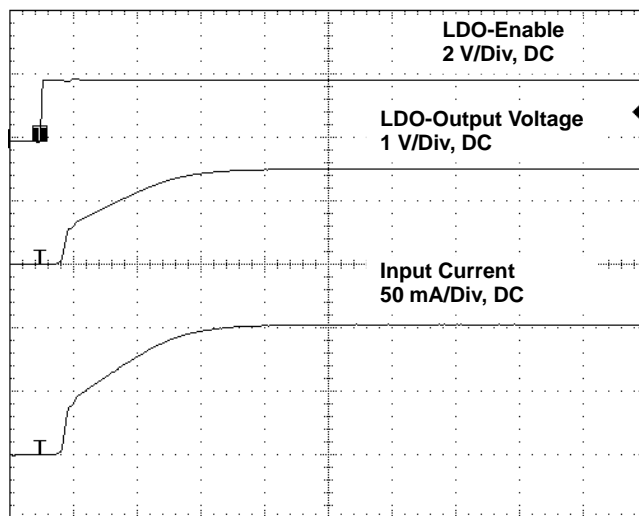


Figure 27

APPLICATION INFORMATION

design procedure

The TPS6110x boost converters are intended for systems powered by a single-cell NiCd or NiMH battery with a typical terminal voltage between 0.9 V and 1.6 V. They can also be used in systems powered by two-cell NiCd or NiMH batteries with a typical stack voltage between 1.8 V and 3.2 V. Additionally, single- or dual-cell, primary and secondary alkaline battery cells can be the power source in systems where the TPS6110x is used.

programming the output voltage

boost converter

The output voltage of the TPS61100 boost converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μ A and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R6 should be lower than 500 k Ω , in order to set the divider current at 1 μ A or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 k Ω . From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using equation 1:

$$R3 = R6 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180 \text{ k}\Omega \times \left(\frac{V_O}{500 \text{ mV}} - 1 \right) \quad (1)$$

boost converter (continued)

Figure 28. Typical Application Circuit for Adjustable Output Voltage Option

Programming the output voltage at the LDO follows almost the same rules as at the boost converter section. The maximum programmable output voltage at the LDO is 3.3 V. Since reference and internal feedback circuitry are similar, as they are at the boost converter section, R4 also should be in the 200-k Ω range. The calculation of the value of R5 can be done using the following equation (2):

If as an example, an output voltage of 1.5 V is needed, a 360 k Ω -resistor should be chosen for R5.

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 μA , and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 400 mV, 450 mV or 500 mV. The recommended value for R2 is therefore in the range of 500 k Ω . From that, the value of resistor R₁, depending on the desired minimum battery voltage V_{BAT} can be calculated using equation 3.

20

APPLICATION INFORMATION

programming the LBI/LBO threshold voltage (continued)

For example, if the low-battery detection circuit should flag an error condition for the 450 mV threshold on the LBO outputs at a battery voltage of 1.23 V, a 680-k Ω resistor should be chosen for R1. The resulting battery voltages of the other thresholds can be calculated using equation 4:

$$V_{BAT} = V_{LBI-threshold} \times \left(\frac{R1}{R2} + 1 \right) = 500 \text{ mV} \times \left(\frac{680 \text{ k}\Omega}{390 \text{ k}\Omega} + 1 \right) \quad (4)$$

The result for the 500-mV threshold in our example is 1.37 V and for the 400-mV threshold 1.1 V. This results in the following truth table for the battery supervisor outputs:

VBAT [V]	$\overline{LBO1}$	$\overline{LBO2}$
0–1.1	0	0
1.1–1.23	1	0
1.23–1.37	0	1
1.37–VBAT max	1	1

If the application requires only a simple LBI/LBO function both LBO outputs can be connected together. The LBI threshold then is 500 mV.

The outputs of the low battery supervisor are simple open-drain outputs that go active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 M Ω . The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the boost converter. If not used, the LBO pin can be left floating or tied to GND.

inductor selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6110x's switch is 1200 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using equation 5:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (5)$$

For example, for an output current of 100 mA at 3.3 V, at least 515 mA of current flows through the inductor at a minimum input voltage of 0.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using equation 6:

$$L = \frac{V_{BAT} \times (V_{OUT} - V_{BAT})}{\Delta I_L \times f \times V_{OUT}} \quad (6)$$

APPLICATION INFORMATION

inductor selection (continued)

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., $20\% \times I_L$. In this example, the desired inductor has the value of $12 \mu\text{H}$. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 5. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 1. Inductors

VENDOR	RECOMMENDED INDUCTOR SERIES
Sumida	CDRH73
	CDRH74
	CDRH5D18
	CDRH6D38
Coiltronics	DR73
	DR74
Murata	LQS66C
	LQN6C
TDK	SLF 7045
	SLF 7032
Würth Electronic	WE-PD Type M
	WE-PD Type S

capacitor selection

input capacitor

At least a $10\text{-}\mu\text{F}$ input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

output capacitor boost converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using equation 7:

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{BAT}})}{f \times \Delta V \times V_{\text{OUT}}} \quad (7)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV , a minimum capacitance of $10 \mu\text{F}$ is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using equation 8:

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}} \quad (8)$$

Figure 29. Solution for Maximum Output Power

APPLICATION INFORMATION

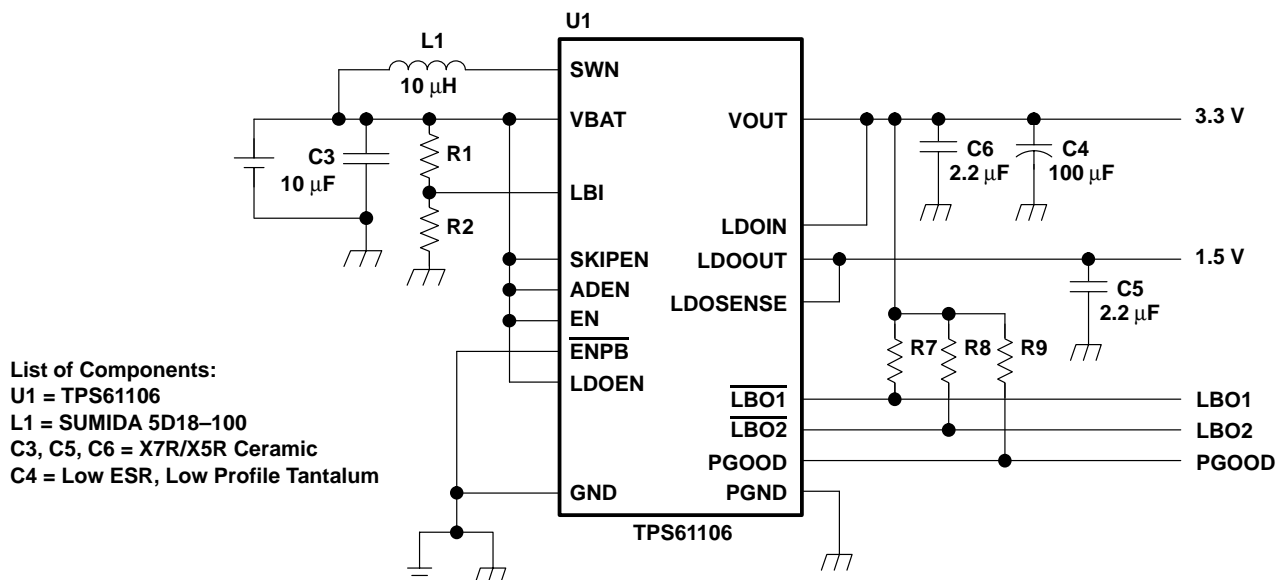


Figure 30. Low Profile Solution, Maximum Height 1,8 mm

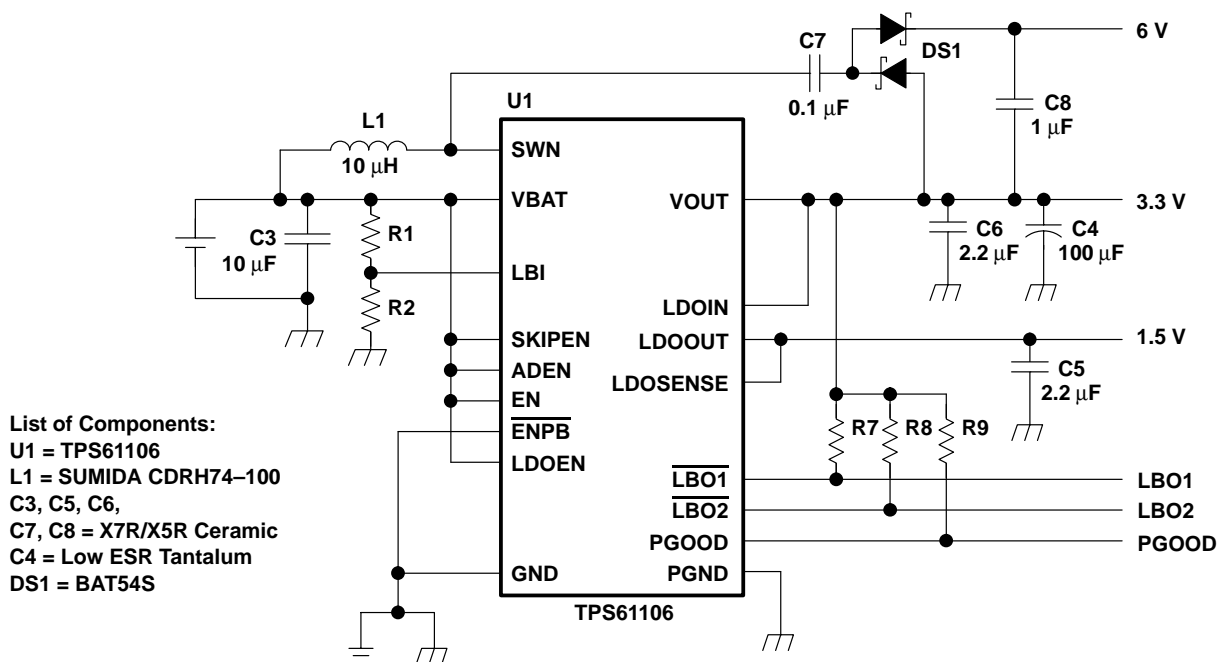


Figure 31. Dual Power Supply With Auxiliary Positive Output Voltage

APPLICATION INFORMATION

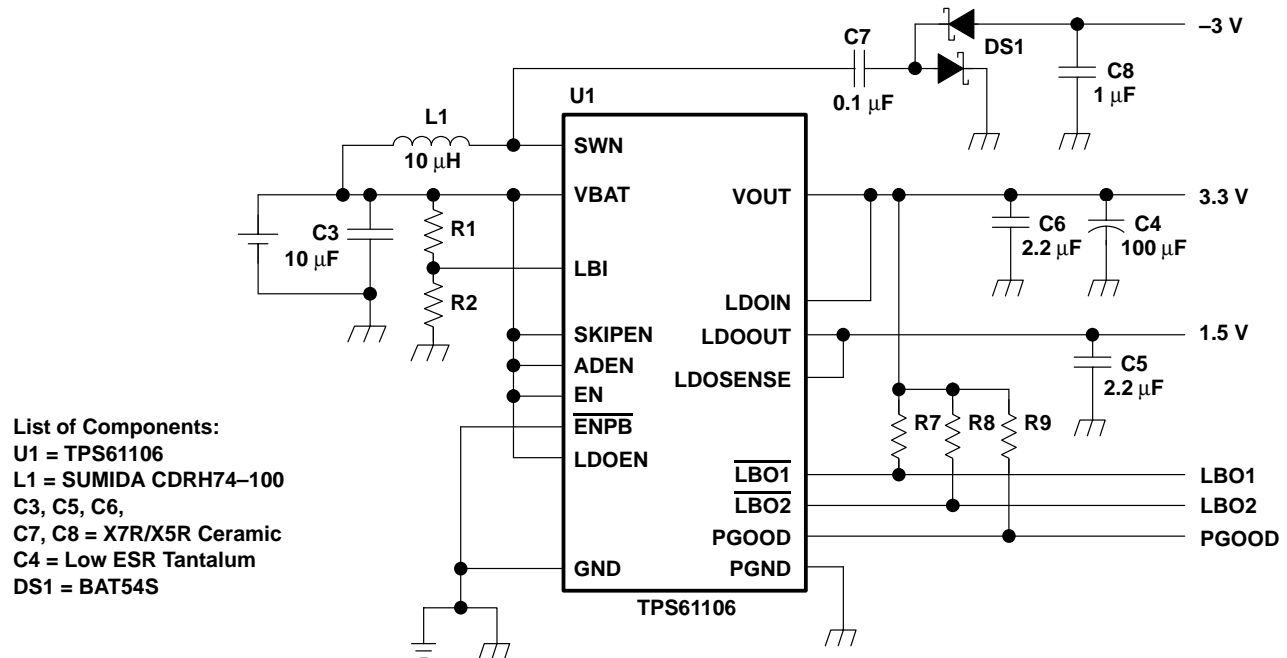


Figure 32. Dual Power Supply With Auxiliary Negative Output Voltage

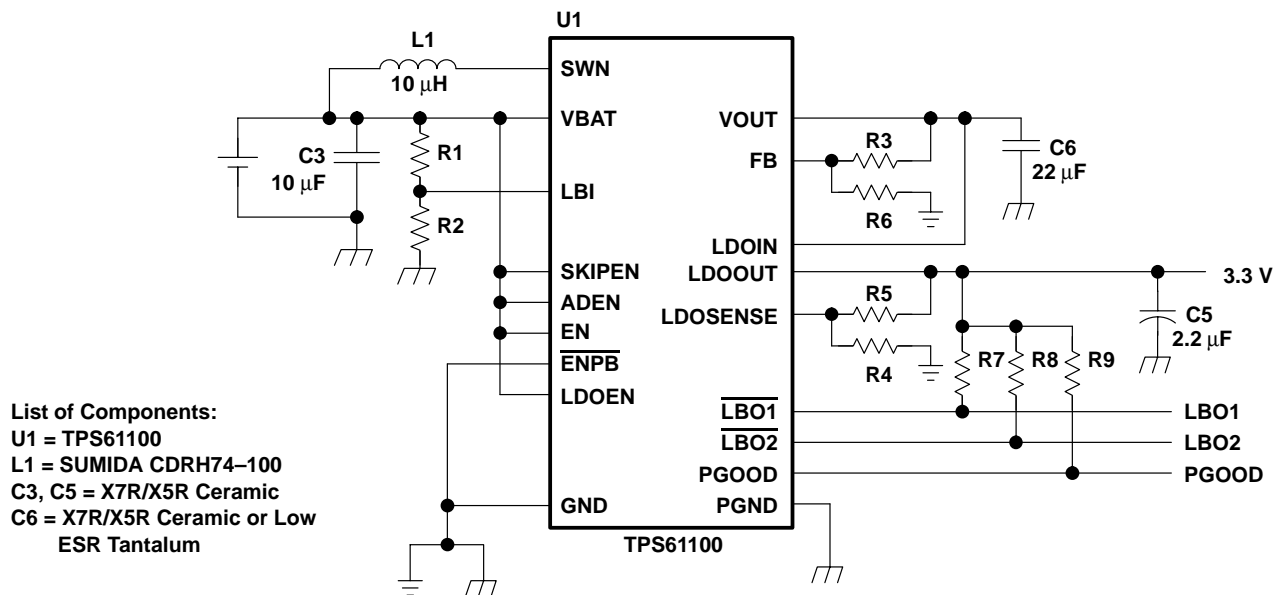


Figure 33. Single Output Using LDO as Filter

APPLICATION INFORMATION

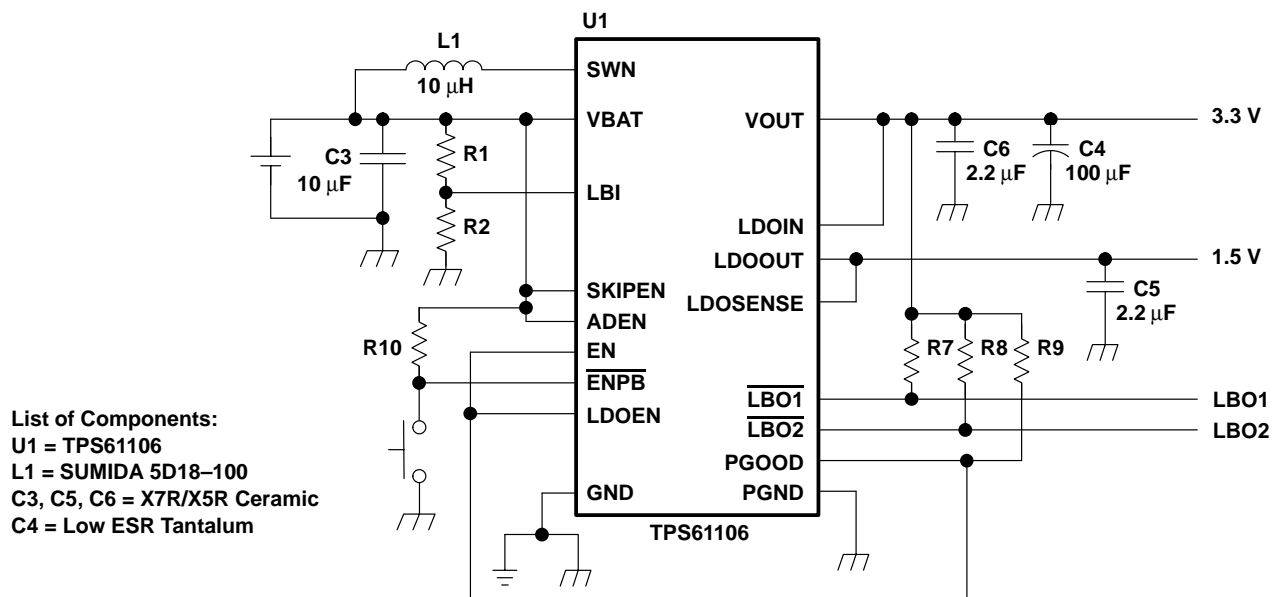


Figure 34. Simple Solution Using a Pushbutton for Start-Up

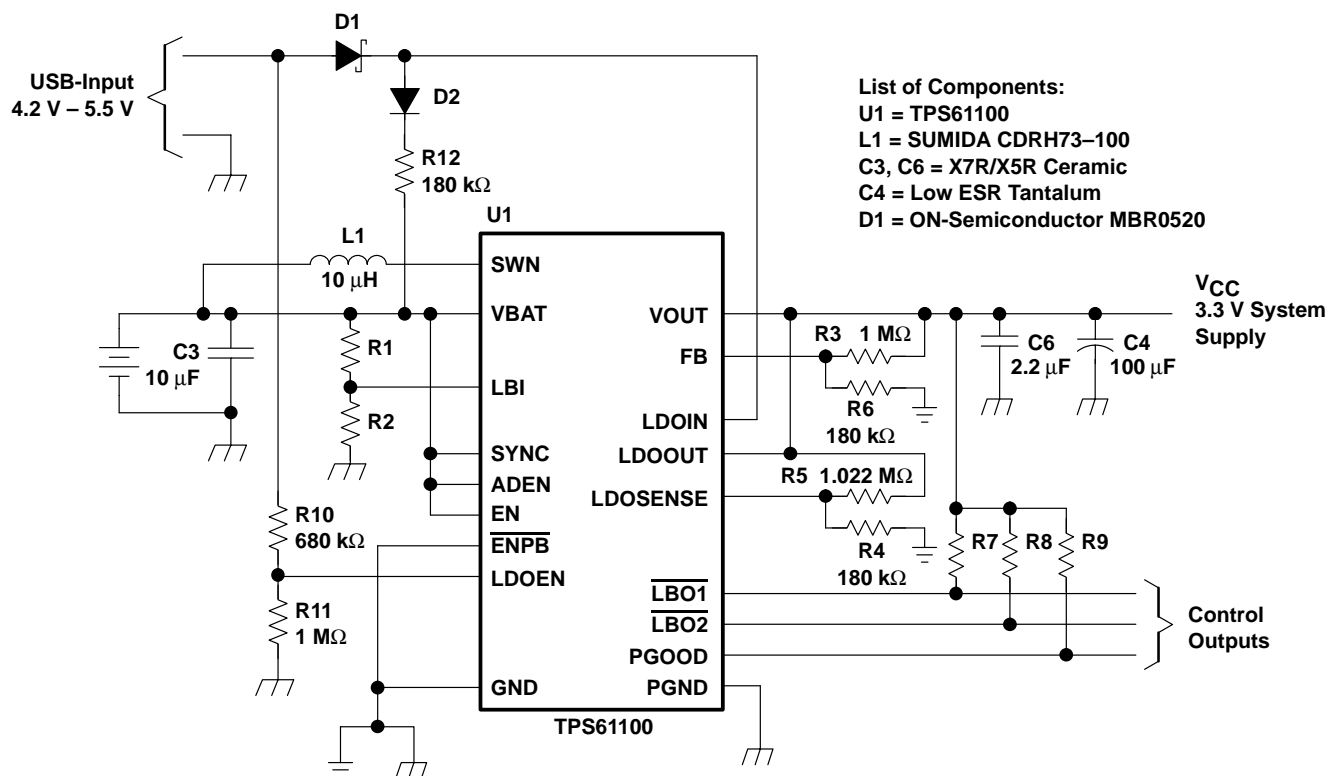


Figure 35. Dual Input Power Supply

APPLICATION INFORMATION

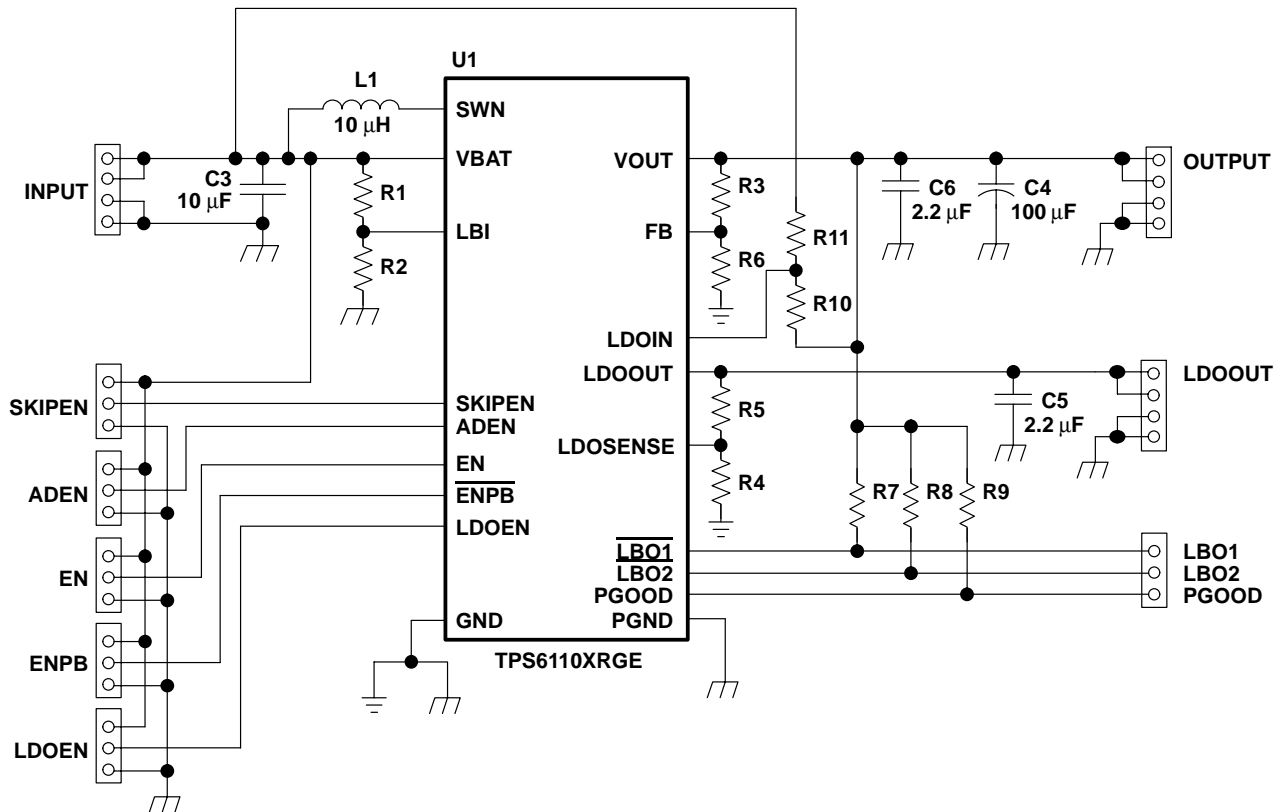


Figure 36. TPS6110x EVM Circuit Diagram

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow in the system.

The maximum junction temperature (T_J) of the TPS6110x devices is 150°C. The thermal resistance of the 20-pin TSSOP package (PW) is $R_{\theta JA} = 155$ K/W (QFN package, RGE, 161 K/W). Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 420 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

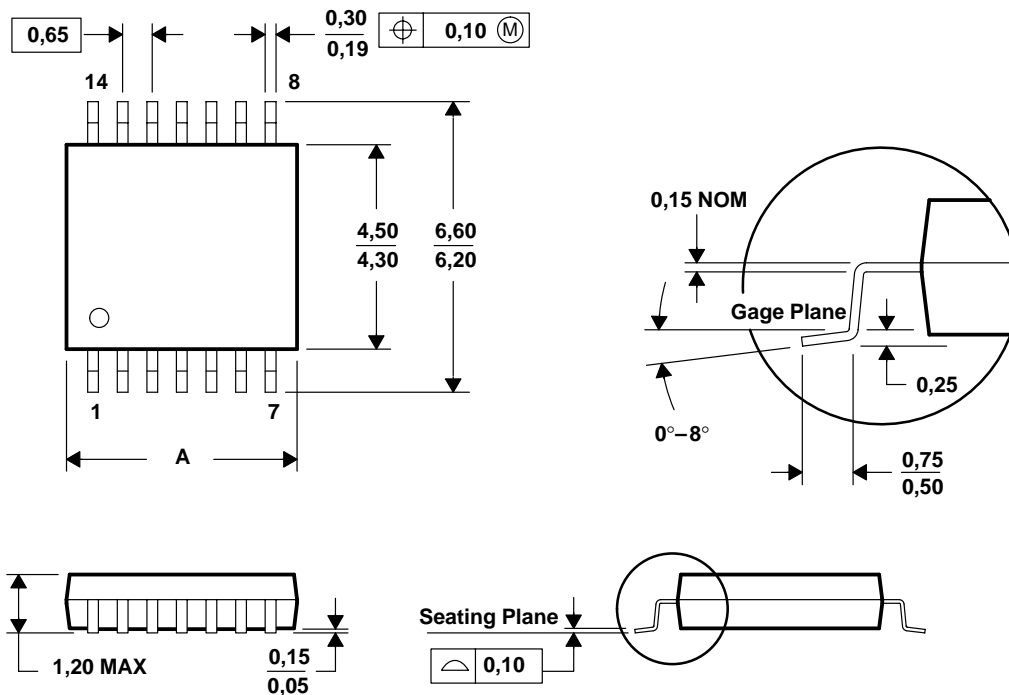
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150^\circ\text{C} - 85^\circ\text{C}}{155 \text{ K/W}} = 420 \text{ mW} \quad (9)$$

MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

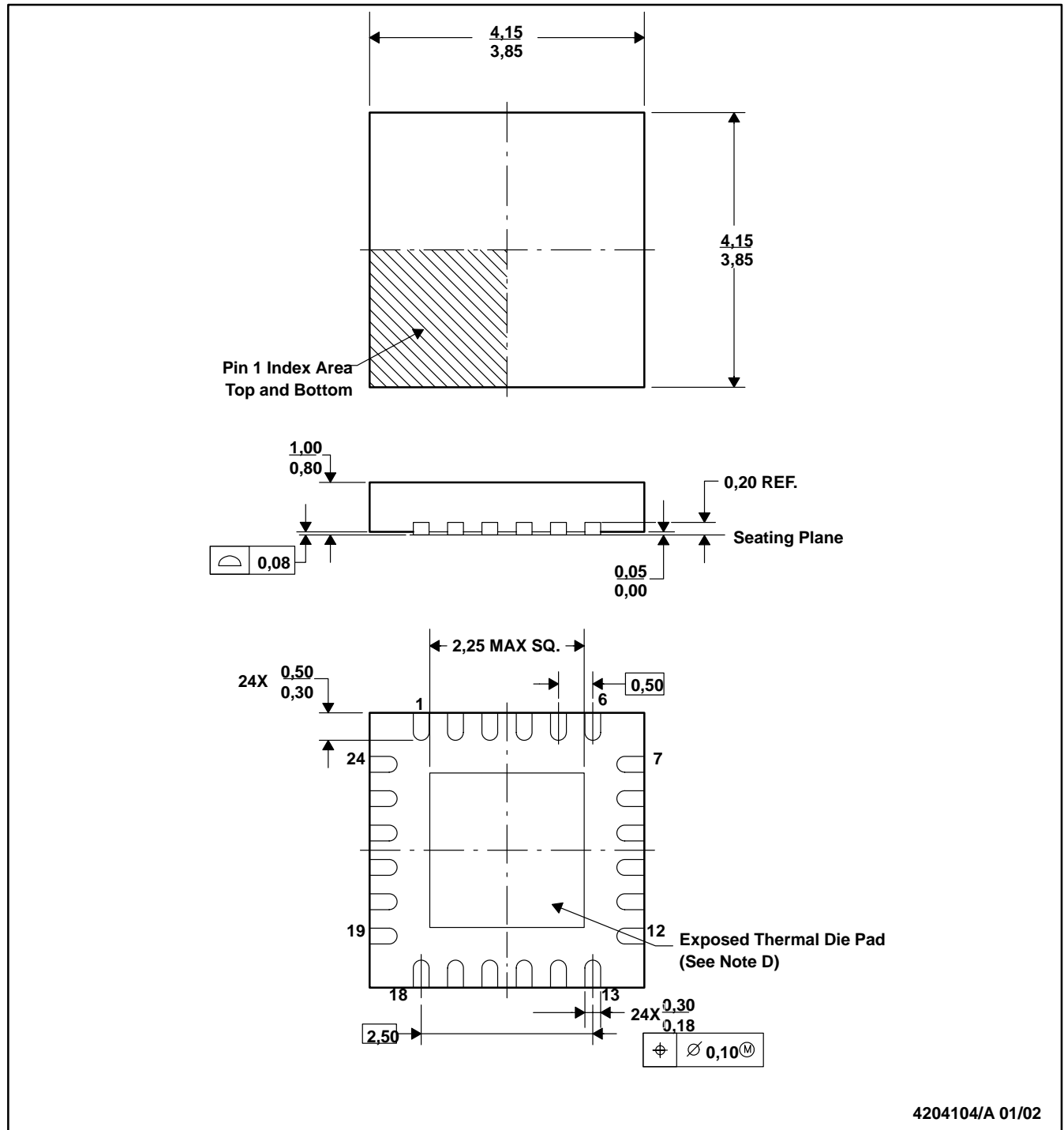
4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

RGE (S-PQFP-N24)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads, (QFN) package configuration.
 - D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
 - E. Falls within JEDEC M0-220.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265