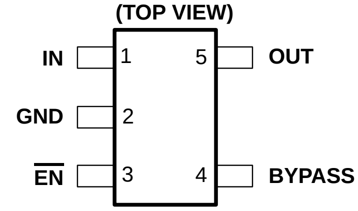
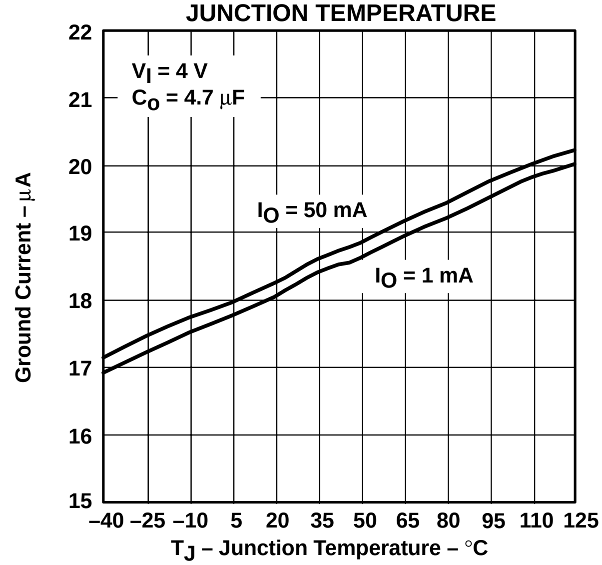
- **50-mA Low-Dropout Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.8-V, 3.0-V**
- **Output Noise Typically 56 μV_{RMS} (TPS79030)**
- **Only 17 μA Quiescent Current at 50 mA**
- **1 μA Quiescent Current in Standby Mode**
- **Dropout Voltage Typically 57 mV at 50 mA (TPS79030)**
- **Over Current Limitation**
- **–40°C to 125°C Operating Junction Temperature Range**
- **5-Pin SOT-23 (DBV) Package**

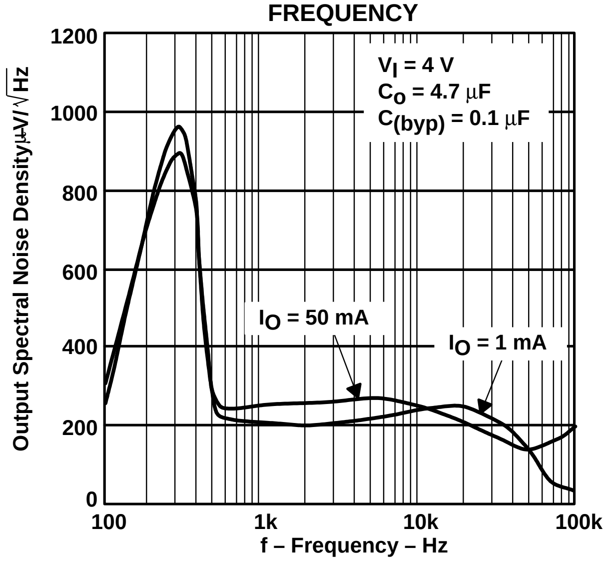
DBV PACKAGE
(TOP VIEW)



TPS79030
GROUND CURRENT
vs
JUNCTION TEMPERATURE



TPS78930
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



description

The TPS790xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, ultralow-power operation, low-output noise, and miniaturized packaging. These regulators feature low-dropout voltages and ultralow quiescent current compared to conventional LDO regulators. An internal resistor, in conjunction with an external bypass capacitor, creates a low-pass filter to reduce the noise. The TPS79030 exhibits only 56 μV_{RMS} of output voltage noise using 0.01 μF bypass and 10 μF output capacitors. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS790xx series devices are ideal for micropower operations, low output noise, and where board space is limited.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 57 mV at 50 mA of load current (TPS79030), and is directly proportional to the load current. The quiescent current is ultralow (17 μA typically) and is stable over the entire range of output load current (0 mA to 50 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life.

description (continued)

The TPS790xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at T_J = 25°C. The TPS790xx is offered in 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3.0 V.

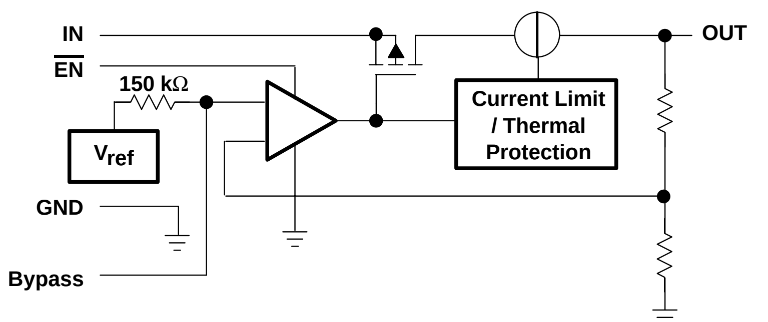
AVAILABLE OPTIONS

T_J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
–40°C to 125°C	1.5 V	SOT-23 (DBV)	TPS79015DBVT†	TPS79015DBVR‡	PEBI
	1.8 V		TPS79018DBVT†	TPS79018DBVR‡	PECI
	2.5 V		TPS79025DBVT†	TPS79025DBVR‡	PEDI
	2.8 V		TPS79028DBVT†	TPS79028DBVR‡	PEEI
	3.0 V		TPS79030DBVT†	TPS79030DBVR‡	PEFI

† The DBVT indicates tape and reel of 250 parts.
‡ The DBVR indicates tape and reel of 3000 parts.

functional block diagram

TPS79015/18/25/28/30



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	4	I	Bypass
EN	3	I	Enable input
GND	2		Ground
IN	1	I	Input supply voltage
OUT	5	O	Regulated output voltage

detail description

The TPS790xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS790xx is essentially constant from no load to maximum load.

The TPS790xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low output noise, low quiescent current (17 µA typically), and enable inputs to reduce supply currents to 1 µA when the regulators are turned off.

The internal voltage reference is a key source of noise in a LDO regulator. The TPS790xx has a BYPASS pin which is connected to the voltage reference through a 150-kΩ internal resistor. The 150-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150-kΩ resistor and external capacitor.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the EN input will disable the TPS790xx internal circuitry, reducing the supply current to 1 µA. A voltage of less than 0.9 V on the $\overline{EN}$ input will enable the TPS790xx and will enable normal operation to resume. The $\overline{EN}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1) . . . . –0.3 V to 13.5 V
Voltage range at $\overline{EN}$ . . . . –0.3 V to V_I + 0.3 V
Voltage on OUT, FB . . . . 7 V
Peak output current . . . . Internally limited
ESD rating, HBM . . . . 2 kV
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K‡	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K§	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

‡ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
§ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 2)	2.7		10	V
Continuous output current, I_O (see Note 3)	0		50	mA
Operating junction temperature, T_J	–40		125	°C

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula: $V_I(min) = V_O(max) + V_{DO}$ (max load)
3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free–air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$V, $C_o = 4.7\ \mu F$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 µA to 50 mA load) (see Note 4)	TPS79015	T_J = 25°C,	2.7 V < V_I < 10 V		1.5		V
		T_J = –40°C to 125°C,	2.7 V < V_I < 10 V	1.455		1.545	
	TPS79018	T_J = 25°C,	2.8 V < V_I < 10 V		1.8		
		T_J = –40°C to 125°C,	2.8 V < V_I < 10 V	1.746		1.854	
	TPS79025	T_J = 25°C,	3.5 V < V_I < 10 V		2.5		
		T_J = –40°C to 125°C,	3.5 V < V_I < 10 V	2.425		2.575	
	TPS79028	T_J = 25°C,	3.8 V < V_I < 10 V		2.8		
		T_J = –40°C to 125°C,	3.8 V < V_I < 10 V	2.716		2.884	
	TPS79030	T_J = 25°C,	4.0 V < V_I < 10 V		3		
		T_J = –40°C to 125°C,	4.0 V < V_I < 10 V	2.910		3.090	
Quiescent current (GND current) (see Note 4)		$\overline{EN}$ = 0 V, T_J = 25°C	10 µA < I_O < 50 mA,		17		µA
		$\overline{EN}$ = 0 V, T_J = –40°C to 125°C	I_O = 50 mA,			28	
Load regulation		$\overline{EN}$ = 0 V, T_J = 25°C	I_O = 10 µA to 50 mA,		8		mV
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 4 and 5)		V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.04		%/V
		V_O + 1 V < V_I ≤ 10 V, T_J = –40°C to 125°C				0.1	
Output noise voltage (TPS79030)		BW = 300 Hz to 50 kHz, $C_{(byp)}$ = 0.01 µF, C_o = 10 µF, I_O = 50 mA, T_J = 25°C			56		µVrms
Output current limit		V_O = 0 V,	See Note 4		350	750	mA
Standby current		$\overline{EN}$ = V_I ,	2.7 < V_I < 10 V		1		µA
		T_J = –40°C to 125°C				2	µA

NOTES: 4. The minimum IN operating voltage is 2.7 V or V_O (typ) + 1 V, whichever is greater. The maximum IN voltage is 10 V. The minimum output current is 10 µA and the maximum output current is 50 mA.
5. If $V_O \le 1.8$ V then V_{Imax}... If $V_O \le 1.8$ V then $V_{Imin} = 2.7$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{Imin} = V_O + 1$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

electrical characteristics over recommended operating free–air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$V, $C_o = 4.7\ \mu$F (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
High level enable input voltage		2.7 V < V_I < 10 V		1.7			V
Low level enable input voltage		2.7 V < V_I < 10 V				0.9	V
Power supply ripple rejection (TPS79030)		f = 1 kHz, T_J = 25°C,	C_o = 10 μF, $C_{(byp)}$ = 0.01 μF		85		dB
Input current (EN)		$\overline{EN}$ = 0 V		–1	0	1	μA
		$\overline{EN}$ = V_I		–1		1	μA
Dropout voltage (see Note 6)	TPS79028	I_O = 50 mA,	T_J = 25°C		60		mV
		I_O = 50 mA,	T_J = –40°C to 125°C			125	
Dropout voltage (see Note 6)	TPS79030	I_O = 50 mA,	T_J = 25°C		57		
		I_O = 50 mA,	T_J = –40°C to 125°C			115	

6. IN voltage equals V_O(typ) –100 mV; The TPS79030 output voltage is set to 2.9 V. The TPS79015, TPS79018, and TPS79025 dropout voltage is limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1, 2, 3
		vs Junction temperature	4, 5, 6
	Ground current	vs Junction temperature	7
	Output spectral noise density	vs Frequency	8 – 10
	Root mean squared output noise	vs Bypass capacitance	11
Z_o	Output impedance	vs Frequency	12
V_{DO}	Dropout voltage	vs Junction temperature	13
	Ripple rejection	vs Frequency	14 – 16
V_O	Output voltage, enable voltage	vs Time (start-up)	17 – 19
	Line transient response		20, 22
	Load transient response		21, 23
	Equivalent series resistance (ESR)	vs Output current	24, 25

TYPICAL CHARACTERISTICS

TPS79025
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

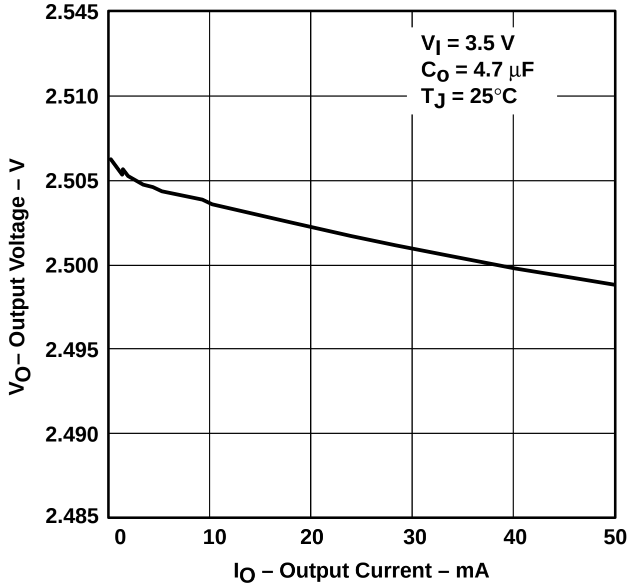


Figure 1

TPS79015
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

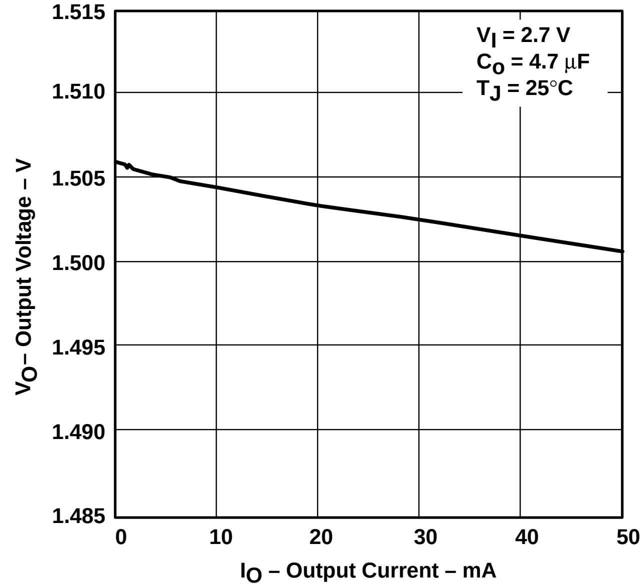


Figure 2

TPS79030
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

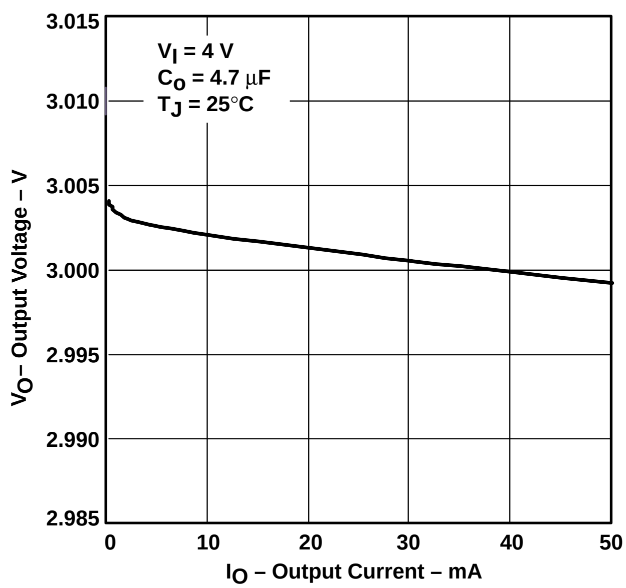


Figure 3

TPS79015
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

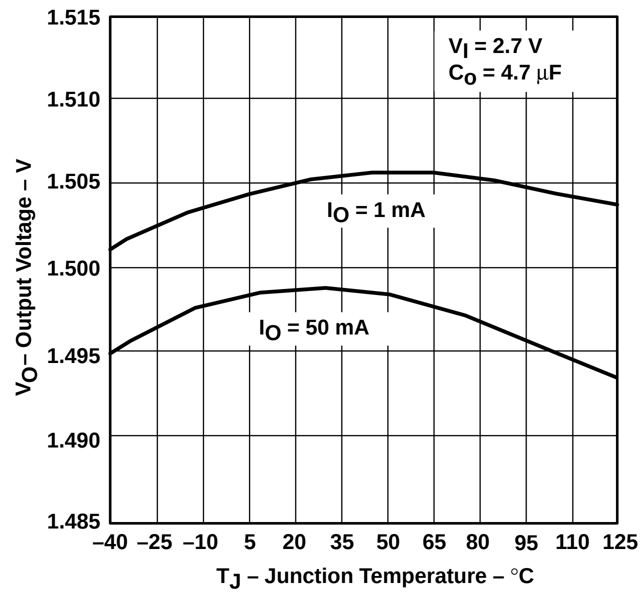


Figure 4

TYPICAL CHARACTERISTICS

TPS79025
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

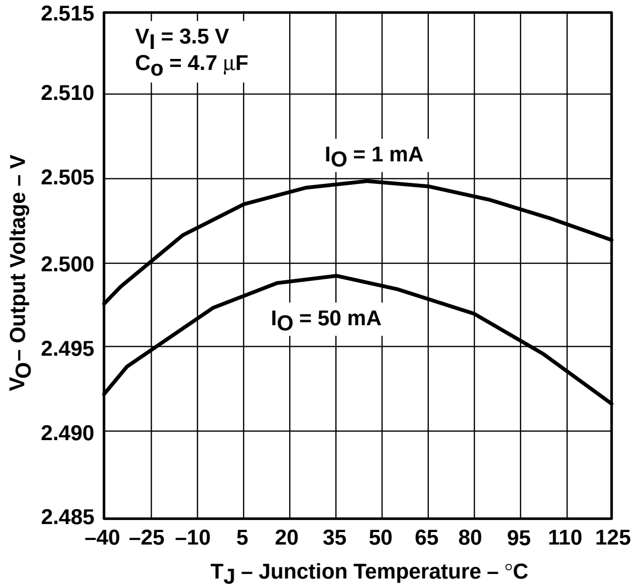


Figure 5

TPS79030
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

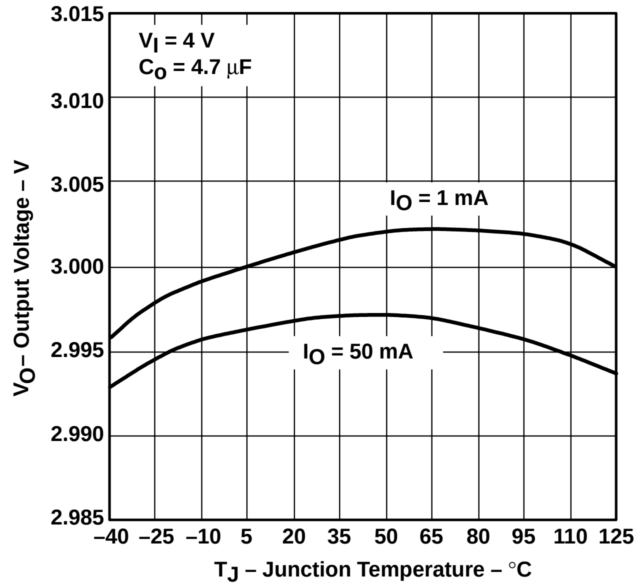


Figure 6

TPS79030
GROUND CURRENT
vs
JUNCTION TEMPERATURE

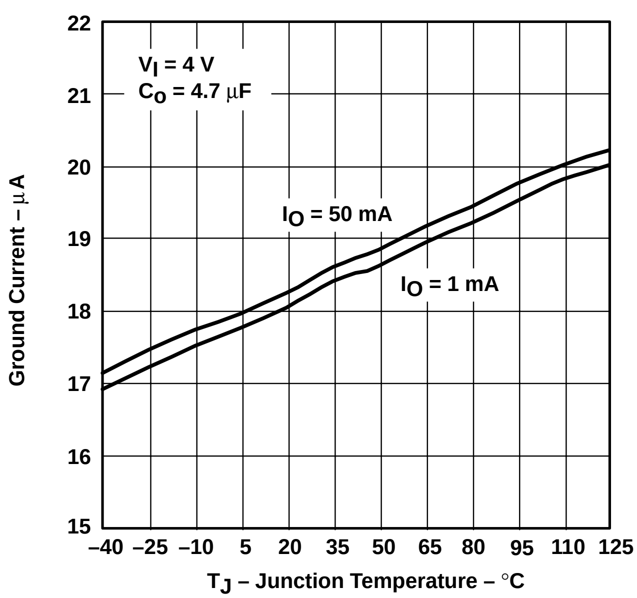


Figure 7

TPS79030
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

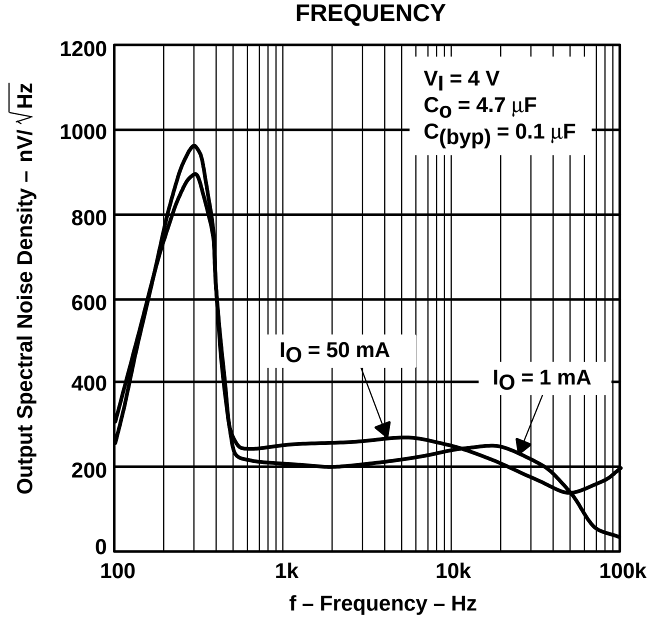


Figure 8

TYPICAL CHARACTERISTICS

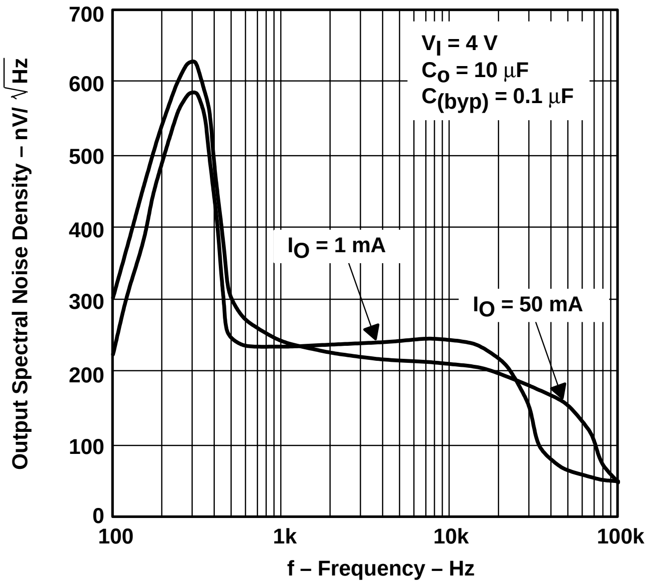


Figure 9

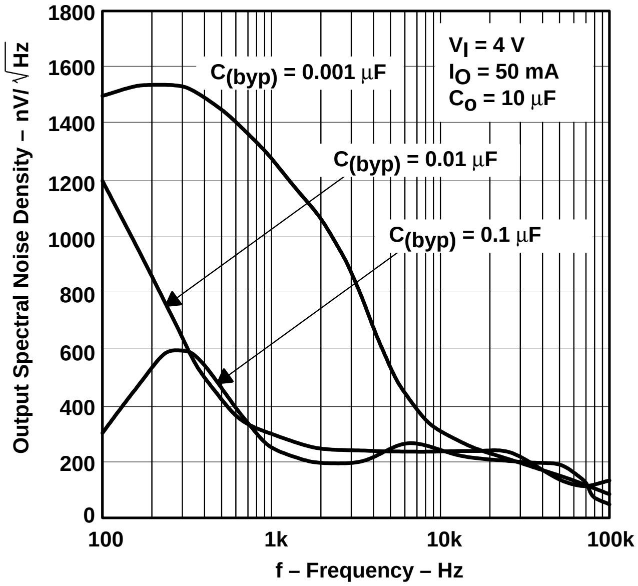


Figure 10

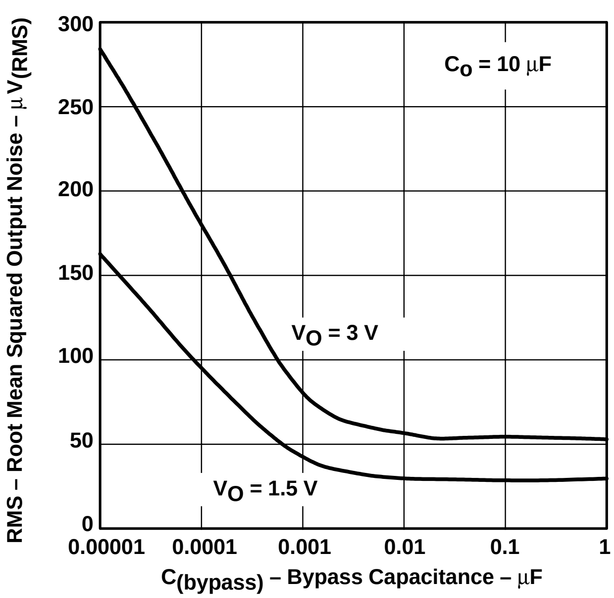


Figure 11

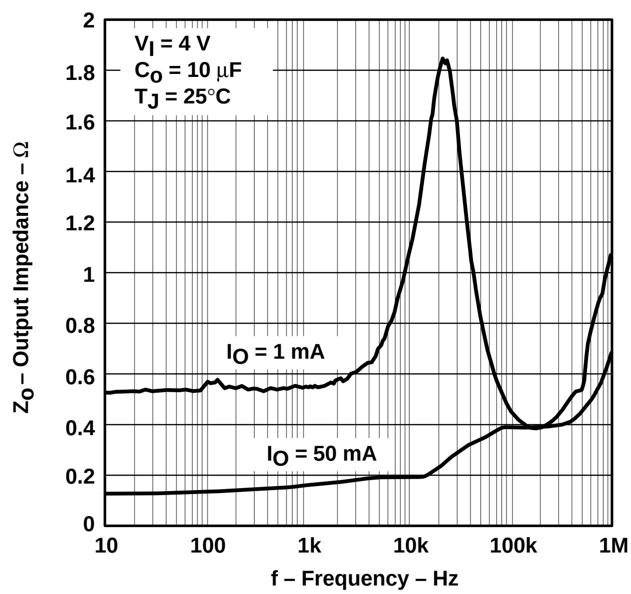


Figure 12

TYPICAL CHARACTERISTICS

TPS79030
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

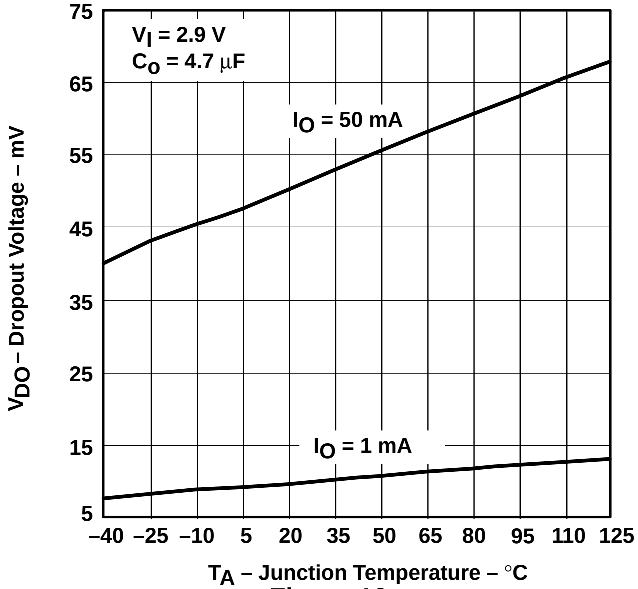


Figure 13

TPS79030
RIPPLE REJECTION
vs
FREQUENCY

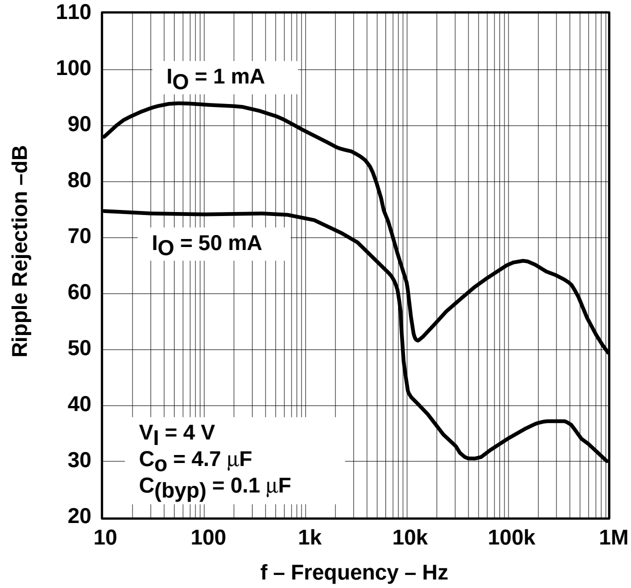


Figure 14

TPS79030
RIPPLE REJECTION
vs
FREQUENCY

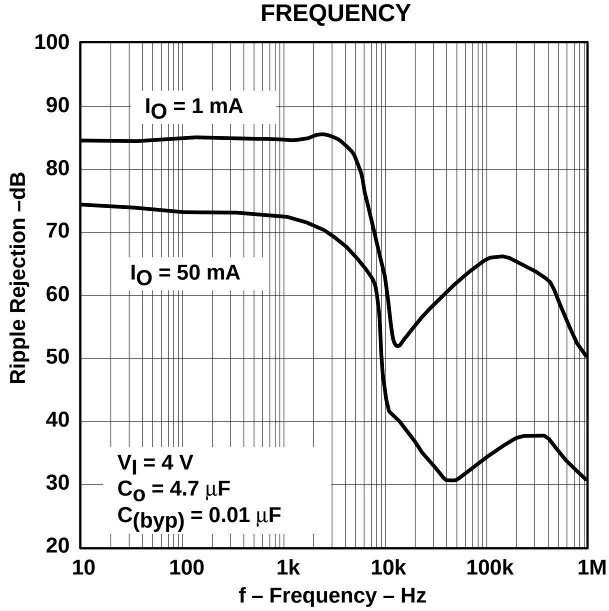


Figure 15

TPS79030
RIPPLE REJECTION
vs
FREQUENCY

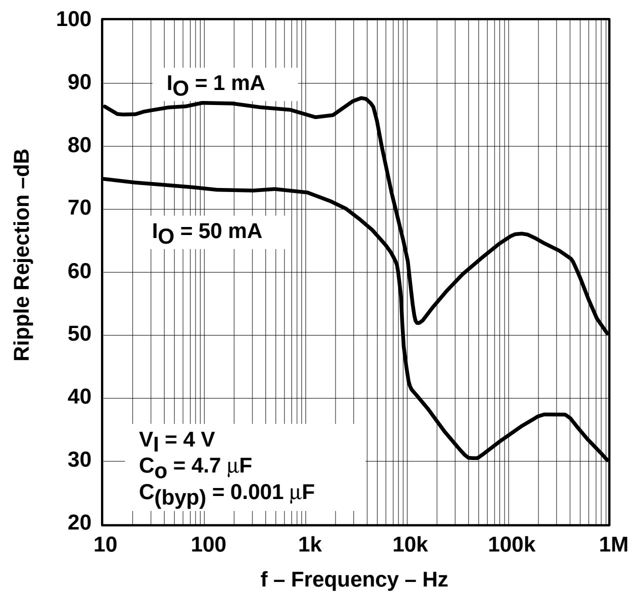


Figure 16

TYPICAL CHARACTERISTICS

TPS79030
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

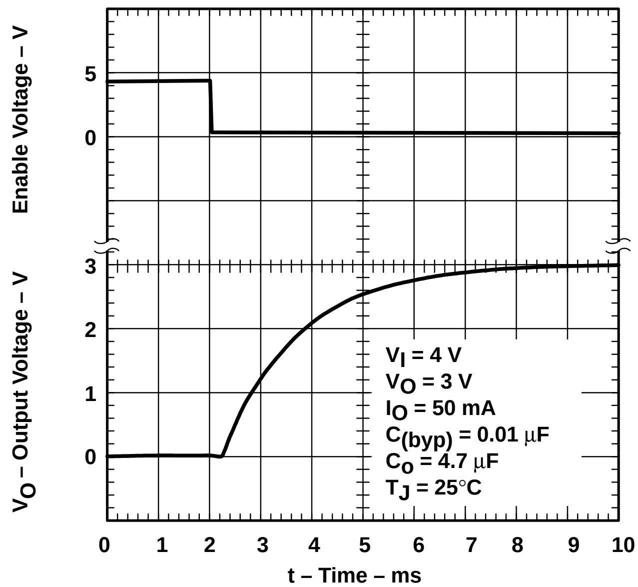


Figure 17

TPS79030
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

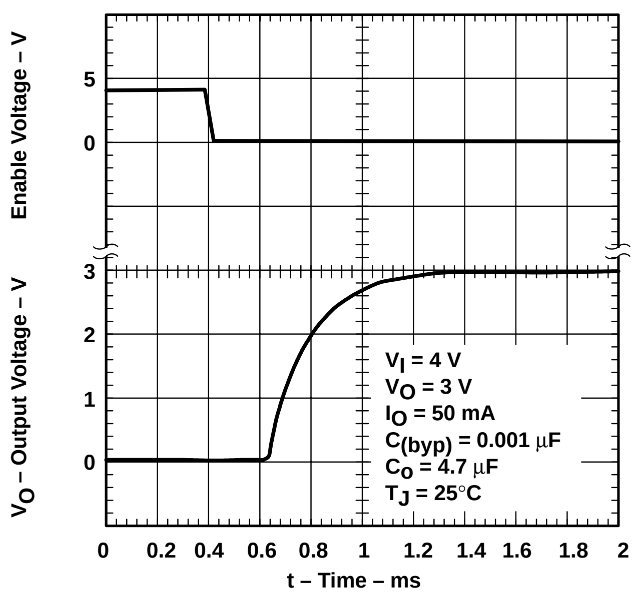


Figure 18

TPS79030
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

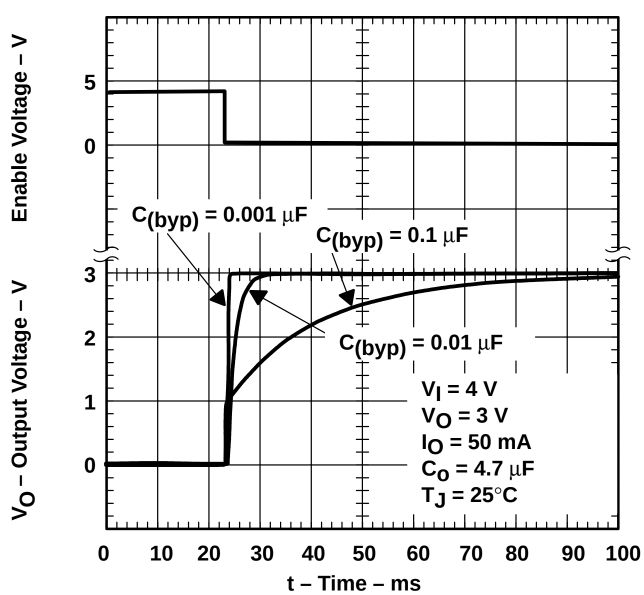


Figure 19

TYPICAL CHARACTERISTICS

TPS79015
LINE TRANSIENT RESPONSE

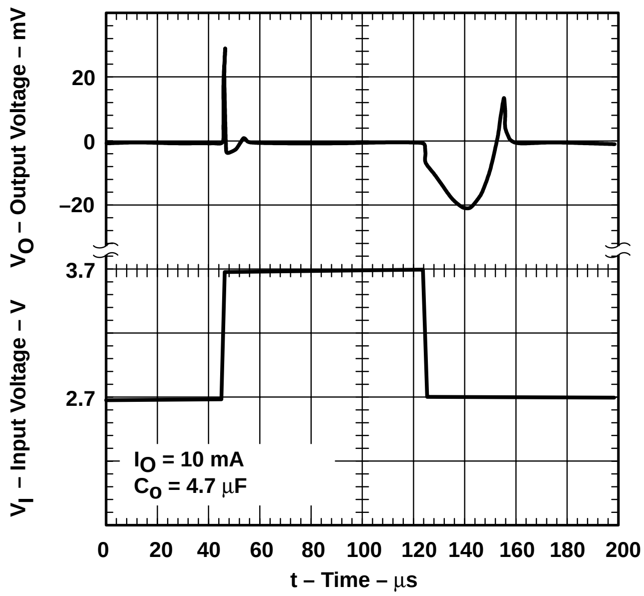


Figure 20

TPS79015
LOAD TRANSIENT RESPONSE

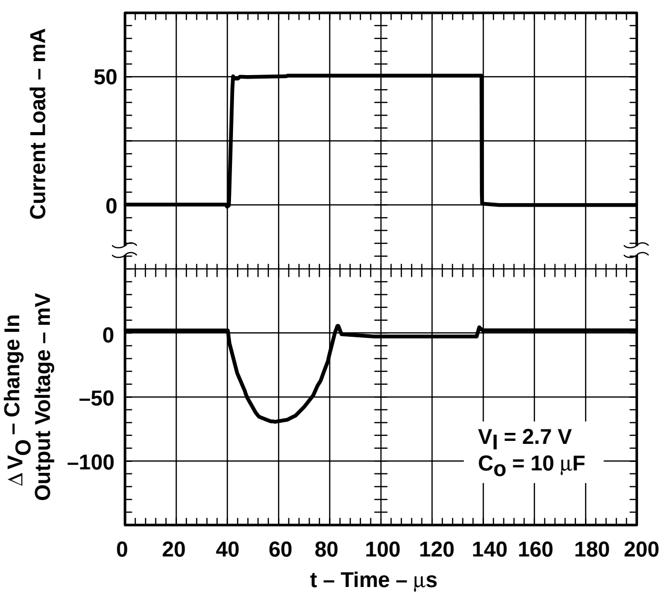


Figure 21

TPS79030
LINE TRANSIENT RESPONSE

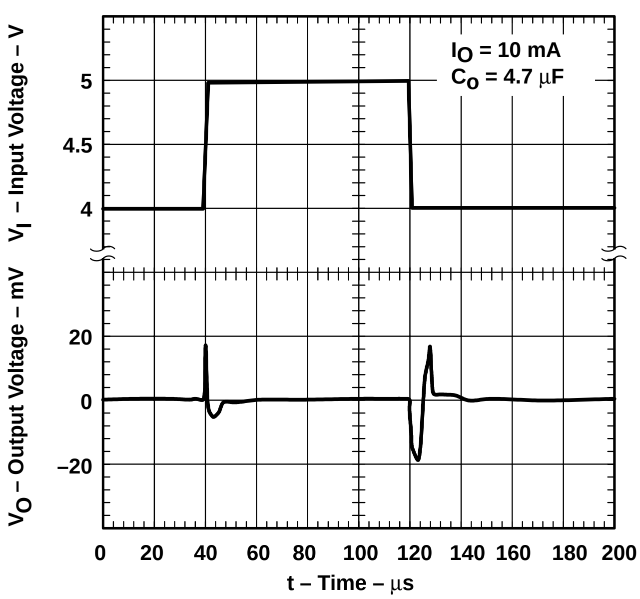


Figure 22

TPS79030
LOAD TRANSIENT RESPONSE

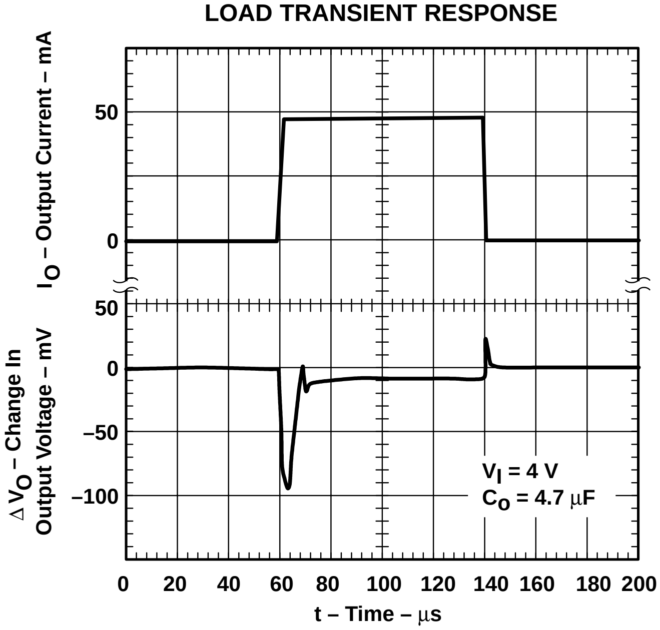


Figure 23

TYPICAL CHARACTERISTICS

TPS79030
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

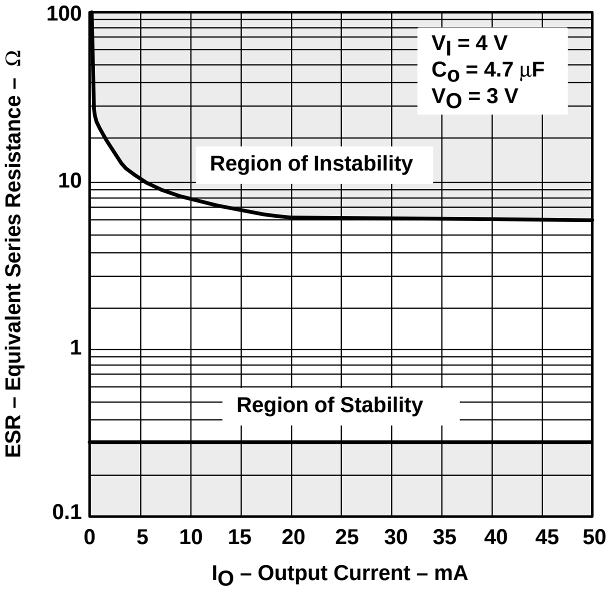


Figure 24

TPS79030
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

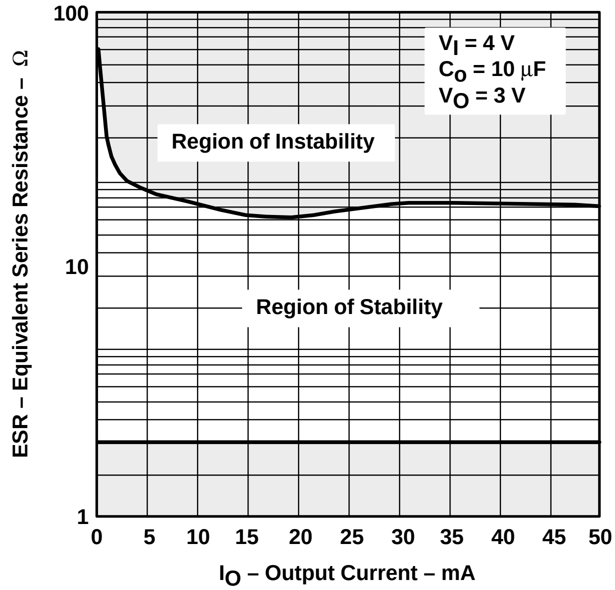


Figure 25

APPLICATION INFORMATION

The TPS790xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low quiescent current (17 µA typically), and enable inputs to reduce supply currents to less than 1 µA when the regulators are turned off.

A typical application circuit is shown in Figure 26.

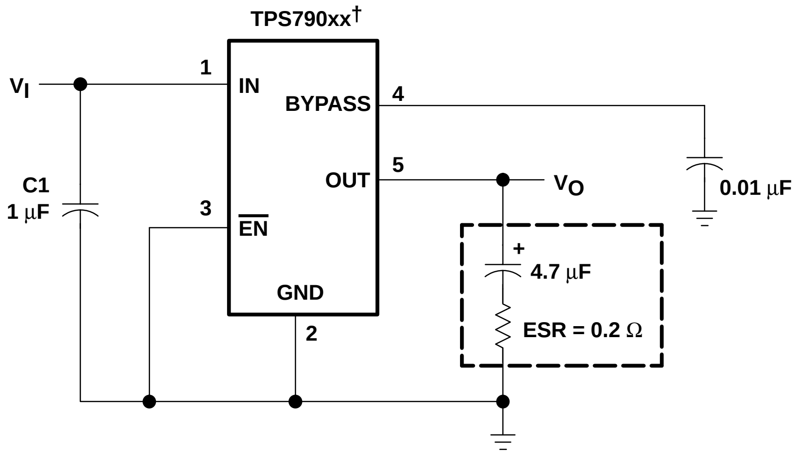


Figure 26. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS790xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS790xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 µF. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω to ensure stability. Capacitor values larger than 4.7 µF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 µF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6.0 × 3.2

† Size is in mm. The ESR maximum resistance is in Ohms at 100 kHz and T_A = 25°C. Contact the manufacturer for the minimum ESR values.

APPLICATION INFORMATION

external capacitor requirements (continued)

The external bypass capacitor, used in conjunction with an internal resistor to form a low-pass filter, should be a low ESR ceramic capacitor. For example, the TPS79030 exhibits only 56 μV_{RMS} of output voltage noise using a 0.01 µF ceramic bypass capacitor and a10 µF ceramic output capacitors. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150 kΩ resistor and external capacitor.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

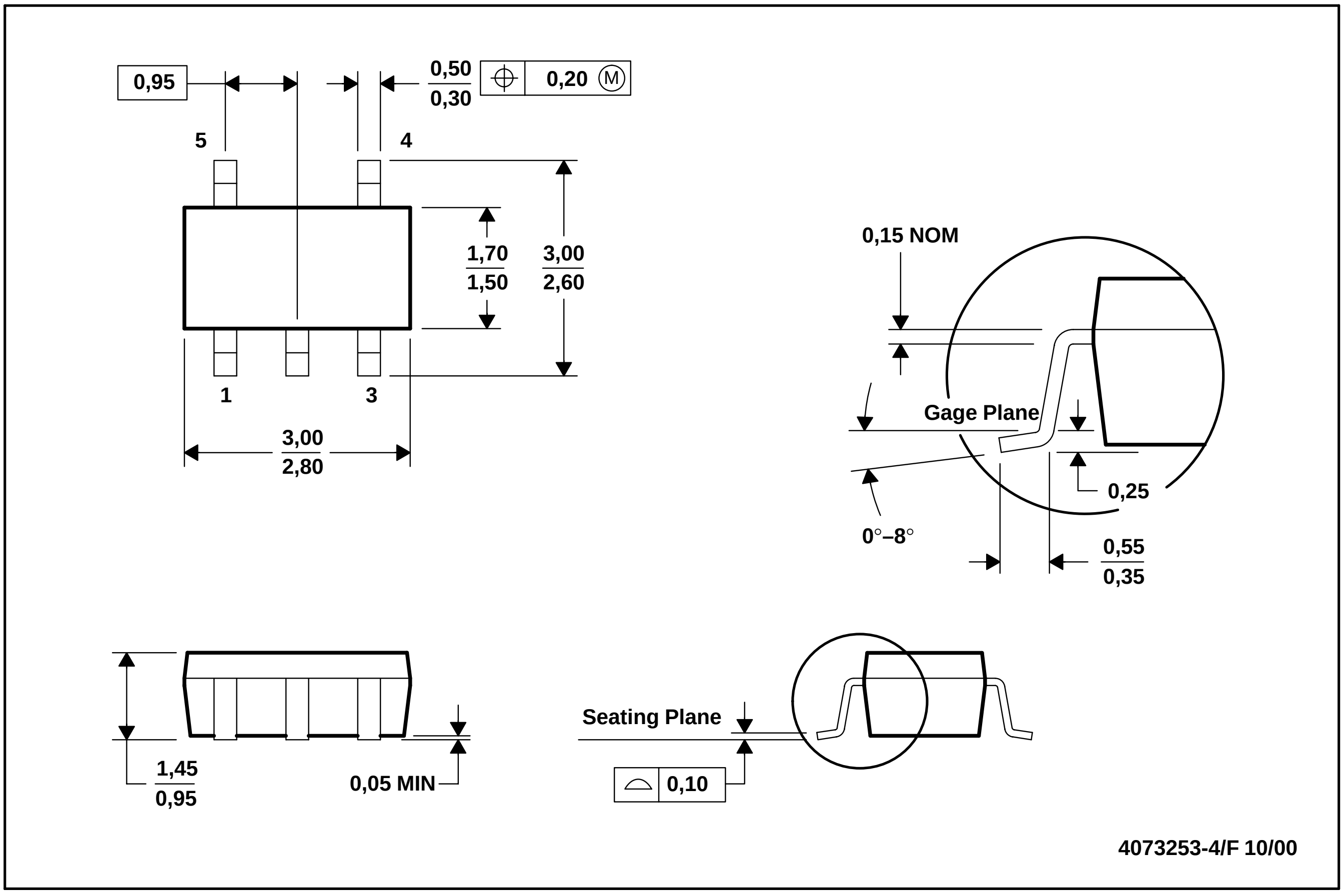
regulator protection

The TPS790xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS790xx features internal current limiting and thermal protection. During normal operation, the TPS790xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

MECHANICAL DATA

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

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