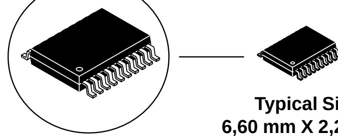


Typical Size
6,60 mm X 2,20 mm

SLVS416 – FEBRUARY 2002

3-V TO 6-V INPUT, 3-A OUTPUT SYNCHRONOUS-BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

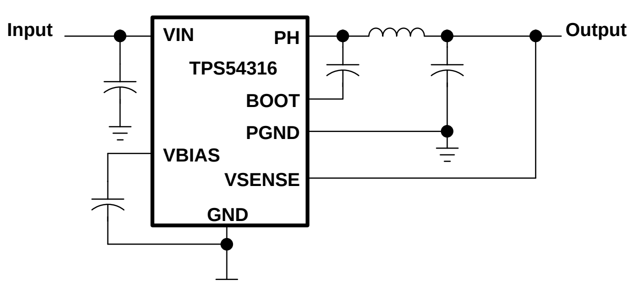
FEATURES

- **60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Source or Sink Current**
- **0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V Fixed Output Voltage Devices With 1% Initial Accuracy**
- **Internally Compensated for Ease of Use and Minimal Component Count**
- **Fast Transient Response**
- **Wide PWM Frequency—Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

APPLICATIONS

- **Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V**
- **Point of Load Regulation for High-Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking, and Optical Communications Infrastructure**
- **Portable Computing/Notebook PCs**

Simplified Schematic

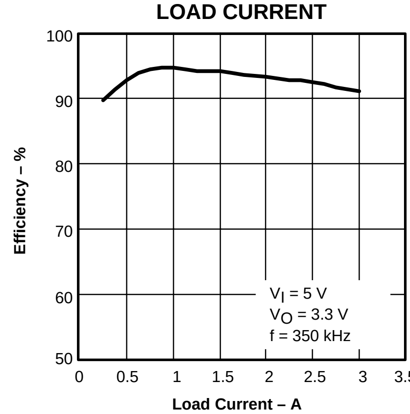


DESCRIPTION

As members of the SWIFT™ family of dc/dc regulators, the TPS54311, TPS54312, TPS54313, TPS54314, TPS54315 and TPS54316 low-input-voltage high-output-current synchronous-buck PWM converters integrate all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that provides fast response under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling and supply sequencing.

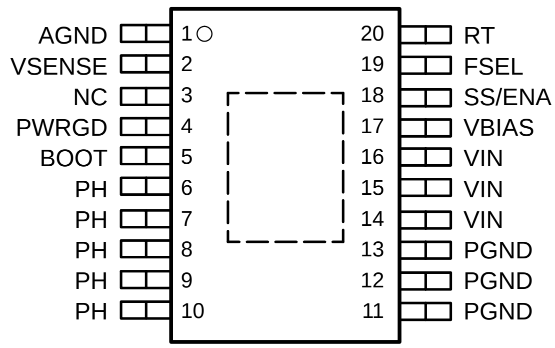
The TPS54311-6 devices are available in a thermally enhanced 20-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

EFFICIENCY vs LOAD CURRENT



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE	PACKAGED DEVICES PLASTIC HTSSOP (PWP)†	T_J	OUTPUT VOLTAGE	PACKAGED DEVICES PLASTIC HTSSOP (PWP)†
–40°C to 125°C	0.9 V	TPS54311PWP	–40°C to 125°C	1.8 V	TPS54314PWP
	1.2 V	TPS54312PWP		2.5 V	TPS54315PWP
	1.5 V	TPS54313PWP		3.3 V	TPS54316PWP

† The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54316PWPR). See application section of datasheet for PowerPAD™ drawing and layout information.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1		Analog ground. Return for compensation network/output divider, slow start capacitor, VBIAS capacitor, RT resistor and FSEL pin. Make PowerPad™ connection to AGND.
BOOT	5		Bootstrap input. 0.022 µF to 0.1 µF low ESR capacitor connected from BOOT to PH generates floating drive for the high-set FET driver.
FSEL	19		Frequency select input. Provides logic input to select between two internally set switching frequencies.
NC	3		No connection
PGND	11–13		Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
PH	6–10		Phase input/output. Junction of the internal high- and low-side power MOSFETs, and output inductor.
PWRGD	4		Powergood open drain output. Hi-Z when VSENSE ≥90% VREF, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
RT	20		Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, Fs.
SS/ENA	18		Slow start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
VBIAS	17		Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1 µF to 1.0 µF ceramic capacitor.
VIN	14–16		Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1 µF to 10 µF ceramic capacitor.
VSENSE	2		Error amplifier inverting input. Connect directly to output voltage sense point.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Input voltage range, V_I:	VIN, SS/ENA, FSEL	–0.3 V to 7 V
	RT	–0.3 V to 6 V
	VSENSE	–0.3 V to 4 V
	BOOT	–0.3 V to 17 V
Output voltage range, V_O:	VBIAS, PWRGD	–0.3 V to 7 V
	PH	–0.6 V to 10 V
Source current, I_O:	PH	Internally Limited
	VBIAS	6 mA
Sink current, I_S:	PH	6 A
	SS/ENA, PWRGD	10 mA
Voltage differential:	AGND to PGND	±0.3 V
Continuous power dissipation		See Power Dissipation Rating Table
Operating virtual junction temperature range, T_J		–40°C to 125°C
Storage temperature, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE‡

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
20-Pin PWP with solder	26.0 mW/°C	3.85 W§	2.12 W	1.54 W
20-Pin PWP without solder	57.5 mW/°C	1.73 W	0.96 W	0.69 W

‡ Test board conditions:
1. 3" x 3", 2 layers, Thickness: 0.062"
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 10 thermal vias (see Recommended Land Pattern in applications section of this data sheet)

For more information on the PWP package, refer to TI technical brief, literature number SLMA002.

§ Maximum power dissipation may be limited by over current protection.

ADDITIONAL 3A SWIFT™ DEVICES

DEVICE	OUTPUT VOLTAGE
TPS54310	0.9 V to 3.3 V

related dc/dc products

- UCC3585—dc/dc controller
- PT5500 series—3-A plug-in modules
- TPS757xx—3-A low dropout regulator

electrical characteristics, T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
	Input voltage range at VIN			3.0		6.0	V
I_Q	Quiescent current		Fs = 350 kHz, FSEL ≤ 0.8 V, RT open, Phase pin open		6.2	9.6	mA
			Fs = 550 kHz, FSEL ≥ 2.5 V, RT open, Phase pin open		8.4	12.8	mA
			Shutdown, SS/ENA = 0 V		1	1.4	mA
UNDER VOLTAGE LOCK OUT							
$V_{IT(start)}$	Start threshold voltage at UVLO				2.95	3.0	V
$V_{IT(stop)}$	Stop threshold voltage at UVLO			2.70	2.80		V
V_{hys}	Hysteresis voltage at UVLO			0.14	0.16		V
t_f, t_r	Rising and falling edge deglitch at UVLO		See Note 1		2.5		µs
BIAS VOLTAGE							
	Output voltage at VBIAS		I_{VBIAS} = 0	2.70	2.80	2.90	V
	Output current at VBIAS		See Note 2			100	µA
OUTPUT VOLTAGE							
V_O	Output voltage	TPS54311	T_J = 25°C, VIN = 5.0 V		0.9		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
		TPS54312	T_J = 25°C, VIN = 5.0 V		1.2		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
		TPS54313	T_J = 25°C, VIN = 5.0V		1.5		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
		TPS54314	T_J = 25°C, VIN = 5.0 V		1.8		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–3%		3%	
		TPS54315	T_J = 25°C, VIN = 5.0V		2.5		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–3%		3%	
		TPS54316	T_J = 25°C, VIN = 5.0V		3.3		V
			3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–3%		3%	
REGULATION							
	Line regulation		I_L = 1.5A, 350 ≤ fs ≤ 550 kHz, T_J = 85°C, See Note 1, 3			0.21	%/V
	Load regulation		I_L = 0 to 3A, 350 ≤ fs ≤ 550 kHz, T_J = 85°C, See Notes 1 and 3			0.21	%/A

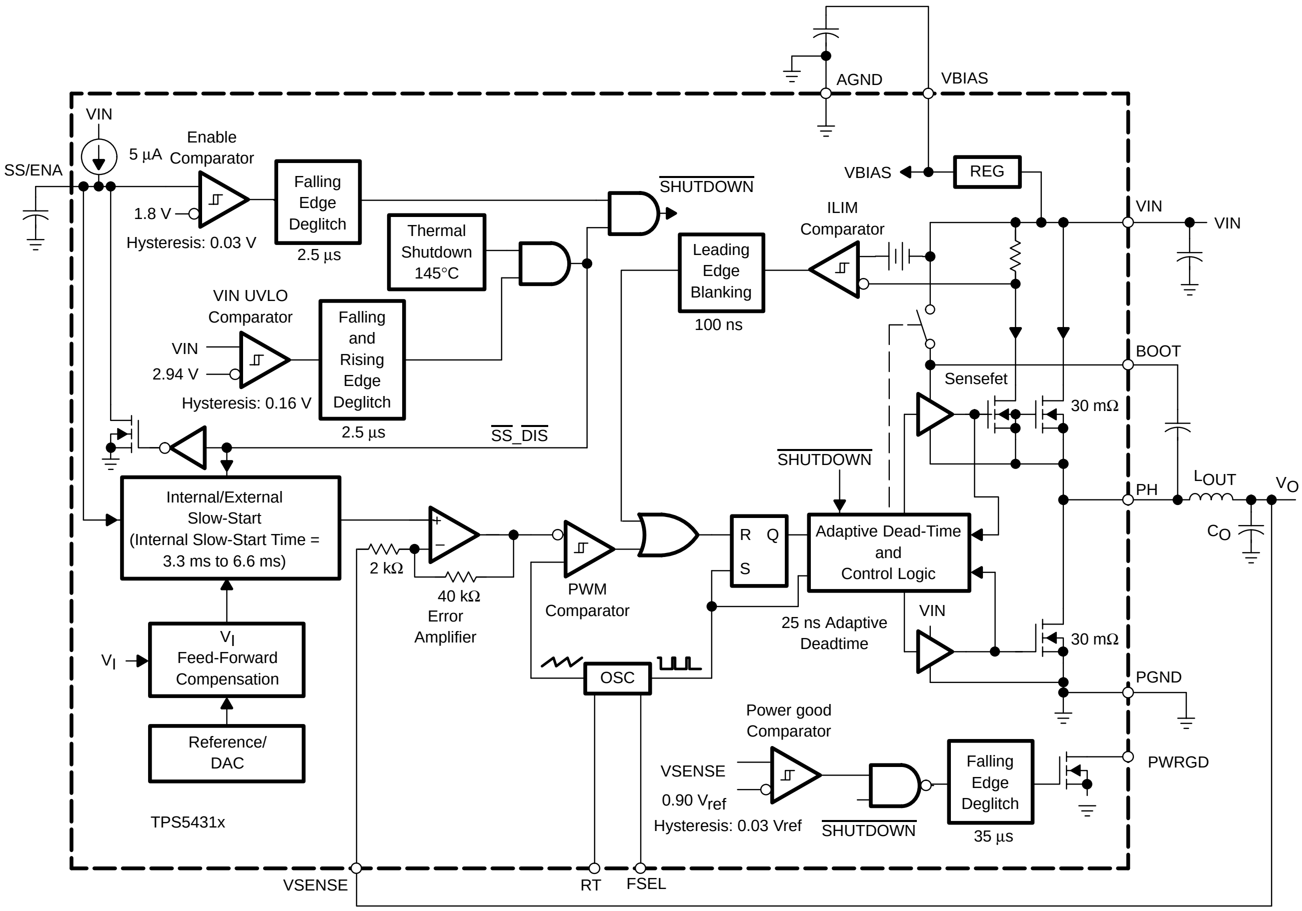
NOTES: 1. Ensured by design
2. Static resistive loads only
3. Tested using circuit in Figure 9

electrical characteristics, T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)(continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR					
Internally set-free running frequency	SYNC<=0.8 V, RT open	280	350	420	kHz
	SYNC>= 2.5V, RT open	440	550	660	
Externally set-free running frequency range	RT = 180 kΩ (1% resistor to AGND)	252	280	308	kHz
	RT = 100 kΩ (1% resistor to AGND)	460	500	540	
	RT = 68 kΩ (1% resistor to AGND)	663	700	762	
High level threshold at FSEL		2.5			V
Low level threshold at FSEL				0.8	V
Ramp valley	See Note 1		0.75		V
Ramp amplitude (peak to peak)	See Note 1		1		V
Minimum controllable on time	See Note 1			200	nS
Maximum duty cycle	See Note 1	90%			
ERROR AMPLIFIER					
Error amplifier open loop voltage gain	See Note 1		26		dB
Error amplifier unity gain bandwidth	See Note 1	3	5		MHz
Error amplifier common mode input voltage range	Powered by internal LDO, See Note 1	0		Vbias	V
PWM COMPARATOR					
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)	10 mV overdrive, See Note 1		70	85	ns
SLOW START / ENABLE					
Enable threshold voltage at SS/ENA		0.95	1.20	1.40	V
Enable hysteresis voltage at SS/ENA	See Note 1		0.03		V
Falling edge deglitch at SS/ENA	See Note 1		2.5		µs
Internal slow-start time		2.6	3.35	4.1	ms
Charge current at SS/ENA	SS/ENA = 0V	3	5	8	µA
Discharge current at SS/ENA	SS/ENA = 1.3 V, V_{IN} = 1.5 V	1.5	2.3	4.0	mA
POWER GOOD					
Power good threshold voltage	VSENSE falling		90		%Vout
Power good hysteresis voltage	See Note 1		3		%Vout
Power good falling edge deglitch	See Note 1		35		µs
Output saturation voltage at PWRGD	I_{sink} = 2.5 mA		0.18	0.30	V
Leakage current, PWRGD	V_{IN} = 5.5 V			1	µA
CURRENT LIMIT					
Current limit	V_{IN} = 3 V (see Note 1)	4.0	6.5		A
	V_{IN} = 6 V (see Note 1)	4.5	7.5		
Current limit leading edge blanking time			100		ns
Current limit total response time			200		ns
THERMAL SHUTDOWN					
Thermal shutdown trip point	See Note 1	135	150	165	°C
Thermal shutdown hysteresis	See Note 1		10		°C
OUTPUT POWER MOSFETS					
Small signal drain-source on power MOSFET switches R_{DS-ON}	I_O = 3A, V_{IN} = 6.0 V See Note 4		59	88	mΩ
	I_O = 3A, V_{IN} = 3.0 V See Note 4		85	136	

NOTES: 3: Tested using circuit in Figure 9
4. Matched MOSFETs, low side R_{DS-ON} production tested, high side R_{DS-ON} ensured by design

internal block diagram



detailed description

undervoltage lock out (UVLO)

An under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5 µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

slow-start/enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5 µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

slow-start/enable (SS/ENA) (continued)

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \left(\frac{1.2\ V}{5\ \mu A}\right) \tag{1}$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \left(\frac{0.7\ V}{5\ \mu A}\right) \tag{2}$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

voltage reference

The voltage reference system produces a precise, temperature stable voltage from a bandgap circuit. A scaling amplifier and DAC are then used to produce the reference voltages for each of the fixed output devices

oscillator and PWM ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the FSEL pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor from the RT pin to AGND and floating the FSEL pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY} = \left(\frac{100\ k\Omega}{RT}\right) \times 500\ kHz \tag{3}$$

The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 180 k to 68 k

detailed description (continued)

error amplifier

The high performance, wide bandwidth, voltage error amplifier is gain limited to provide internal compensation of the control loop. The user is given limited flexibility in choosing output L and C filter components. Inductance values of 4.7 µH to 10 µH are typical and available from several vendors. The resulting designs exhibit good noise and ripple characteristics, along with exceptional transient response. Transient recovery times are typically in the range of 10 to 20 µs.

PWM control

Signals from the error amplifier, oscillator and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead–time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as V_{REF}. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54611–TPS54616 devices are capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

dead-time control and MOSFET drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5 Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

overcurrent protection

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and a differential amplifier with preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

detailed description (continued)

thermal shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point, and will start up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device will cycle continuously: starting up by control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown trip point.

power good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

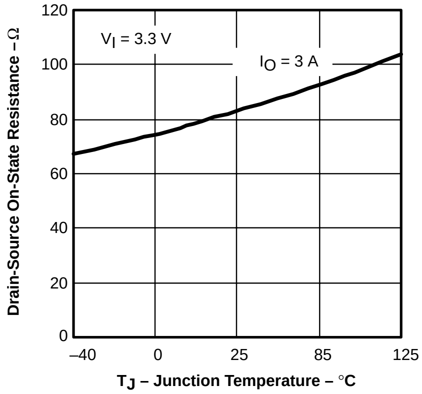


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

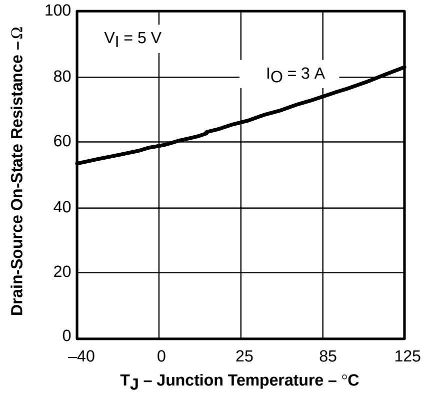


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

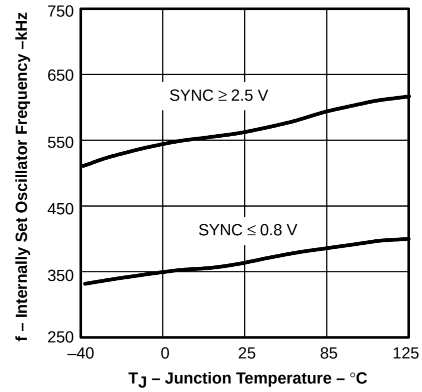


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

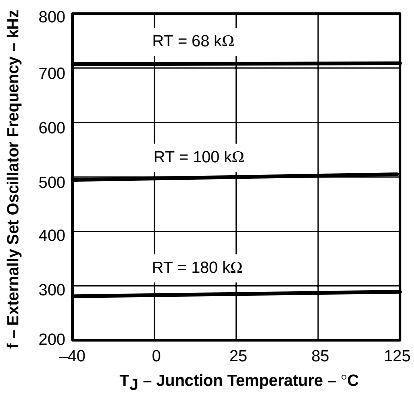


Figure 4

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

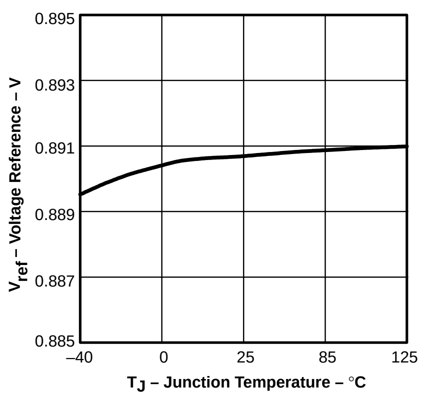


Figure 5

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

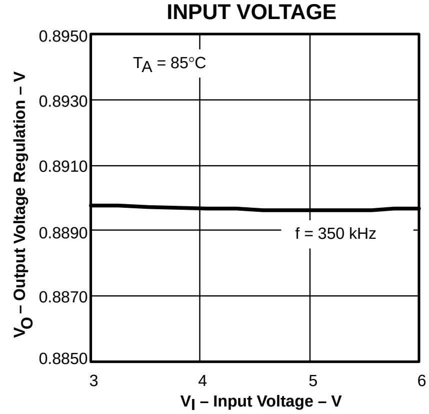


Figure 6

ERROR AMPLIFIER OPEN LOOP RESPONSE

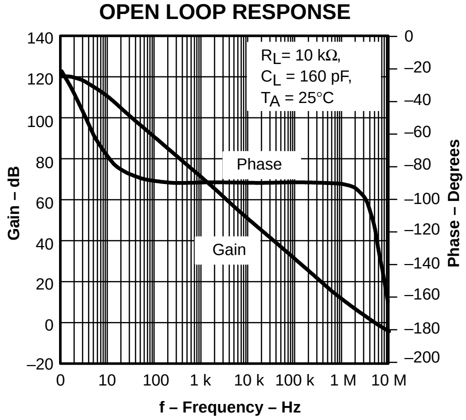


Figure 9

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

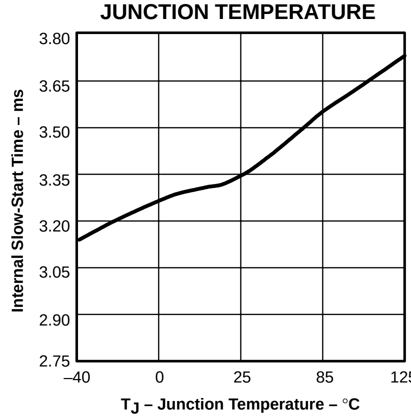


Figure 8

DEVICE POWER LOSSES vs LOAD CURRENT

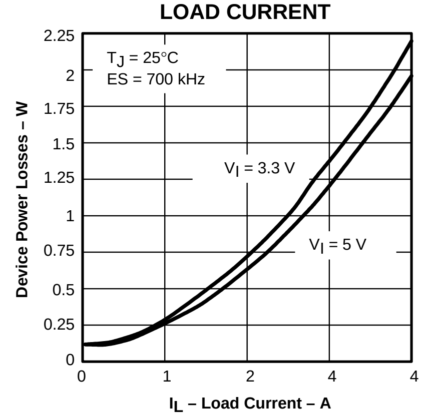


Figure 7

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54314 application. The TPS54314 (U1) can provide up to 3 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the power pad underneath the integrated circuit TPS54314 needs to be soldered well to the printed-circuit board.

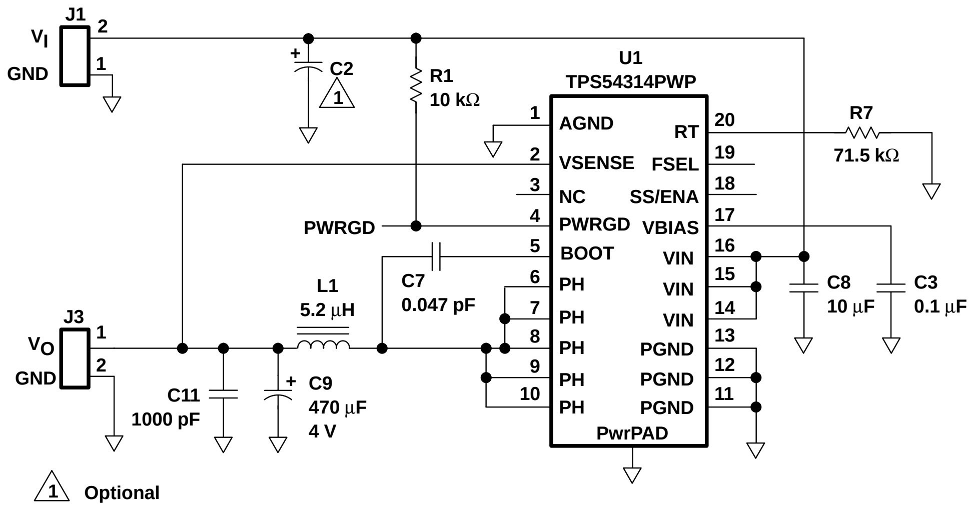


Figure 10. TPS54314 Schematic

input voltage

The input to the circuit is a nominal 5 VDC, applied at J1. The optional input filter (C2) is a 220–uF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 is the decoupling capacitor for the TPS54314 and must be located as close to the device as possible.

feedback circuit

The output voltage of the converter is fed directly into the VSENSE pin of the TPS54314. The TPS54314 is internally compensated to provide stability of the output under varying line and load conditions.

operating frequency

In the application circuit, a 700 kHz operating frequency is selected by leaving FSEL open and connecting a 71.5 kΩ resistor between the RT pin and AGND. Different operating frequencies may be selected by varying the value of R3 using equation 4:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ \text{k}\Omega \tag{4}$$

Alternately, preset operating frequencies of 350 kHz or 550 kHz my be selected by leaving RT open and connecting the FSEL pin to AGND or Vin respectively.

output filter

The output filter is composed of a 5.2 µH inductor and 470 µF capacitor. The inductor is a low dc resistance(16-mΩ) type, Sumida CDRH104R–5R2. The capacitor used is a 4-V POSCAP with a maximum ESR of 40 mΩ. The output filter components work with the internal compensation network to provide a stable closed loop response for the converter.

APPLICATION INFORMATION

grounding and PowerPAD layout

The TPS54311–16 have two internal grounds (analog and power). Inside the TPS54311–16, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be connected directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54311–16, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes should tie together directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54311–16. The layout of the TPS54314 evaluation module is representative of a recommended layout for a 4-layer board. Documentation for the TPS54314 evaluation module can be found on the Texas Instruments web site under the TPS54314 product folder and in the application note, TI literature number SLVA111.

layout considerations for thermal performance

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

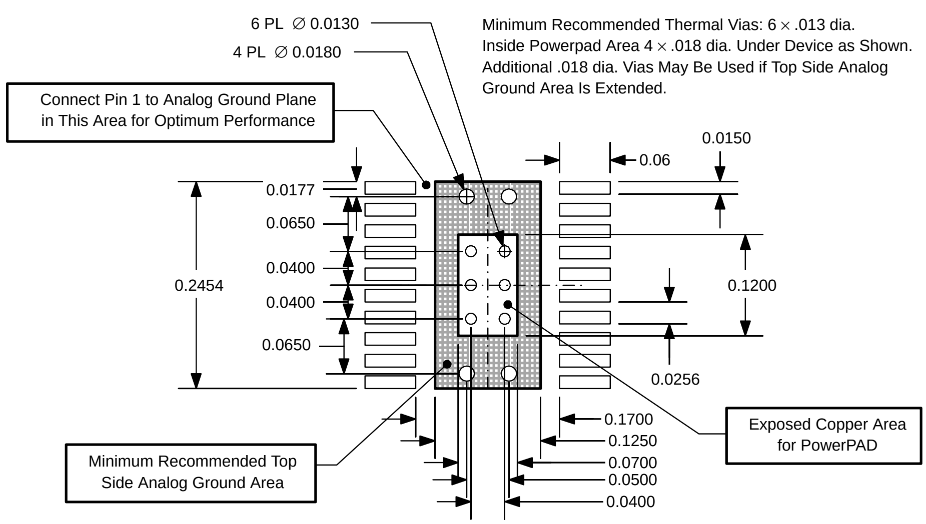


Figure 11. Recommended Land Pattern for 20-Pin PWP PowerPAD

APPLICATION INFORMATION

performance graphs

EFFICIENCY vs LOAD CURRENT

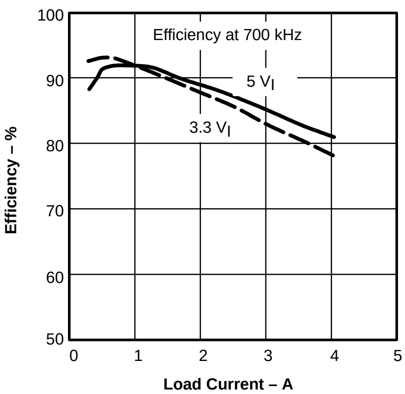


Figure 12

OUTPUT VOLTAGE vs LOAD CURRENT

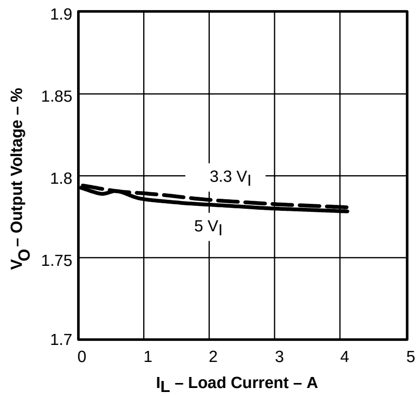


Figure 13

LOOP RESPONSE

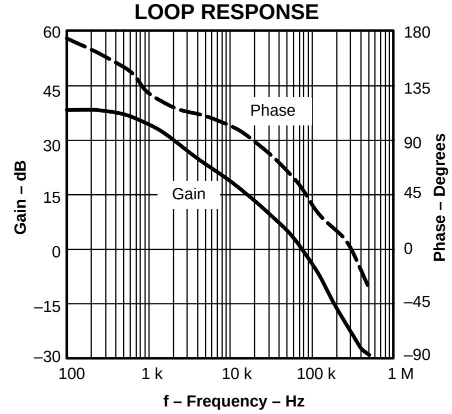


Figure 14

OUTPUT RIPPLE VOLTAGE

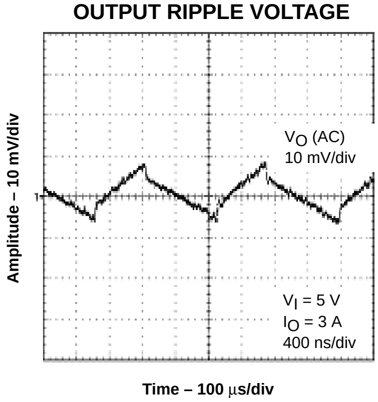


Figure 15

LOAD TRANSIENT RESPONSE

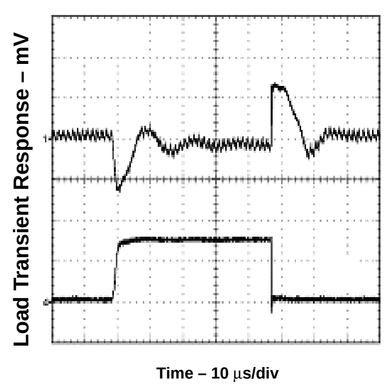


Figure 16

START-UP WAVEFORMS

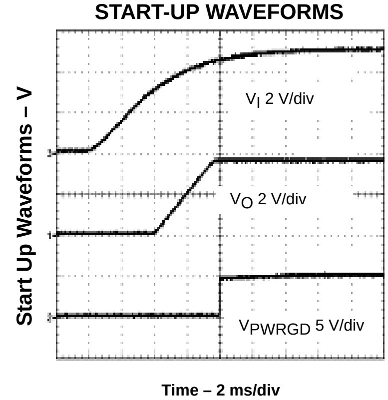


Figure 17

AMBIENT TEMPERATURE vs LOAD CURRENT

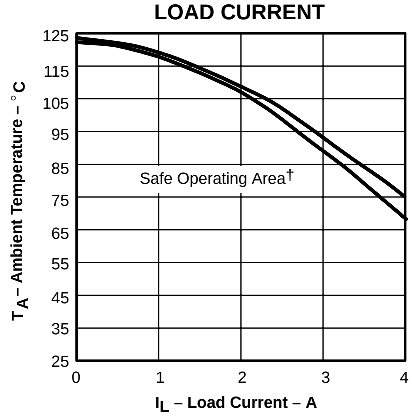


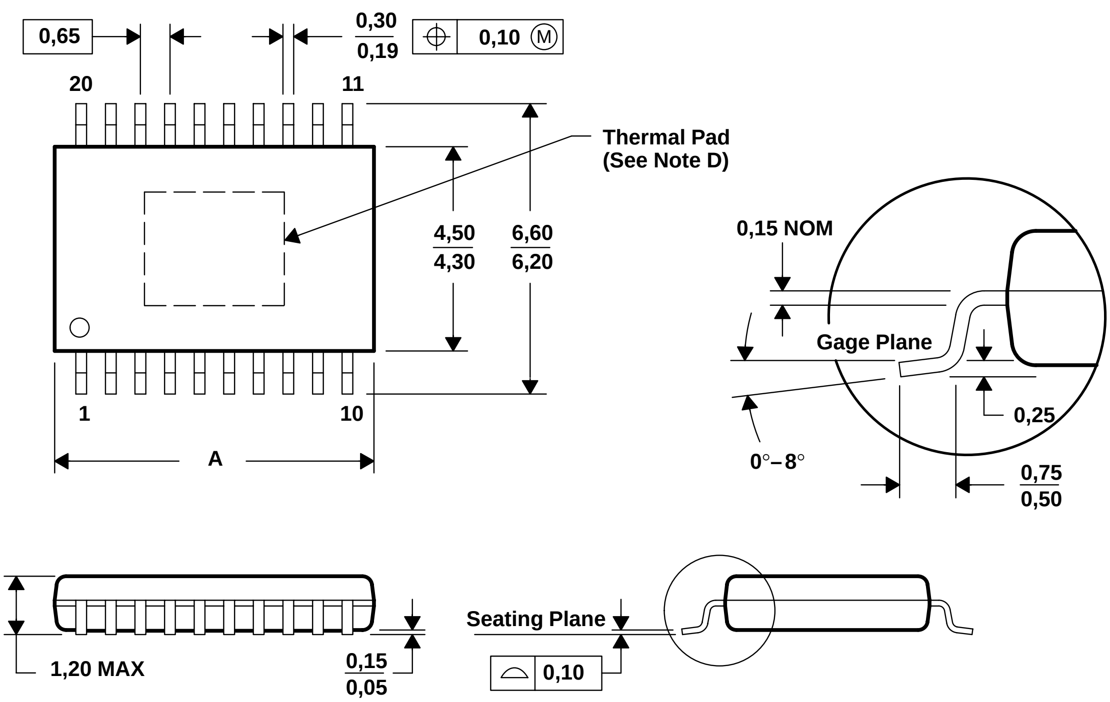
Figure 18

† Safe operating area is applicable to the test board conditions listed in the Dissipation Rating Table section of this data sheet.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



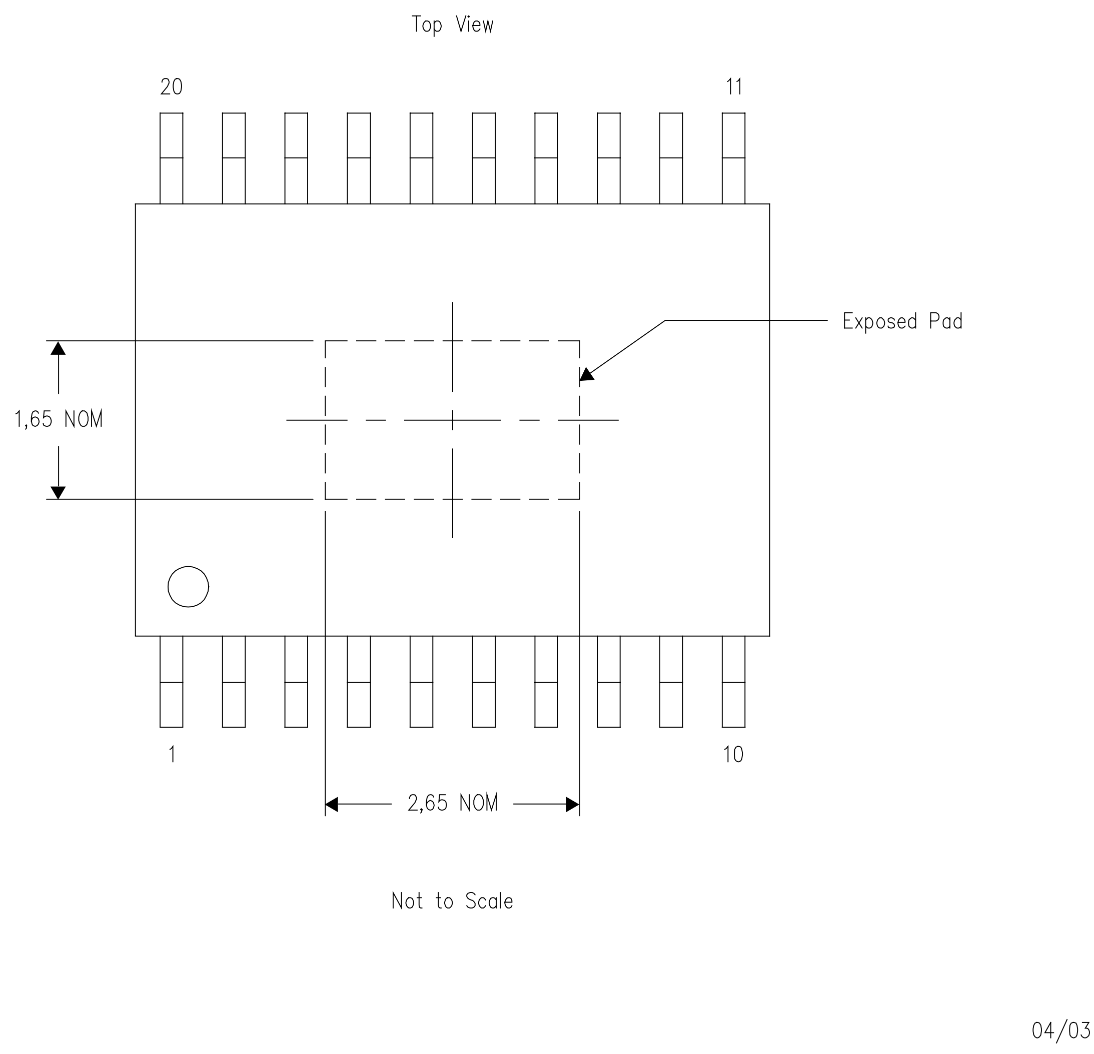
PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PWP (R-PDSO-G20) **PowerPAD™ PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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