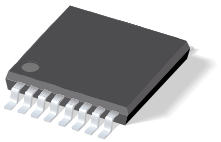


SLUS543A – DECEMBER 2002 – REVISED FEBRUARY 2003

WIDE-INPUT SYNCHRONOUS BUCK CONTROLLER

FEATURES

- **Operating Input Voltage 10 V to 55 V**
- **Input Voltage Feed-Forward Compensation**
- **0.5% Internal 0.7-V Reference**
- **Programmable Fixed-Frequency, Up to 1-MHz Voltage Mode Controller**
- **Internal Gate Drive Outputs for High-Side P-Channel and Synchronous N-Channel MOSFETs**
- **16-Pin PowerPAD™ Package (θ_{JC} = 2°C/W)**
- **Thermal Shutdown**
- **Externally Synchronizable**
- **Programmable High-Side Current Limit**
- **Programmable Closed-Loop Soft-Start**
- **TPS40060 Source Only/TPS40061 Source/Sink**

APPLICATIONS

- **Networking Equipment**
- **Telecom Equipment**
- **Base Stations**
- **Servers**

DESCRIPTION

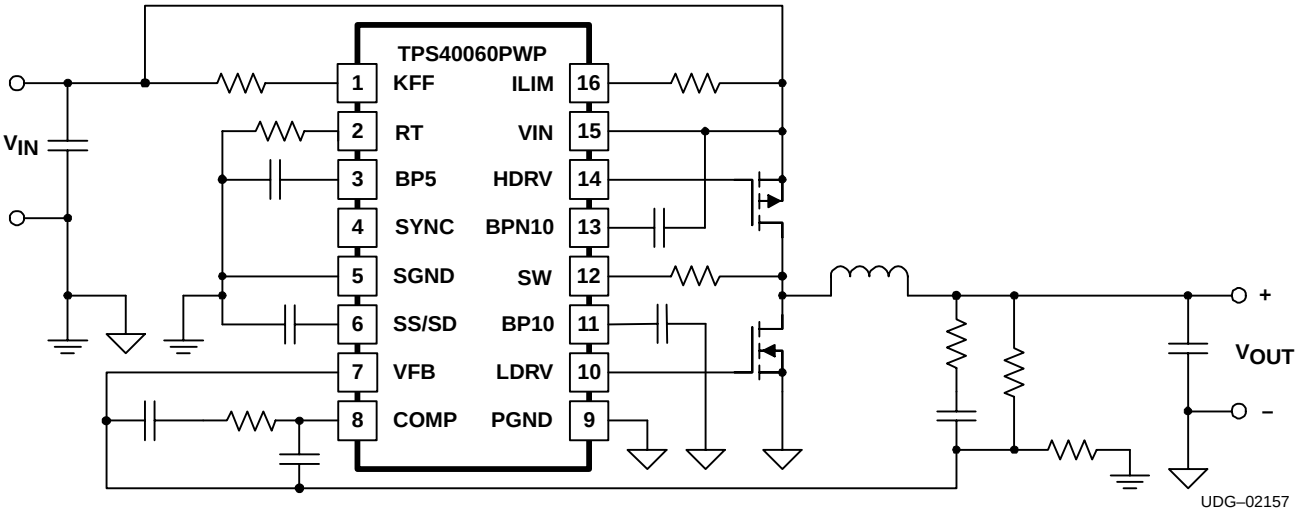
The TPS40060 and TPS40061 are high-voltage, wide input (10 V to 55 V) synchronous, step-down converters.

This family of devices offers design flexibility with a variety of user programmable functions, including; soft-start, UVLO, operating frequency, voltage feed-forward, high-side current limit, and loop compensation. These devices are also synchronizable to an external supply.

The TPS40060 and TPS40061 incorporate MOSFET gate drivers for external P-channel high-side and N-channel synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction.

For the TPS40061, the anti-cross conduction circuitry also allows the output to sink current by allowing the synchronous rectifier to turn on without the switch node (SW) first collapsing.

SIMPLIFIED APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD™ is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	LOAD CURRENT	PACKAGE(1)	PART NUMBER
–40°C to 85°C	SOURCE	Plastic HTSSOP (PWP)	TPS40060PWP
	SOURCE/SINK	Plastic HTSSOP (PWP)	TPS40061PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40060PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

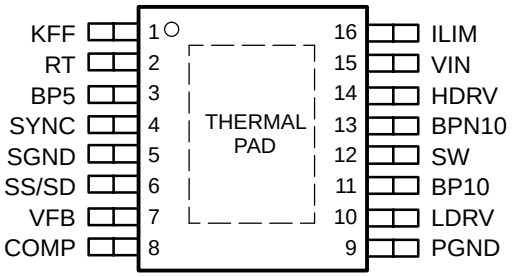
		TPS40060 TPS40061	UNIT
Input voltage range, VI	VIN	60	V
	VFB, KFF, SS/SD, SYNC	–0.3 to 6	
	SW	–0.3 to 60V or VIN+5 V (whichever is less)	
	SW. transient < 50 ns	–2.5 V	
Output voltage range, V_O	COMP, RT, KFF, SS	–0.3 to 6	
Output current, I_{OUT}	RT	200	µA
Operating junction temperature range, T_J		–40 to 125	°C
Storage temperature, T_{stg}		–55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	10		55	V
Operating free-air temperature, T_A	–40		85	°C

PWP PACKAGE(3)(4)
(TOP VIEW)



(3) For more information on the PWP package, refer to TI Technical Brief, Literature No. SLMA002.
(4) PowerPAD™ heat slug must be connected to SGND (Pin 5), or electrically isolated from all other pins.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 165 kΩ, R_{KFF} = 182 kΩ, f_{SW} = 300 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		10		55	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching		1.5	2.5	mA
5-V REFERENCE						
V_{BP5}	Input voltage		4.5	5.0	5.5	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Frequency		270	300	330	kHz
V_{RAMP}	PWM ramp voltage(1)			2		V
V_{IH}	High-level input voltage, SYNC		2			
V_{IL}	Low-level input voltage, SYNC				0.8	
I_{SYNC}	Input current, SYNC			5	10	µA
	Pulse width, SYNC	Pulse amplitude = 5 V	50			ns
V_{RT}	RT voltage		2.32	2.50	2.68	V
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW} ≤ 1 MHz	85%		98%	
	Minumum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.50	3.65	V
I_{KFF}	Feed-forward current operating range(1)		20		1100	µA
SOFT START						
I_{SS}	Soft-start source current		1.8	2.3	2.9	µA
V_{SS}	Soft-start clamp voltage		3.1	3.7	4.0	V
t_{DSCH}	Discharge time	C_{SS} = 220 pF	1.8	2.2	2.8	µs
t_{SS}	Soft-start time	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	120	155	190	
$V_{SS/SD}$		Shutdown outputs threshold voltage	90	120	145	mV
		Enable outputs threshold voltage	160	210	260	
10-V REFERENCE						
V_{BP10}	Input voltage		9.0	9.7	10.7	V
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage	T_A = 25°C	0.698	0.700	0.704	V
		0°C ≤ T_A ≤ 85°C	0.690	0.700	0.707	
			0.690	0.700	0.715	
G_{BW}	Gain bandwidth		3	5		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current	V_{COMP} = 2.0 V, V_{FB} = 0 V	1.5	4.0		mA
I_{OL}	Low-level output sink current	V_{COMP} = 2.0 V, V_{FB} = 1 V	2.5	4.0		
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	300	nA
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA, V_{FB} = 0 V	3.25	3.45	3.60	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA, V_{FB} = 1 V	0.050	0.215	0.350	

(1) Ensured by design. Not production tested.
(2) All parameters measured at zero power dissipation.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 165 kΩ, R_{KFF} = 182 kΩ, f_{SW} = 300 kHz (unless otherwise noted)

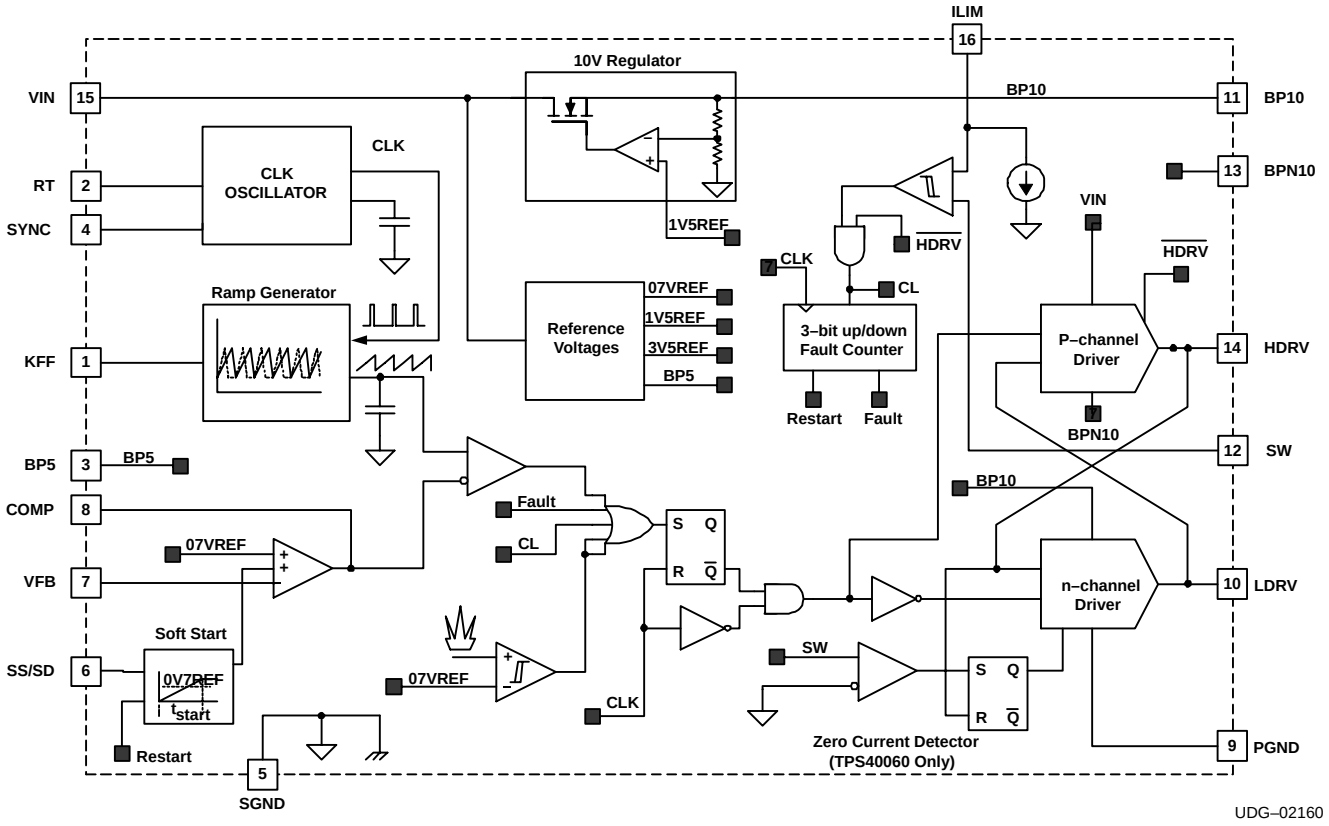
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8.3	10.0	11.5	µA
t_{DELAY}	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)		330	400	ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)		200	300	
t_{ON}	Switch leading-edge blanking pulse time(1)		100			
t_{OFF}	Off time during a fault			7		cycles
V_{OS}	Overcurrent comparator offset voltage		–175	–60	35	mV
OUTPUT DRIVER						
t_{HFALL}	High-side driver fall time(1)	C_{HDRV} = 2200 pF, (V_{IN} – V_{BPN10})		48	96	ns
t_{HRISE}	High-side driver rise time(1)	C_{HDRV} = 2200 pF, (V_{IN} – V_{BPN10})		36	72	
t_{LFALL}	Low-side driver fall time(1)	C_{LDRV} = 2200 pF, BP10		24	48	
t_{LRISE}	Low-side driver rise time(1)	C_{LDRV} = 2200 pF, BP10		48	96	
V_{OH}	High-level ouput voltage, HDRV	I_{HDRV} = 0.1 A , (V_{IN} – V_{HDRV})		1.0	1.4	V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A , (V_{HDRV} – V_{BPN10})			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = 0.1 A, (V_{BP10} – V_{LDRV})		1.0	1.5	
V_{OL}	Low-level ouput voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width			100	150	ns
BPN10 REGULATOR						
V_{BPN10}	Output voltage	Referenced to V_{IN}	–7.5	–8.5	–9.5	V
RECTIFIER ZERO CURRENT COMPARATOR (TPS40060 ONLY)						
V_{SW}	Switch voltage	LDRV output OFF	–6	0	6	mV
SW NODE						
I_{LEAK}	Leakage current(1)				1	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			25		
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold voltage, BP10	R_{KFF} = 10 kΩ	6.25	6.5	7.5	V
	Undervoltage lockout hysteresis			0.4		
V_{KFF}	KFF programmable threshold voltage	R_{KFF} = 82.5 kΩ	9	10	11	

(1) Ensured by design. Not production tested.
(2) All parameters measured at zero power dissipation.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BP5	3	O	5-V reference for the internal device logic only. This pin should be bypassed to ground with a 0.1-μF ceramic capacitor. **This pin is not for external use.**
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-μF ceramic capacitor. **This pin is not for external use.**
BPN10	13	O	Negative 8-V reference with respect to VIN. This voltage is used to provide gate drive for the high side P-channel MOSFET. This pin should be bypassed to VIN with a 0.1-μF capacitor
COMP	8	I	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The comp pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	14	O	Floating gate drive for the high-side P-channel MOSFET. This pin switches from VIN (MOSFET off) to BPN10 (MOSFET on).
ILIM	16	I	Current limit pin, used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VIN. The voltage on this pin is compared to the voltage drop (VIN –SW) across the high side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feed-forward. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	I	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9	–	Power ground reference for the device. There should be a low-impedance connection from this point to the source of the power MOSFET.
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator ramp charging current and switching frequency.
SGND	5	–	Signal ground reference for the device.
SS/SD	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 μA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin 1.6 V.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing. This pin is used for zero current sensing in the TPS40060.
SYNC	4	I	Syncronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency.
VFB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device.

SIMPLIFIED BLOCK DIAGRAM



UDG–02160

FUNCTIONAL DESCRIPTION

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40060 and TPS40061 have independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by equation (1) and the relationship is charted in Figure 2.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \right) (k\Omega) \quad (1)$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations since the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 1).

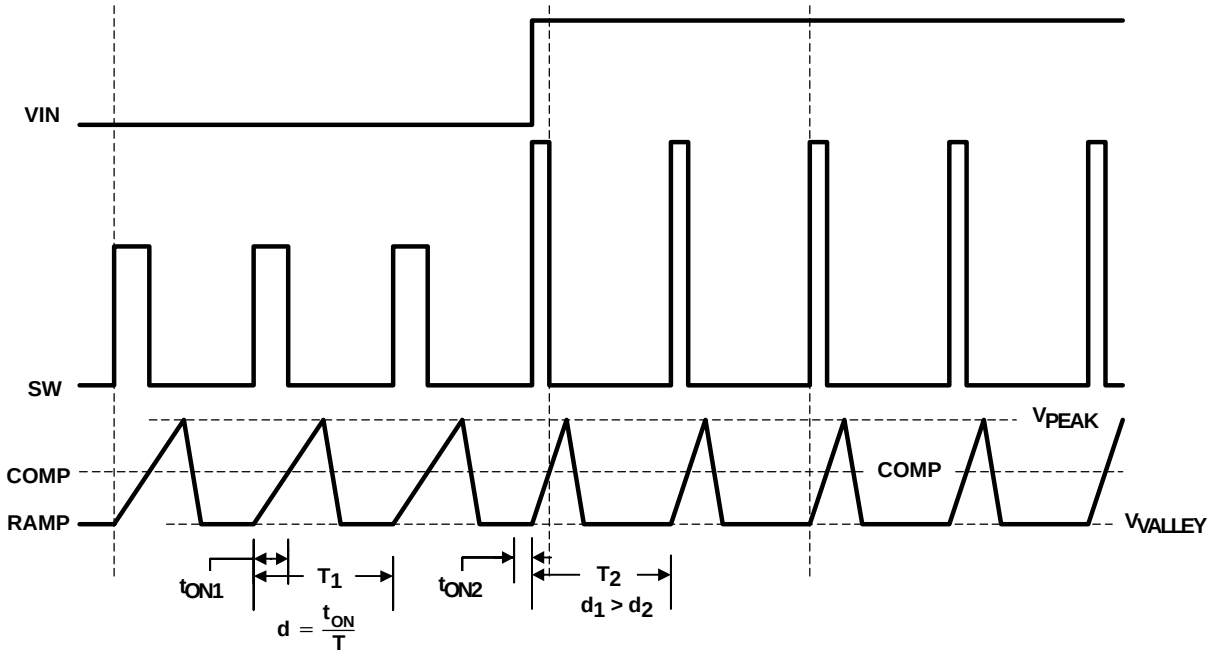


Figure 1. Voltage Feed-Forward Effect on PWM Duty Cycle

FUNCTIONAL DESCRIPTION

The PWM ramp must be faster than the master clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed via a single resistor (R_{KFF}) pulled up to VIN. R_{KFF} is related to R_T, and the minimum input voltage, $V_{IN(min)}$ through the following:

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(65.27 \times R_T + 1502\right)\ (\Omega) \quad (2)$$

where:

- V_{IN} is the desired start-up (UVLO) input voltage
- R_T is the timing resistance in kΩ

See the section on UVLO operation for further description.

The curve showing the feedforward impedance required for a given switching frequency, f_{SW}, at various input voltages is shown in Figure 3.

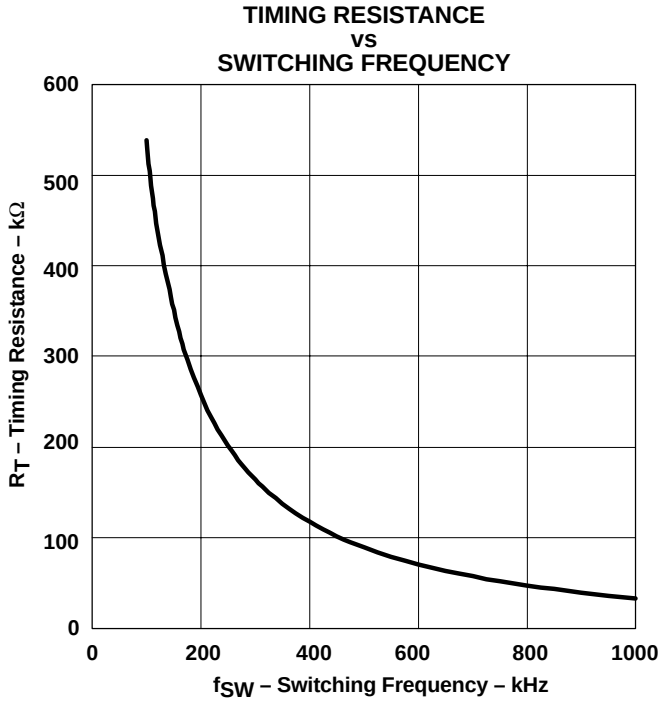


Figure 2

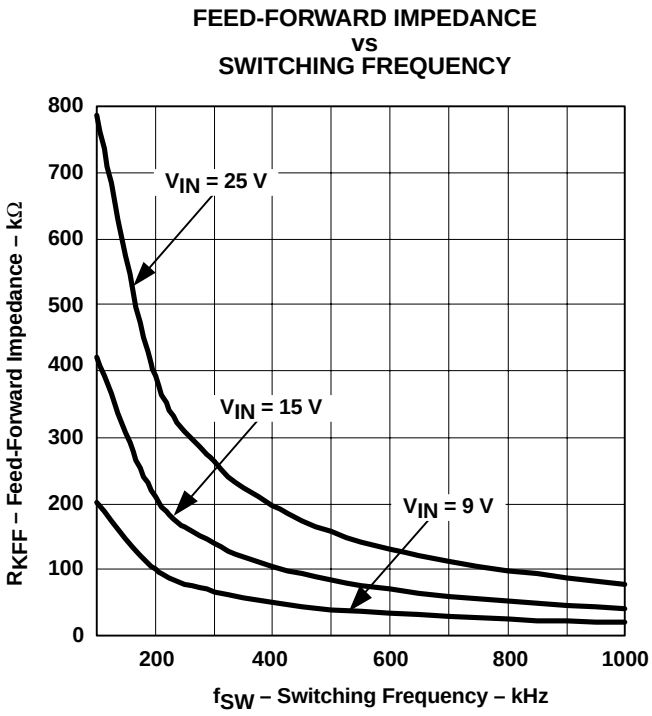


Figure 3

FUNCTIONAL DESCRIPTION

UVLO OPERATION

The TPS40060 and TPS40061 use both fixed and variable (user programmable) UVLO protection. The fixed UVLO monitors the BP10 and BP5 bypass voltages. The UVLO circuit holds the soft-start low until the BP5 and BP10 voltage rails have exceeded their thresholds and the input voltage has exceed the user programmable undervoltage threshold.

The TPS40060 and TPS40061 use the feed-forward pin, KFF, as a user programmable low-line UVLO detection. This variable low-line UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition existis if the device receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as descibed in equation (3):

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(65.27 \times R_T + 1502\right) \quad (\Omega) \tag{3}$$

where:.

- V_{IN} is the desired start-up (UVLO) input voltage

The variable UVLO function utilizes a three–bit full adder to prevent spurious shut-downs or turn-ons due to spikes or fast line transients. When the adder reaches a total of seven counts in which the ramp duration is shorter the clock cycle a powergood signal is asserted, a soft-start initiated, and the upper and lower MOSFETs are turned off.

Once the soft-start is initiated, the UVLO cicruit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared (See Figure 4).

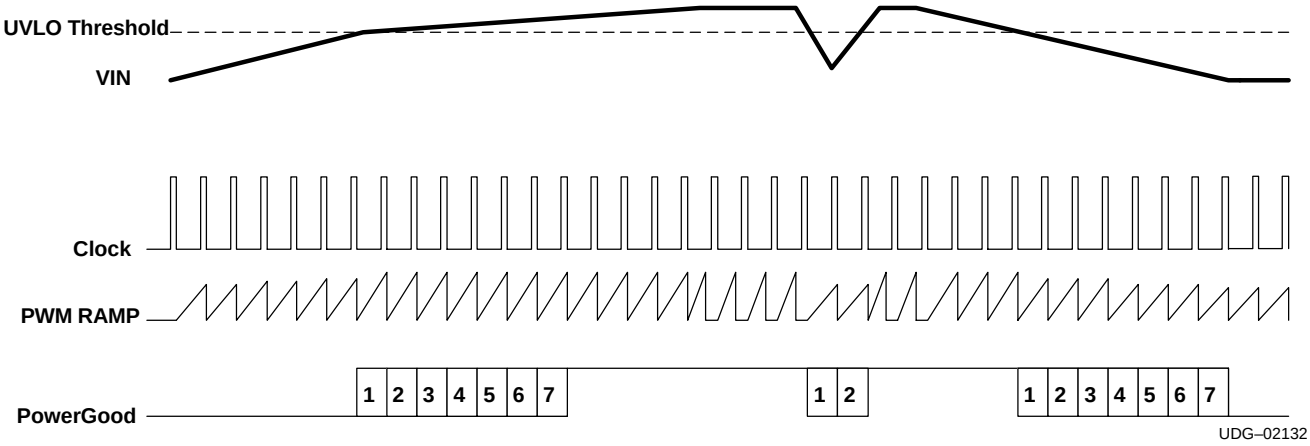


Figure 4. Undervoltage Lockout Operation

Some applications may require an additional circuit to prevent false restarts at the UVLO voltage level. such as systems which have high impedance on the input voltage line or which have excessive ringing on the V_{IN} line. The input voltage impedance can cause the input voltage to sag enought at startup to cause a UVLO shutdown and subsequent restart. A simple external circuit provides a selectable amount of hysteresis to prevent a nuisance UVLO shutdown.

Assuming a hysteresis current of 10% of I_{KFF}, and the peak detector charges to 8 V and $V_{IN(min)}$ = 18 V, the value of R_A is calculated in the following equation.

$$R_A = \frac{R_{KFF} \times (8 - 3.5)}{0.1 \times \left(V_{IN(min)} - 3.5\right)} = 565\ k\Omega,\ \approx 562\ k\Omega \tag{4}$$

The value of CA is chosen to keep the peak voltage high enough between switching cycles. To keep the capacitor charge from drooping by 0.1 V, (in this case from 8.0 V to 7.9 V), use the following equation.

$$C_A = \frac{(8 - 3.5)}{\left(R_A \times 7.9 \times f_{SW}\right)} \quad (5)$$

The value of CA may calculate to less that 10 pF, but some standard value up to 470 pF allows the design to work correctly. This design can use a small signal switching diode or a Schottky rated for more than 20 V. Figure 5 shows a typical implementation.

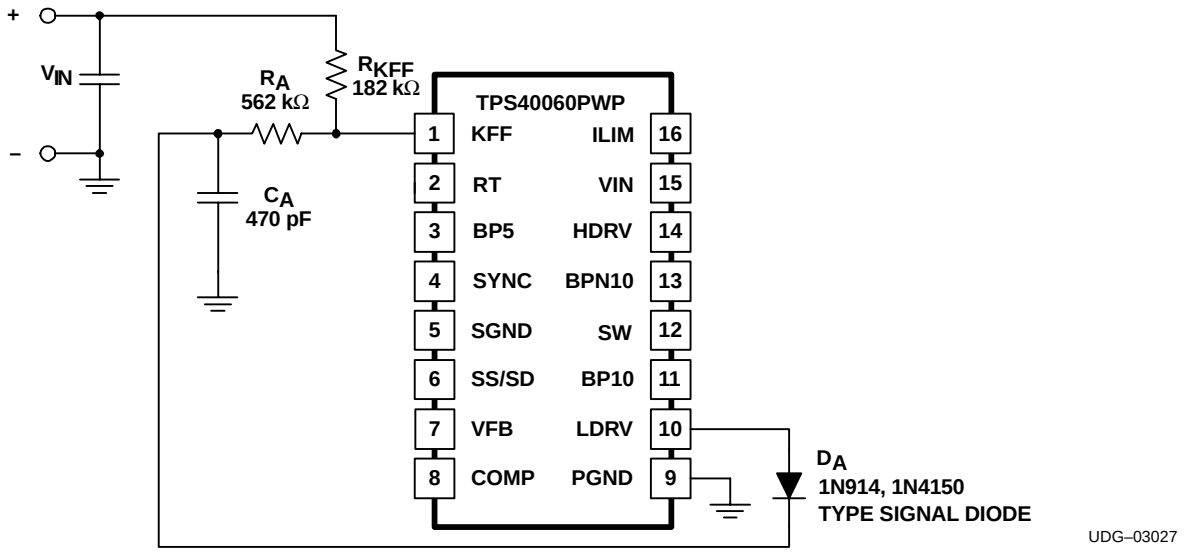


Figure 5. Hysteresis for Programmable Undervoltage Lockout

SOFT-START

The soft-start circuit produces a closed-loop controlled ramp up of the output voltage. The duration of the soft-start is programmable through a single capacitor connected to the SS/SD pin. Closed loop control is provided by feeding the soft-start ramp into a second non-inverting input to the error amplifier, the internal 0.7-V reference is connected to the first non-inverting input. The error amplifier regulates on the lowest non-inverting input voltage. The external soft-start capacitor is charged by an internal current source of 2.3-μA nominal. The output voltage ramps up when the voltage on the SS/SD pin ramps between 0.8 V and 1.5 V and:

$$t_{SS} = 0.304 \times C_{SS} \text{ (s)} \quad (6)$$

where

- CSS is in μF

There is a time delay equal to t_{SS} from the application of power until the start of the soft-start ramp.

For applications in which the V_{IN} supply ramps up slowly, (typically about 50 ms) it may be necessary to increase the soft-start time to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN} supply transitions between 6 V and 7 V.

ENABLE

If the voltage on the SS/SD pin is pulled to less than 0.2 V, the output becomes disabled. An open drain MOSFET is well suited to implement this feature.

FUNCTIONAL DESCRIPTION

PROGRAMMING CURRENT LIMIT

This device uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven low. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 6 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{LIM}) depends on t_{START}, C_O, V_O, and the load current at turn-on (I_L).

$$I_{LIM} = \left[\frac{\left(C_O \times V_O\right)}{t_{SS}} \right] + I_L \quad (A) \tag{7}$$

The current limit programming resistor (R_{ILIM}) is calculated using equation (8).

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]}}{1.12 \times I_{SINK}} + \frac{V_{OS}}{I_{SINK}} \quad (\Omega) \tag{8}$$

where:

- I_{SINK} is the current into the ILIM pin and is nominally 10 μA
- I_{OC} is the overcurrent setpoint which is the DC output current plus one-half of the peak inductor current
- V_{OS} is the overcurrent comparator offset and is nominally –95 mV

FUNCTIONAL DESCRIPTION

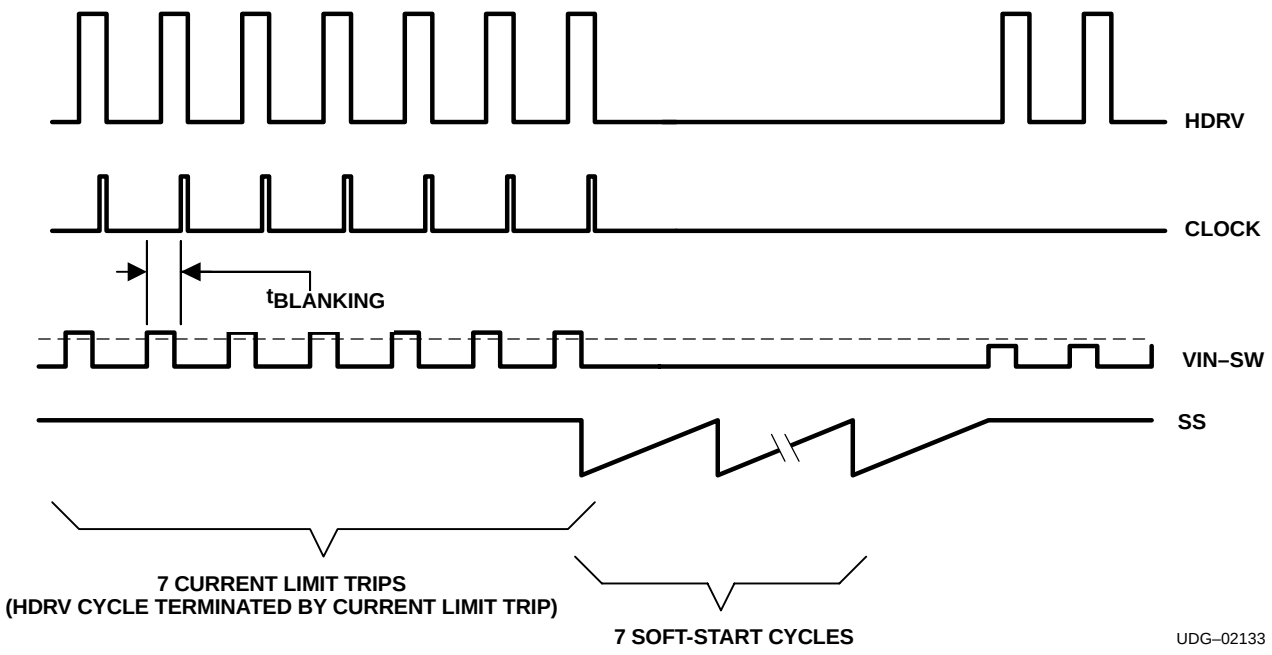


Figure 6. Typical Current Limit Protection Waveforms

CALCULATING THE BPN10 AN BP10V BYPASS CAPACITOR

The BPN10 capacitance provides a local, low impedance source for the high-side driver. The BPN10 capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BPN10 capacitance is described in the following equation.

$$C_{BPN10} = \frac{Q_g}{\Delta V} \quad (F) \tag{9}$$

The 10-V reference pin, BP10V needs to provide energy for the synchronous MOSFET gate drive via the BP10V capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in the following equation.

$$C_{BP10V} = \frac{Q_{gSR}}{\Delta V} \quad (F) \tag{10}$$

SYNCHRONIZING TO AN EXTERNAL SUPPLY

The TPS40060 and TPS40061 can be synchronized to an external clock through the SYNC pin. The device must be synchronized at a frequency 20% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the device to freely run at the frequency programmed by R_T.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency.

APPLICATION INFORMATION

SELECTING THE INDUCTOR VALUE

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. Too small an inductance results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter doesn't enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in the following equation.

$$L = \frac{\left(V_{IN} - V_O\right) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad (H) \tag{11}$$

where:.

- V_O is the output voltage
- ΔI is the peak-to-peak inductor current

CALCULATING THE OUTPUT CAPACITANCE

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst case output ripple is described in the following equation.

$$\Delta V = \Delta I \left[ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right] \quad \left(V_{P-P}\right) \tag{12}$$

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy-to-light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in the following equation.

$$E_L = \frac{1}{2} \times L \times I^2 \quad (J) \tag{13}$$

where:

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left((Amperes)^2 \right) \tag{14}$$

where:

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions

APPLICATION INFORMATION

Energy in the capacitor is given by the following equation:

$$E_C = \frac{1}{2} \times C \times V^2 \quad (J) \tag{15}$$

where:

$$V^2 = \left(V_f\right)^2 - \left(V_i\right)^2 \quad \left(Volts^2\right) \tag{16}$$

where:

- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage

By substituting equation (14) into equation (13), substituting equation (16) into equation (15), setting equation (13) equal to equation (15) and solving for C_O yields the following equation.

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2\right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2\right]} \quad (F) \tag{17}$$

CALCULATING THE INPUT CAPACITANCE

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this standalone supply, onboard capacitance is added to handle input voltage ripple and RMS current considerations. For this power level, input voltage ripple of 150-mV is reasonable, and a conservative minimum capacitance value is calculated in the following equation.

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{10\ A \times 2.5\ \mu s}{0.15\ V} = 167\ \mu F \tag{18}$$

In addition to this minimum capacitance requirement, the RMS current stresses must be considered. Equation (19) is the simplified formula that calculates the RMS current for a trapazoidal current waveform, and for a 24-V input and 2.5-V output at 10 A.

$$I_{RMS} = I \times \sqrt{D} = I \times \sqrt{\frac{V_{OUT}}{V_{IN\ (min)}}} = 10\ A \times \sqrt{\frac{2.5\ V}{24\ V}} = 3.23\ A \tag{19}$$

Additional terms for the ripple component of the current add only a small amount to the total RMS current, and can be neglected. To meet this initial requirement with small size and cost, a combination of capacitors is considered. To carry the high-frequency ripple current, two or three 10-µF, X5R ceramic capacitors are placed close to the power circuitry. These capacitors have an extremely low ESR and the datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz, so two or three of these ceramic capacitors will suffice.

APPLICATION INFORMATION

LOOP COMPENSATION

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS40060 and TPS40061 use voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The modulator gain is described in Figure 7, with V_{IN} being the minimum input voltage required to cause the ramp excursion to cover the entire switching period.

$$A_{MOD} = \frac{V_{IN}}{V_S} \quad \text{or} \quad A_{MOD(db)} = 20 \times \log\left(\frac{V_{IN}}{V_S}\right) \tag{20}$$

Duty dycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage,

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S}$$

Calculate the Poles and Zeros

For a buck converter using voltage mode control there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in equation (21).

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hz)} \tag{21}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in equation (22).

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hz)} \tag{22}$$

The Bode plot for the open-loop control voltage to output voltage gain, V_C to V_O, for a buck converter with voltage feed-forward control operating in continuous mode is shown in Figure 8.

The maximum crossover frequency (0 dB loop gain) is calculated in equation (23).

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hz)} \tag{23}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (–40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade).

Figure 8 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

APPLICATION INFORMATION

A Type III topology, shown in Figure 9, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 10. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies.

PWM MODULATOR RELATIONSHIPS

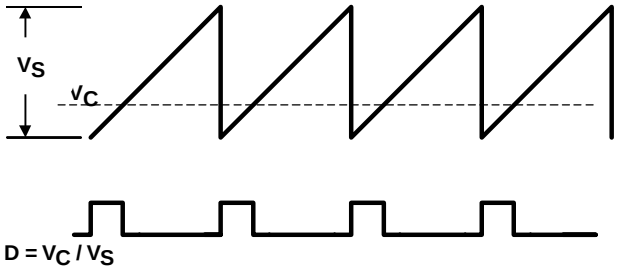


Figure 7

MODULATOR GAIN vs SWITCHING FREQUENCY

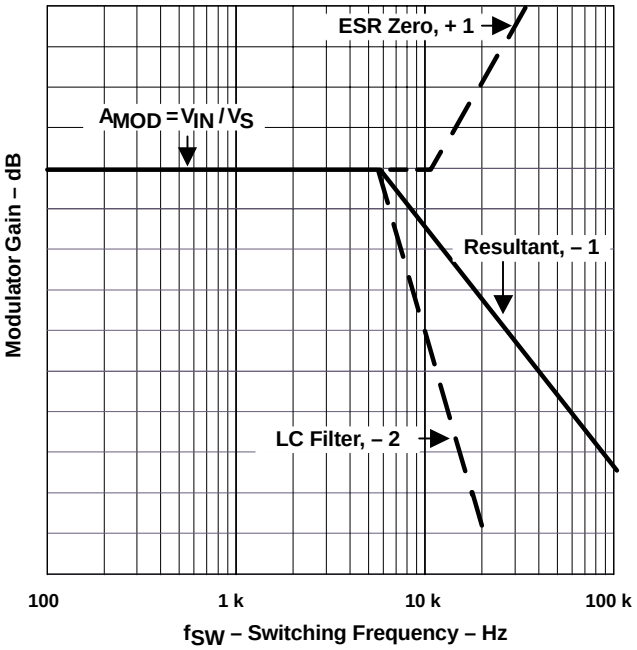


Figure 8

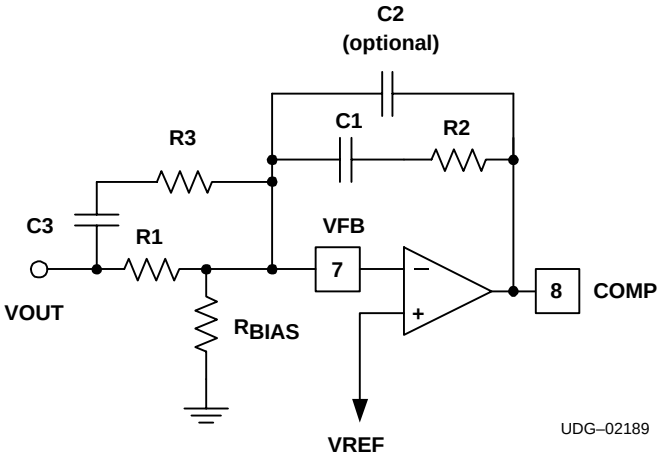


Figure 9. Type III Compensation Configuration

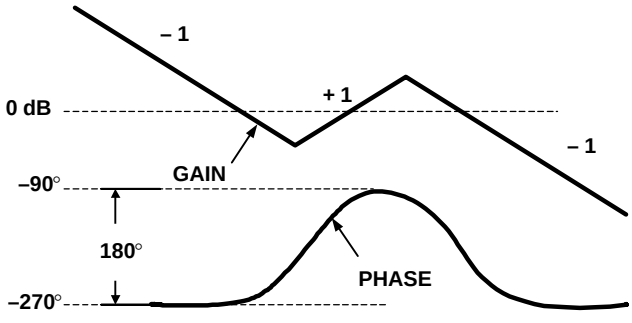


Figure 10. Type III Compensation Gain and Phase

APPLICATION INFORMATION

The poles and zeros for a type III network are described in equations (24).

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \text{ (Hz)} \qquad f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \text{ (Hz)}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \text{ (Hz)} \qquad f_{P2} = \frac{1}{2\pi \times R3 \times C3} \text{ (Hz)} \tag{24}$$

The unity gain frequency is described in equation (25)

$$f_C = \frac{1}{2\pi \times R1 \times C2} \text{ (Hz)} \tag{25}$$

The double zeros, f_{Z1} and f_{Z2} and the double poles, f_{P1} and f_{P2} are chosen from Venable's *The K Factor*[1], which states:

$$f_{Z1} = f_{Z2} = \frac{f_C}{\sqrt{K}} \quad \text{and} \quad f_{P1} = f_{P2} = f_C \times \sqrt{K} \tag{26}$$

To determine the factor K, the phase boost must be calculated knowing the desired phase margin, M, and the modulator phase shift, P, at the unity gain frequency, f_C. In addition, Boost = M–P–90. It is best to measure P, but typical values range from –140° to –170°. Then the value of K is calculated from:

$$K = \left(\text{Tan}\left(\frac{\text{Boost}}{4} + 45^{o}\right)\right)^2 \tag{27}$$

Calculate the value of R_{BIAS} to set the output voltage, V_{OUT}.

$$R_{BIAS} = \frac{0.7 \times R1}{V_{OUT} - 0.7} \tag{28}$$

Error Amplifier Minimum Load Resistance

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current which must be considered when sizing R2. Too small a value does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\ (max)}}{I_{SOURCE\ (min)}} (\Omega) = \frac{3.45\ V}{2.0\ mA} = 1.725\ k\Omega \tag{29}$$

dv/dt INDUCED TURN-ON

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore the SR MOSFET should be chosen so that the C_{GD} capacitance is smaller than the C_{GS} capacitance. A 2-Ω to 5-Ω resistor in the upper MOSFET gate lead shapes the turn-on and dv/dt of the SW node and helps reduce the induced turn-on.

APPLICATION INFORMATION

HIGH-SIDE MOSFET POWER DISSIPATION

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by equation (30).

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25^{\circ}C\right]\right) \quad (W) \tag{30}$$

where:

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$

The TC_R varies depending on MOSFET technology and manufacturer but is typically ranges between 0.0035 ppm/°C and 0.010 ppm/°C.

The I_{RMS} current for the high side MOSFET is described in equation (31).

$$I_{RMS} = I_O \times \sqrt{d} \quad \left(Amperes_{RMS}\right) \tag{31}$$

For the high-side MOSFET the switching losses are descibed in equation (32).

$$P_{SW(fsw)} = V_{IN} \times \left(\frac{I_{D1} \times ts1}{6} + \frac{I_{D2} \times ts2}{2}\right) \times f_{SW} \tag{32}$$

where:

- I_{D1} and I_{D2} are the current magnitudes at the instance of MOSFET switching (See Figure 11)

I_{D1} and I_{D2} are a function of the inductor value and load current. The inductance value is usually selected so that the converter remains in continuous mode of operation until approximately 10% to 30% of the typical load is acheived. The change in inductor current is described in equation (33).

$$\Delta I = 2 \times I_{O\,(dis)} \quad (A) \tag{33}$$

where:

- $I_{O\,(dis)}$ is the load current when the converter enters discontinuous mode of operation.

I_{D1} and I_{D2} can be calculated from equations (34).

$$I_{D1} = I_O - \left(\frac{\Delta I}{2}\right) \quad \text{and} \quad I_{D2} = I_O + \left(\frac{\Delta I}{2}\right) \quad (A) \tag{34}$$

where:

- ΔI is the inductor ripple current. (See Figure 11)

The converter enters discontinuous mode when the DC output current is one-half the inductor ripple current. Refer to *Selecting the Inductor Value* section, equation (11) for more information.

The transition times, ts1 and ts2, are a function of the external MOSFETS selected.

APPLICATION INFORMATION

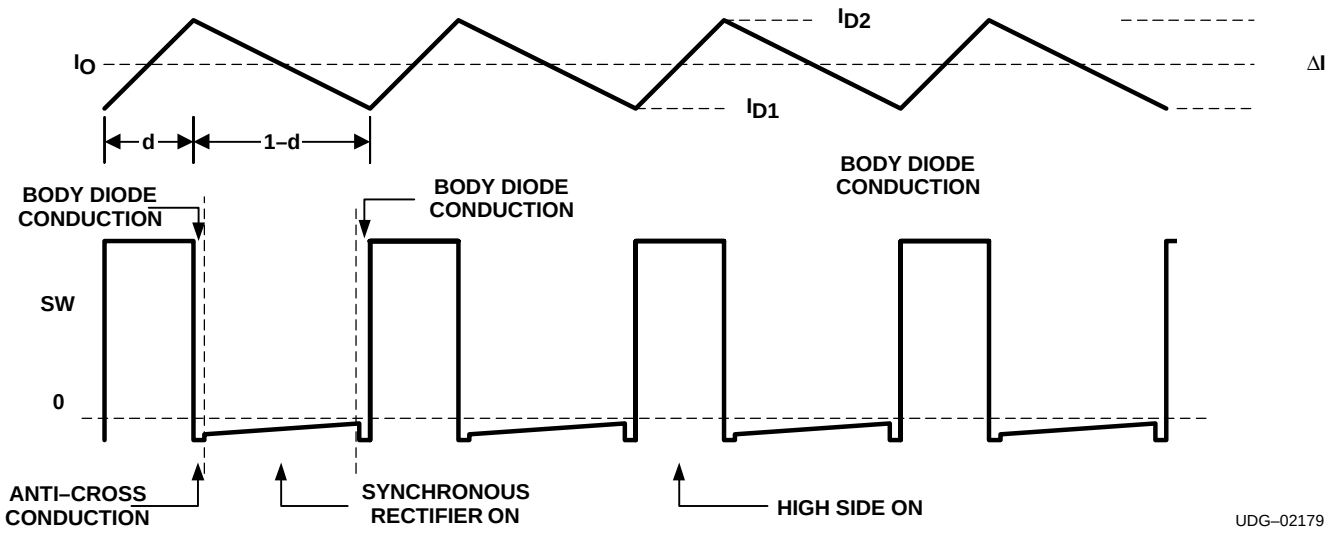


Figure 11. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by the following equation.

$$P_T = \frac{\left(T_J - T_A\right)}{\theta_{JA}} \quad (W) \tag{35}$$

where:

$$P_T = P_{COND} + P_{SW(fsw)} \quad (W) \tag{36}$$

and θ_{JA} is the package thermal impedance.

SYNCHRONOUS RECTIFIER MOSFET POWER DISSIPATION

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be found using equation (30) and the RMS current through the synchronous rectifier MOSFET is described in equation (37).

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad \left(A_{RMS}\right) \tag{37}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti-cross conduction delay time. The body diode conduction losses are described by equation (38).

$$P_{DC} = I_O \times V_F \times t_{DELAY} \times f_{SW} \quad (W) \tag{38}$$

where:

- V_F is the body diode forward voltage
- t_{DELAY} is the total delay time per switching period

APPLICATION INFORMATION

The reverse recovery losses are due to the time it takes for the body diode to recovery from a forward bias to a reverse blocking state. The reverse recovery losses are described in equation (39).

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad (W) \tag{39}$$

where:

- Q_{RR} is the reverse recovery charge of the body diode

The total synchronous rectifier MOSFET power dissipation is described in equation (40).

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad (W) \tag{40}$$

TPS40060/TPS40061 POWER DISSIPATION

The power dissipation in the TPS40060 and TPS40061 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance, refer to [2] can be calculated from equation (41).

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad (W) \tag{41}$$

And the total power dissipation in the device, assuming MOSFETs with similar gate charges for both the high-side and synchronous rectifier is described in equation (42).

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad (W) \tag{42}$$

or

$$P_T = \left[\left(2 \times Q_g \times f_{SW}\right) + I_Q\right] \times V_{IN} \quad (W) \tag{43}$$

where:

- I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the device's PowerPad package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow.

θ_{JA} = 36.51°C/W

The maximum allowable package power dissipation is related to ambient temperature by equation (35). Substituting equation (35) into equation (43) and solving for f_{SW} yields the maximum operating frequency for the TPS40060 and TPS40061. The result is:

$$f_{SW} = \frac{\left(\left[\frac{\left(T_J - T_A\right)}{\left(\theta_{JA} \times V_{DD}\right)}\right] - I_Q\right)}{\left(2 \times Q_g\right)} \quad (Hz) \tag{44}$$

LAYOUT CONSIDERATIONS

THE POWERPAD™ PACKAGE

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. For maximum thermal performance, the circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the area is 5 mm x 3.4 mm [3].

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD Thermally Enhanced Package*[3] for more information on the PowerPAD package.

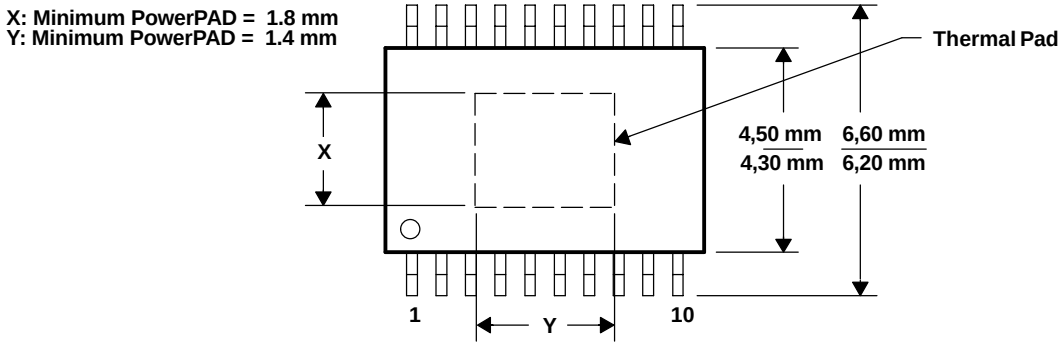


Figure 12. PowerPAD Dimensions

MOSFET PACKAGING

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G–10/FR–4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

GROUNDING AND CIRCUIT LAYOUT CONSIDERATIONS

The device provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10, BP5, and BPN10) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BPN10, and the switch node (SW).

DESIGN EXAMPLE

- Input voltage: 18 V_{DC} to 55 V_{DC}
- Output voltage: 3.3 V ±2%
- Output current: 5 A (maximum, steady-state), 7 A (surge, 10-ms duration, 10% duty cycle maximum)
- Output ripple: 33 mV_{P-P} at 5 A
- Output load response: 0.3 V => 10% to 90% step load change
- Operating temperature: –40°C to 85°C
- f_{SW} = 300 kHz

1. Calculate maximum and minimum duty cycles

$$d_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = 0.0588 \quad d_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = 0.187 \tag{45}$$

2. Select I

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 2.0 \text{ A} \tag{46}$$

3. Calculate the power losses in the high side MOSFET (Si9407AEY) at 48-V input

$$d48V = \frac{V_O}{V_{IN}} = 0.069 \tag{47}$$

from (31)

$$I_{RMS} = I_O \times \sqrt{d} = 5 \times \sqrt{0.069} = 1.31 \text{ A} \tag{48}$$

substituting (48) into (30) yields

$$P_{COND} = I_{RMS}{}^2 \times R_{DS(on)} \times \left(1 + T_{CR} \times \left[T_J - 25°C\right]\right) \tag{49}$$

$$= 1.31^2 \times 0.12 \times (1 + 0.007 \times (150 - 25)) = 0.386 \text{ W}$$

from (34)

$$I_{D1} = I_O - \frac{\Delta I}{2} = 5 - 1.0 = 4.0 \text{ A} \quad I_{D2} = I_O + \frac{\Delta I}{2} = 5 + 1.0 = 6.0 \text{ A} \tag{50}$$

t_{S1} (rise time) and t_{S2} (fall time) is approximated from the Gate Charge Characteristics graph on the MOSFET data sheet.

Let Q2–Q1 equal the charge required to increase the gate voltage to its plateau voltage (V_{PLT}). The equivalent input capacitance during this period is:

$$C_{IN} = \frac{dQ}{dV} = \frac{5 \text{ nC}}{4.5 \text{ V}} = 1111 \text{ pF} \tag{51}$$

DESIGN EXAMPLE

The time required to charge the equivalent capacitance is:

$$4.5 = 10 - (10 - 2) \times e^{\left(\frac{-t}{R \times C}\right)} \quad (52)$$

where R is the effective gate drive resistance of 10 Ω.

$$t_1 = -10 \times 1111\ pF \times \ln\left(\frac{5.5}{8}\right) = 4.2\ ns \quad (53)$$

The time it takes the drain-source voltage V_{DS} to fall is calculated in the datasheet. During this time, the change in charge occurs when V_{GS} is constant at the Miller charging voltage, 3.1 V:

$$\Delta Q = Q3 - Q2 = 2\ nC \quad (54)$$

During this period of time V_{GS} is held constant. Therefore the MOSFET gate drive looks like a constant current source with a current of:

$$I_{DRV} = \frac{V_{DRV} - V_{GS}}{R_{DRV}} = \frac{8 - 3.1}{10} = 490\ mA \quad (55)$$

The time it takes for V_{DS} to fall is calculated:

$$t_2 = \frac{\Delta Q}{I_{DRV}} = \frac{2.0\ nC}{0.490\ A} = 4.1\ ns \quad (56)$$

The total rise time is :

$$t_{S1} = t_R = t_I + t_2 = 4.2\ ns + 4.1\ ns = 8.3\ ns \quad (57)$$

Similarly, the fall time can be found from:

$$t_3 = (Q3 - Q2) \times \frac{R_{DRV}}{V_{PLT}} = 2.0\ nC \times \frac{7.5\ \Omega}{3.1\ V} = 4.8\ ns \quad (58)$$

$$t_4 = -R_{DRV} \times C_{IN} \times \ln\left(\frac{3.1}{8}\right) = 8.0\ ns \quad (59)$$

The total fall time is:

$$t_{S2} = t_F = t_3 + t_4 = 4.8\ ns + 8\ ns = 12.8\ ns \quad (60)$$

Substituting t_{S1}, t_{S2}, I_{D1} and I_{D2} into (32) yields:

$$P_{SW}(f_{SW}) = 48 \times \left(\frac{8.3\ ns \times 4.0}{6} + \frac{12.6\ ns \times 6.0}{2}\right) \times 300\ kHz = 477\ mW \quad (61)$$

The MOSFET junction temperature can be found by rearranging (35) and substituting (36).

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A$$

DESIGN EXAMPLE

4. Calculate Synchronous Rectifier Losses

The synchronous rectifier MOSFET has two loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from (37)

$$I_{RMS} = I_O \times \sqrt{1 - d} = 5 \times \sqrt{1 - 0.069} = 4.82\ A_{RMS} \quad (62)$$

The synchronous MOSFET conduction loss from (30) is:

$$P_{COND} = {I_{RMS}}^2 \times R_{DS(on)} \times \left(1 + T_{CR} \times \left[T_J - 25^{\circ}C\right]\right) \quad (63)$$

$$= 4.82^2 \times 0.011 \times (1 + 0.007(150 - 25)) = 0.48\ W$$

The body diode conduction loss from (38) is:

$$P_{DC} = I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 5.0 \times 0.8 \times 100\ ns \times 300\ kHz = 0.120\ W \quad (64)$$

The body diode reverse recovery loss from (39) is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{DD} \times f_{SW} = 0.5 \times 30\ nC \times 48 \times 300\ kHz = 0.216\ W \quad (65)$$

The total power dissipated in the synchronous rectifier MOSFET from (40) is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.216 + 0.48 + 0.12 = 0.816\ W \quad (66)$$

The junction temperature of the synchronous rectifier is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (0.816) \times 40 + 85 = 118^{o}C \quad (67)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

5. Calculate the Inductor Value

The inductor value is calculated from (11)

$$L = \frac{(48 - 3.3) \times 3.3}{48 \times 1.0 \times 300\ kHz} = 10.2\ \mu H \quad (68)$$

A standard inductor value of 10-µH is chosen.

6. Setting the switching frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be derived from the following equation, with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82\ E - 06} - 23\right) k\Omega = 164\ k\Omega, \quad \text{use } 165\ k\Omega \quad (69)$$

7. Programming the Ramp Generator Circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 14.4V (20% below the 18 $V_{IN(min)}$, R_{KFF} is calculated in the following equation.

$$R_{KFF} = \left(V_{IN(min)} - 3.5\right)\left(65.27 \times R_T + 1502\right)\ \Omega = 133.7\ k\Omega, \text{ use } 133\ k\Omega \quad (70)$$

DESIGN EXAMPLE

8. Calculating the Output Capacitance (C_O)

In this example. the output capacitance is determined by the load response requirement of $\Delta V = 0.3$ V for a 1 A to 5 A step load. C_O can be calculated using (17).

$$C_O = \frac{10\ \mu H \times \left(5^2 - 1^2\right)}{\left(3.3^2 - 3.0^2\right)} = 127\ \mu F \tag{71}$$

Using equation (12) calculate the ESR required to meet the output ripple requirements.

$$33\ mV = 2.0\left(ESR + \frac{1}{8 \times 127\ \mu F \times 300\ kHz}\right) \tag{72}$$

$ESR = 14.9\ m\Omega$

In order to get the required ESR, the capacitance needs to be greater than the 127-µF calculated. For example, a single Panasonic SP capacitor, 180-µF with ESR of 12 mΩ can be used. Re-calculating the ESR required with the new value of 180-µF is shown in equation (73).

$$33\ mV = 2.0\left(ESR + \frac{1}{8 \times 180\ \mu F \times 300\ kHz}\right) \tag{73}$$

$ESR = 16.5\ m\Omega$

9. Calculate the Soft-Start Capacitor (C_{SS})

This design requires a soft-start time (t_{START}) of 1 ms. C_{SS} is calculated in the following equation.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times 1\ ms = 3.28\ nF = 3300\ pF \tag{74}$$

10. Calculate the Current Limit Resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O, C_O and I_{LOAD} at start up as shown in equation (7).

$$I_{LIM} > \frac{180\ \mu F \times 3.3}{1\ m} + 7.0 = 7.6\ A \tag{75}$$

Set I_{LIM} for 10.0 A minimum, then from equation (8)

$$R_{ILIM} = \frac{10 \times 0.14}{1.12 \times 10.0\ \mu A} + \frac{V_{OS}}{I_{SINK}}\ \Omega = \frac{10 \times 0.14}{1.12 \times 10.0\ \mu A} + \frac{(-60\ mV)}{10\ mA}\ \Omega = 119\ k\Omega = 118\ k\Omega \tag{76}$$

DESIGN EXAMPLE

11. Calculate Loop Compensation Values

Calculate the voltage feed forward constant (K) from (20)

$$A_{MOD} = \frac{10}{2} = 5 \quad (77)$$

$$A_{MOD(dB)} = 20 \times \log(5.0) = 14\ dB \quad (78)$$

Calculate the output poles and zeros from (21) and (22) of the L-C filter.

$$f_{LC} = \frac{1}{2\pi\sqrt{10\ \mu H \times 180\ \mu F}} = 3.7\ kHz \quad (79)$$

and

$$f_Z = \frac{1}{2\pi \times 0.012 \times 180\ \mu F} = 74\ kHz \quad (80)$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 20 kHz.

Select the double zero location for the Type III compensation network. The location for the pole-zero placement according to [1] is determined by the phase boost required at crossover. For this example a 60° phase margin is desired. The required phase boost for this example is:

$$Boost = M - P - 90^o = 60^o - (-145^o) - 90^o = 115^o \quad (81)$$

where,

- M is the desired phase margin
- P is the modulator phase shift (–145° for this example)

$$K = \left(Tan\left(\frac{115^o}{4} + 45^o\right)\right)^2 \approx 11.77 \text{ and } \sqrt{K} = 3.43 \quad (82)$$

so,

$$f_{P1} = f_{P2} = \sqrt{K} \times 20\ kHz = 69\ kHz \text{ and } f_{Z1} = f_{Z2} = \frac{1}{\sqrt{K}} \times 20\ kHz = 5.8\ kHz$$

Following [1] the double zero is placed at ≅ 5.8 kHz, and the double pole is placed at 69 kHz. Equations (24), (25) and (28) can be solved for the component values in Figure 9. Select R1 = 100 kΩ.

$$C_3 = \frac{1}{2\pi \times 100\ k\Omega \times 5.8\ kHz} = 274p \approx 270\ pF, \text{ from } f_{Z2} \quad (83)$$

$$R_3 = \frac{1}{2\pi \times 270\ pF \times 69\ kHz} = 8.54\ k\Omega \approx 8.45\ k\Omega, \text{ from } f_{P2} \quad (84)$$

$$C_2 = \frac{1}{2\pi \times 100\ k\Omega \times 20\ kHz} = 79.6\ pF, \text{ from } f_C \approx 82\ pF \quad (85)$$

$$R_2 = \frac{1}{2\pi \times 82\ pF \times 69\ kHz} = 28.1\ k\Omega, \text{ from } f_{P1} \approx 28\ k\Omega \quad (86)$$

$$C_1 = \frac{1}{2\pi \times 28\ k\Omega \times 5.8\ kHz} = 980\ pF \approx 1000\ pF, \text{ from } f_{Z1} \quad (87)$$

$$R_{BIAS} = \frac{0.7 \times 100k\Omega}{3.3 - 0.7} = 26.9\ k\Omega \approx 26.7\ k\Omega \quad (88)$$

GATE DRIVE CONFIGURATION

Due to the possibility of dv/dt induced turn-on from the fast MOSFET switching times, high V_{DS} voltage and low gate threshold voltage of the Si4470, the design includes a 2-Ω in the gate lead of the upper MOSFET. The resistor can be used to shape the low-to-high transition of the SWitch node and reduce the tendancy of dv/dt-induced turn on.

DESIGN EXAMPLE

CALCULATING THE BPN10 AND BP10V BYPASS CAPACITANCE

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass capacitor. The BPN10 capacitance, allowing for a 0.5-V droop on the BPN10 pin from (9) is shown in equation (89).

$$C_{BPN10} = \frac{Q_g}{\Delta V} = \frac{30\ nC}{0.5} = 60\ nF \quad (89)$$

and the BP10V capacitance from equation (10) is shown in equation (90).

$$C_{BP10V} = \frac{Q_{gSR}}{\Delta V} = \frac{57\ nC}{0.5} = 114\ nF \quad (90)$$

For this application, a 0.1-µF capacitor was used for the BPN10V and a 1.0-µF was used for the BP10V bypass ccapacitor. Figure 13 shows component selection for the 18-V through 55-V to 3.3-V at 5-A dc-to-dc converter specified in the design example.

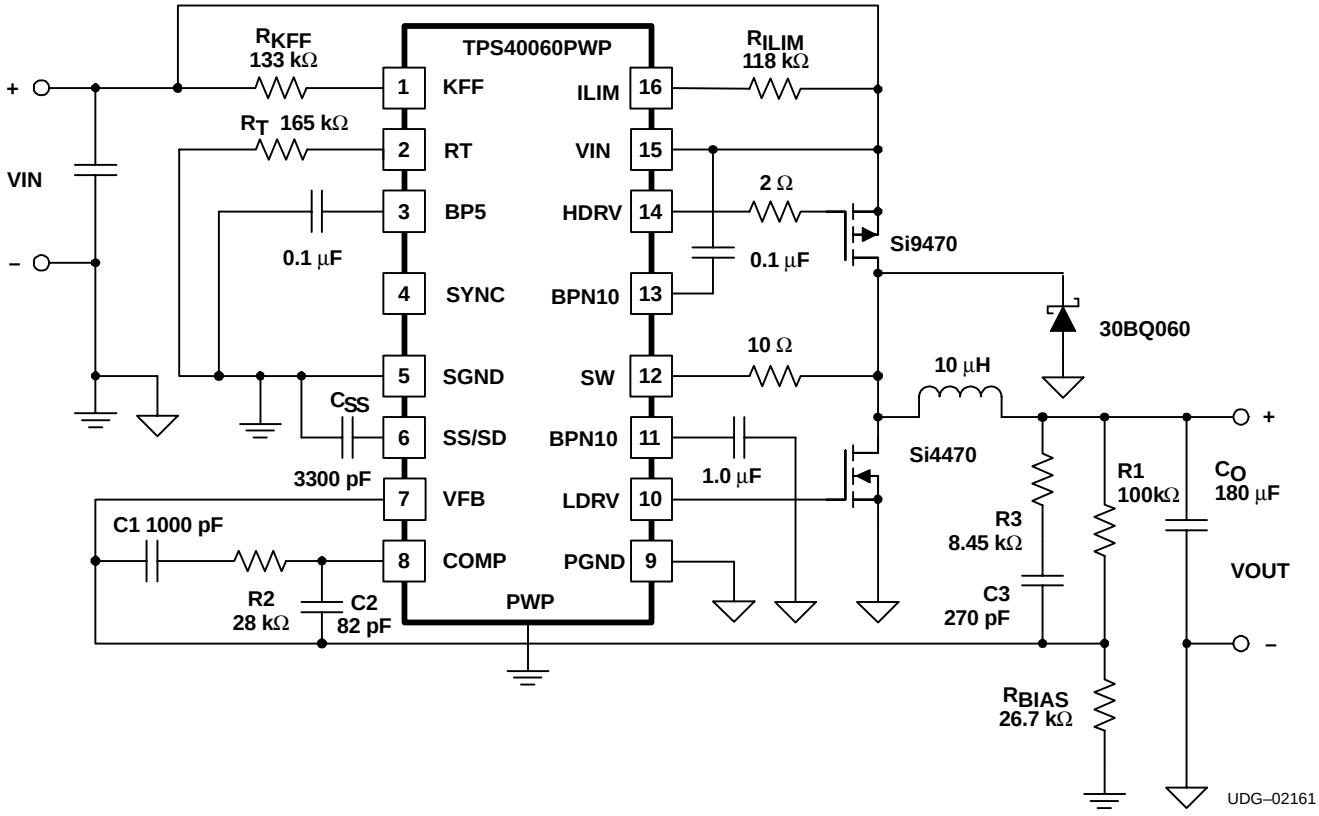


Figure 13. Design Example, 48 V to 3.3 V at 5 A dc-to-dc Converter

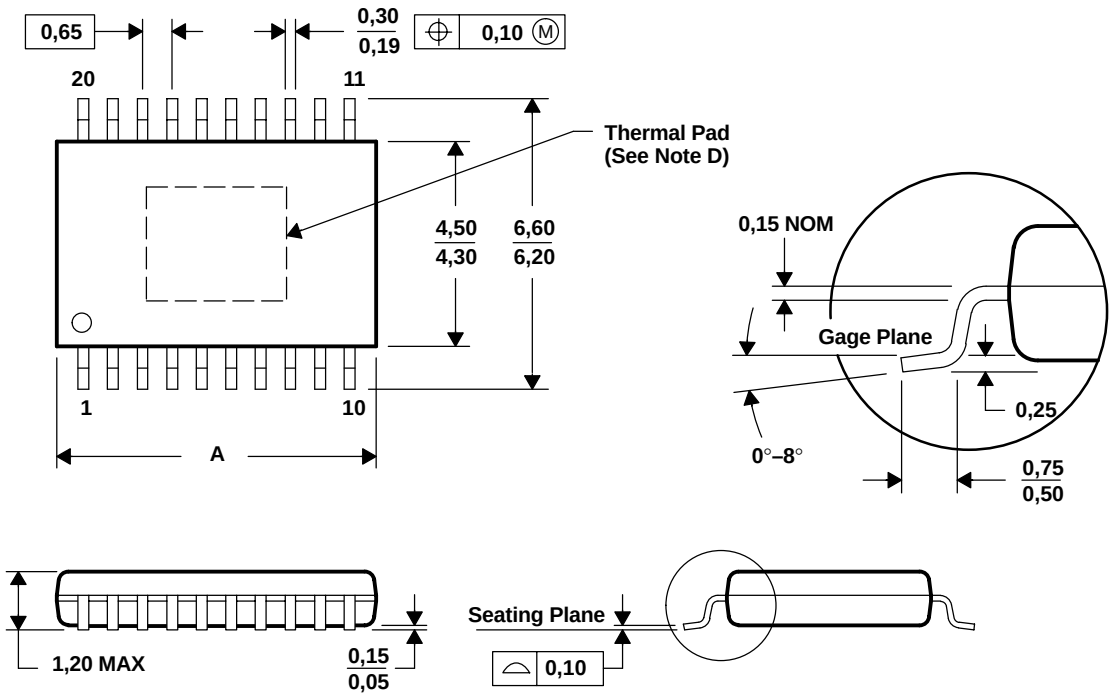
REFERENCES

1. Venable, H. Dean, *The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis* Proceedings of Powercon 10, pp A5–1 through A5–12
2. Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM–1400 Topic 2.
3. *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief: TI Literature No. SLMA002

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265