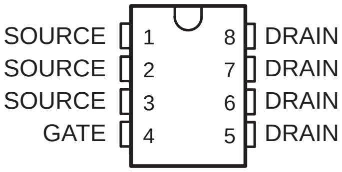
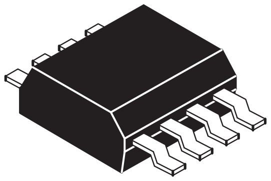
TPS1101, TPS1101Y
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

- **Low $r_{DS(on)}$ . . . 0.09 Ω Typ at V_{GS} = −10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

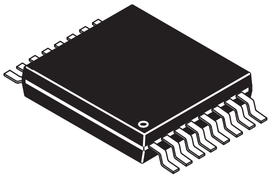
D PACKAGE
(TOP VIEW)



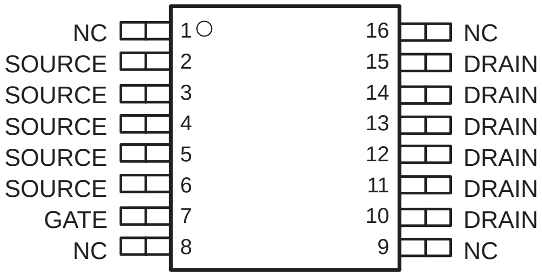
D PACKAGE



PW PACKAGE



PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS1101 is a single, low-$r_{DS(on)}$, P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 µA, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†		CHIP FORM (Y)
	SMALL OUTLINE (D)	TSSOP (PW)	
−40°C to 150°C	TPS1101D	TPS1101PWLE	TPS1101Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at 25°C.

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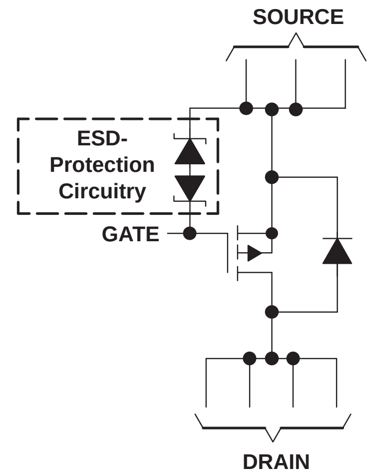
schematic

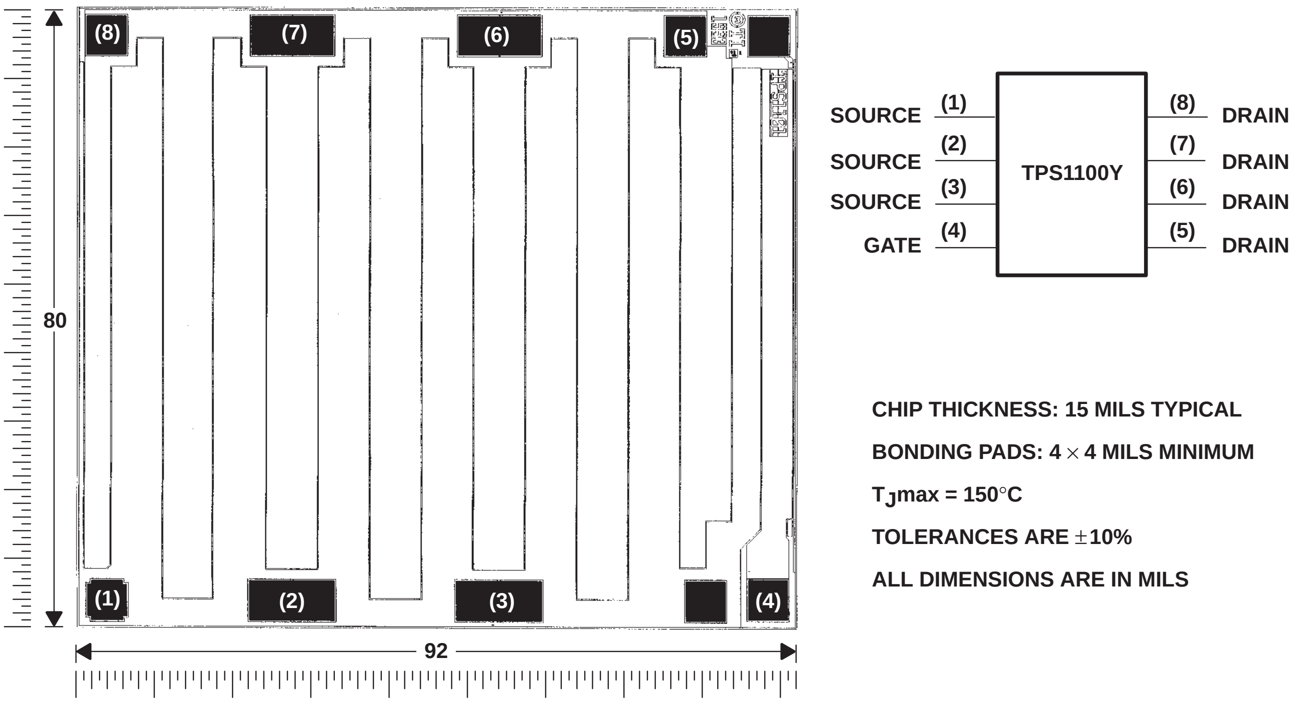


NOTE A: For all applications, all source terminals should be connected and all drain terminals should be connected.

TPS1101Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

					UNIT
Drain-to-source voltage, V_{DS}				– 15	V
Gate-to-source voltage, V_{GS}				2 or – 15	V
Continuous drain current (T_J = 150°C), I_D[‡]	V_{GS} = –2.7 V	D package	T_A = 25°C	±0.62	A
			T_A = 125°C	±0.39	
		PW package	T_A = 25°C	±0.61	
			T_A = 125°C	±0.38	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.88	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.86	
			T_A = 125°C	±0.45	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1.52	
			T_A = 125°C	±0.71	
		PW package	T_A = 25°C	±1.44	
			T_A = 125°C	±0.67	
	V_{GS} = –10 V	D package	T_A = 25°C	±2.30	
			T_A = 125°C	±1.04	
		PW package	T_A = 25°C	±2.18	
			T_A = 125°C	±0.98	
Pulsed drain current, I_D[‡]			T_A = 25°C	±10	A
Continuous source current (diode conduction), I_S			T_A = 25°C	–1.1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	**$T_A \le 25°C$ POWER RATING**	**DERATING FACTOR[‡] ABOVE T_A = 25°C**	**T_A = 70°C POWER RATING**	**T_A = 85°C POWER RATING**	**T_A = 125°C POWER RATING**
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1101			TPS1101Y			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	I_D = –250 μA		–1	–1.25	–1.5		–1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	I_S = –1 A,	V_{GS} = 0 V			–1.04			–1.04		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = –12 V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = –12 V,	V_{GS} = 0 V	T_J = 25°C			–0.5				μA
				T_J = 125°C			–10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = –10 V	I_D = –2.5 A			90			90		mΩ
		V_{GS} = –4.5 V	I_D = –1.5 A			134	190		134		
		V_{GS} = –3 V	I_D = –0.5 A			198	310		198		
		V_{GS} = –2.7 V				232	400		232		
g_{fs}	Forward transconductance†	V_{DS} = –10 V,	I_D = –2 A			4.3			4.3		S

† Pulse test: pulse duration ≤ 300 μs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1101, TPS1101Y			UNIT
					MIN	TYP	MAX	
Q_g	Total gate charge	V_{DS} = –10 V,	V_{GS} = –10 V,	I_D = –1 A		11.25		nC
Q_{gs}	Gate-to-source charge					1.5		
Q_{gd}	Gate-to-drain charge					2.6		
$t_{d(on)}$	Turn-on delay time	V_{DD} = –10 V, R_G = 6 Ω,	R_L = 10 Ω, See Figures 1 and 2	I_D = –1 A,		6.5		ns
$t_{d(off)}$	Turn-off delay time					19		ns
t_r	Rise time					5.5		ns
t_f	Fall time					13		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/μs			16		

PARAMETER MEASUREMENT INFORMATION

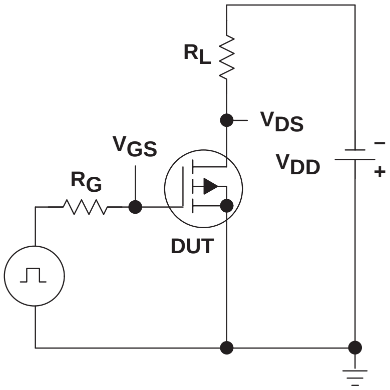


Figure 1. Switching-Time Test Circuit

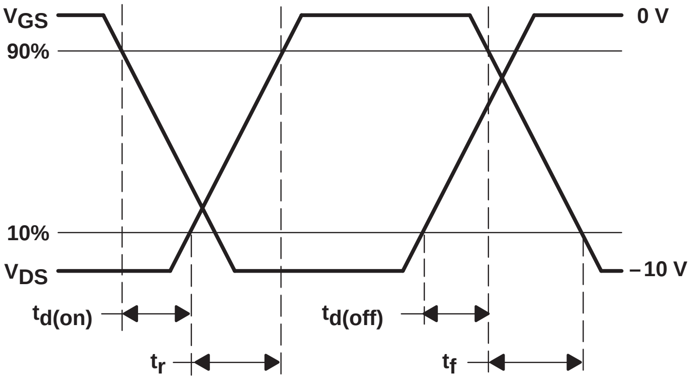


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

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Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

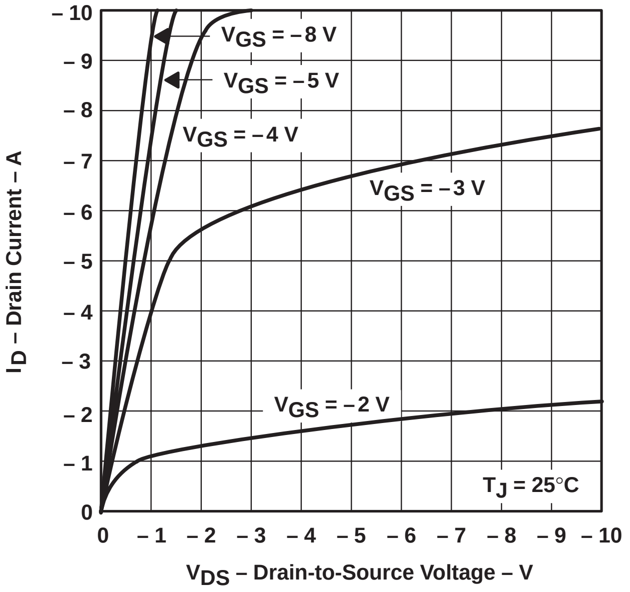


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

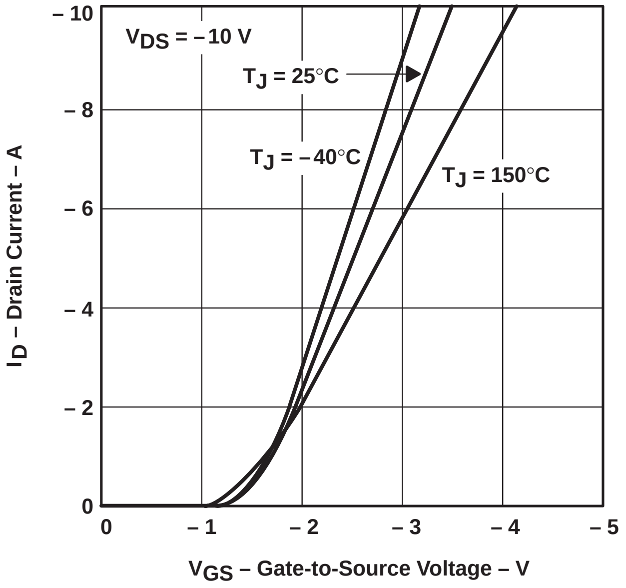


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

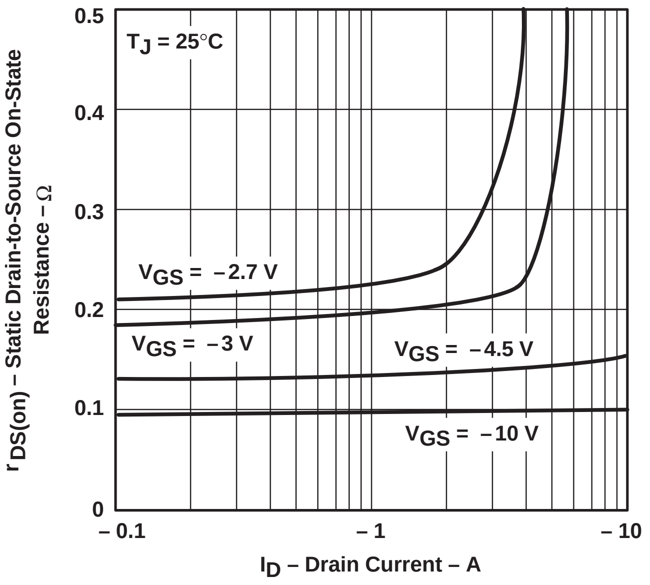
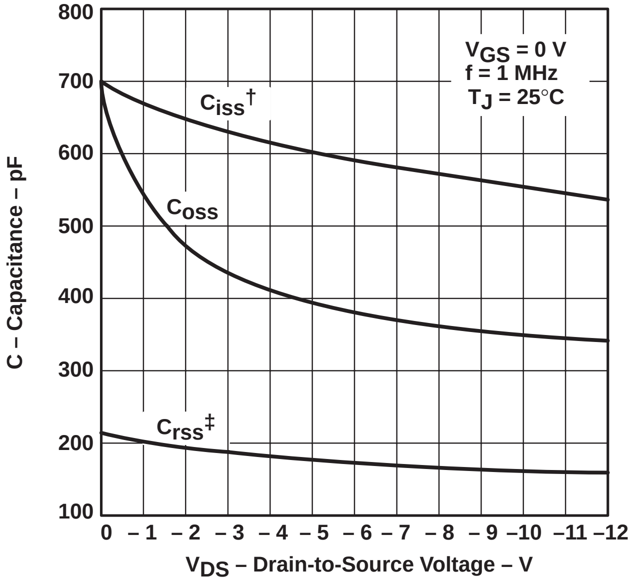


Figure 5

CAPACITANCE[†] vs DRAIN-TO-SOURCE VOLTAGE



[†] $C_{iss} = C_{gs} + C_{gd}, \ C_{ds(shorted)}$

[‡] $C_{rss} = C_{gd}, \ C_{oss} = C_{ds} + \frac{C_{gs}\ C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

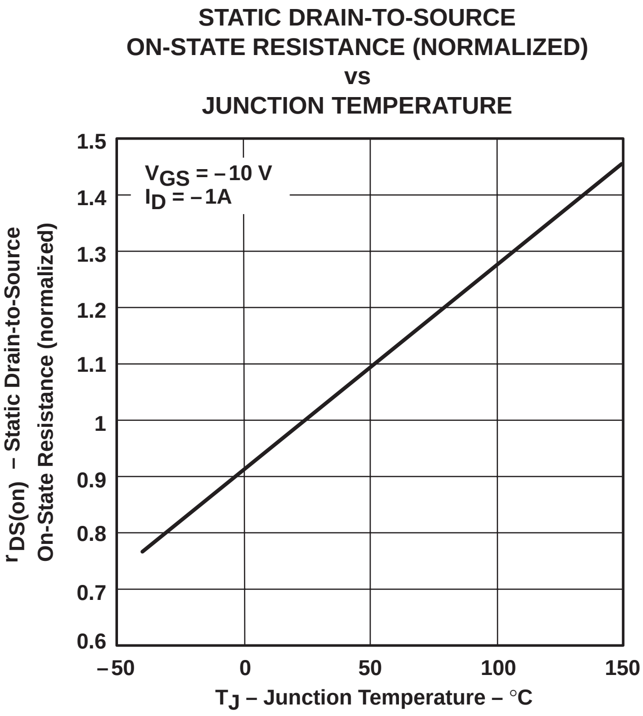


Figure 7

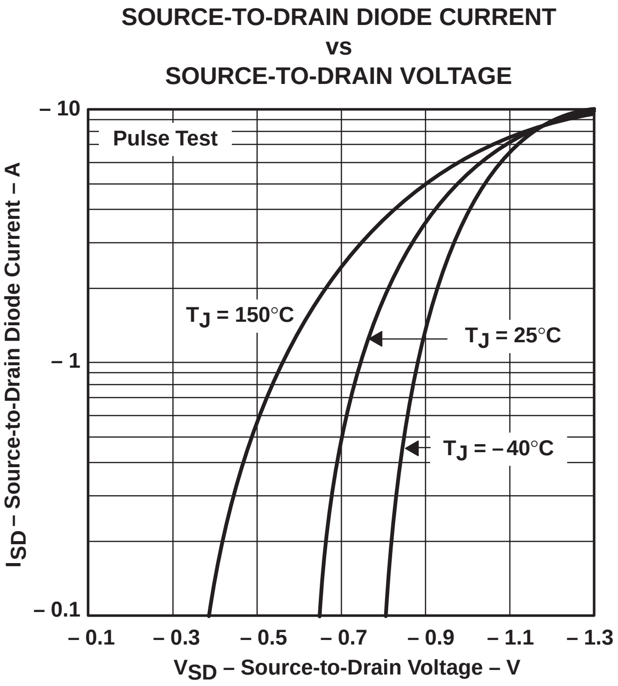


Figure 8

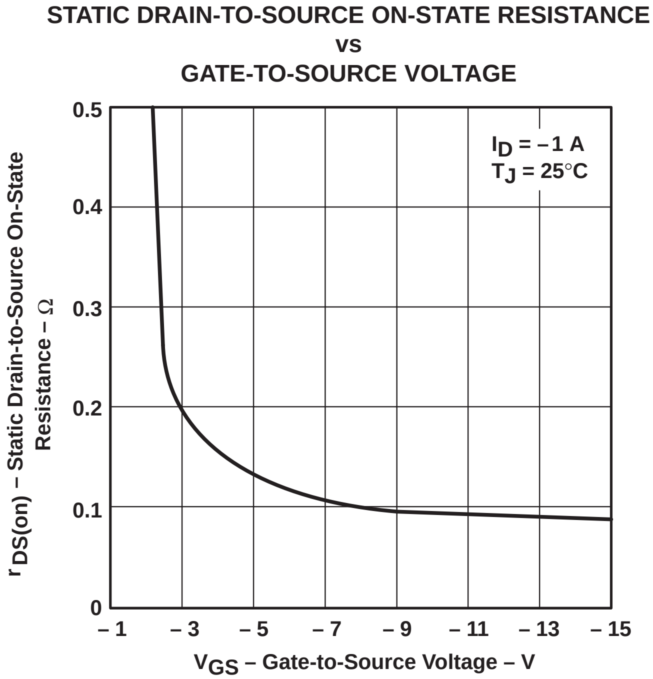


Figure 9

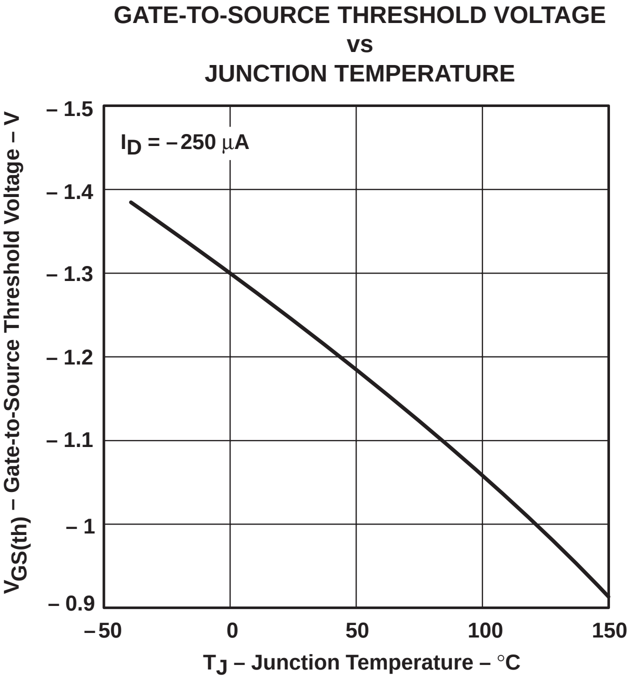


Figure 10

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

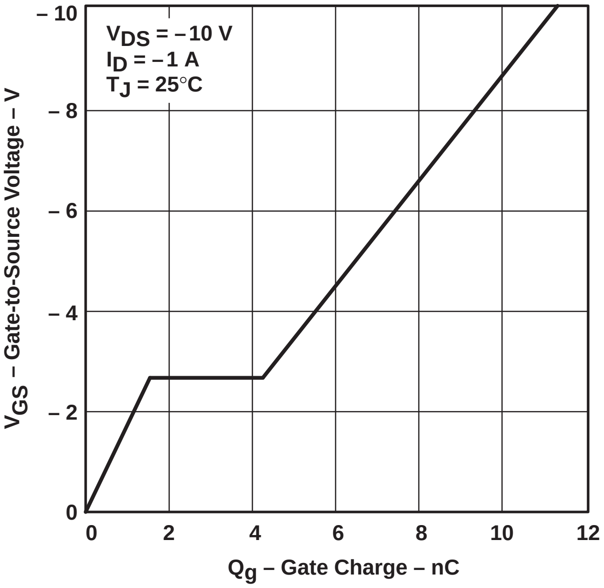
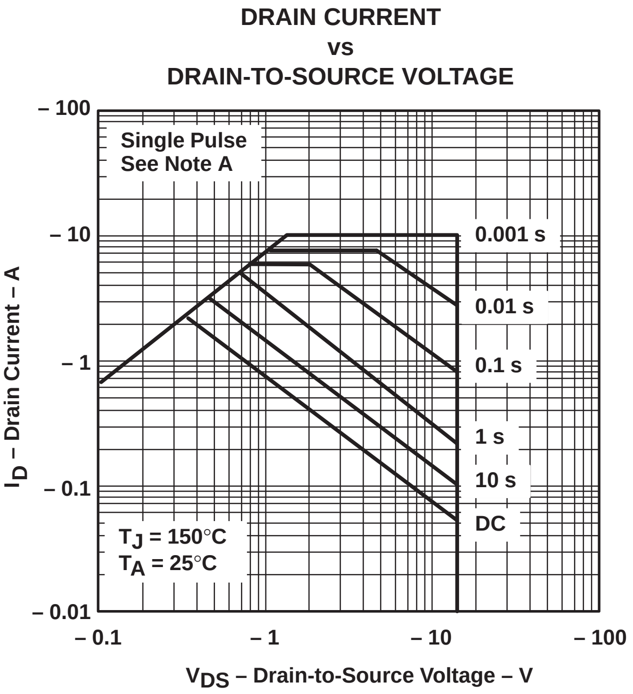


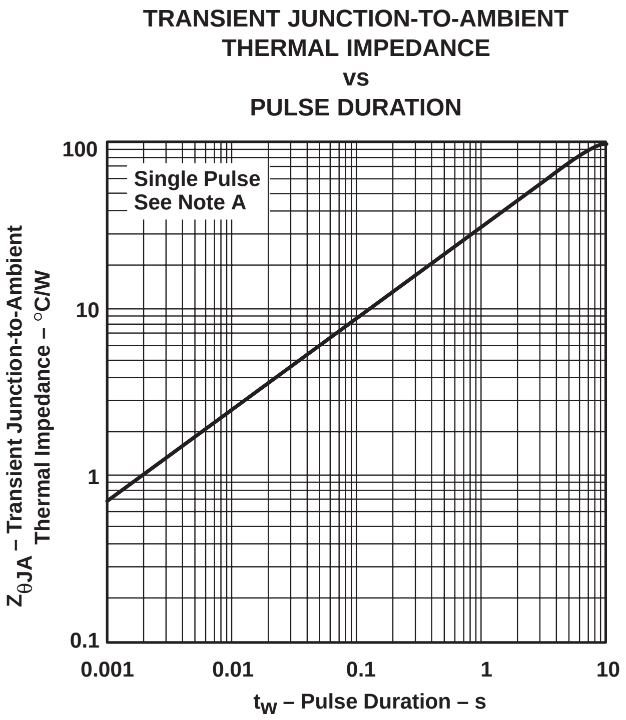
Figure 11

THERMAL INFORMATION



NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 12



NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 13

APPLICATION INFORMATION

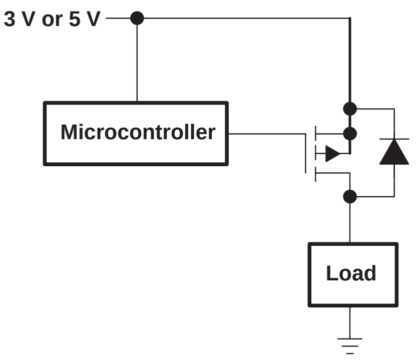


Figure 14. Notebook Load Management

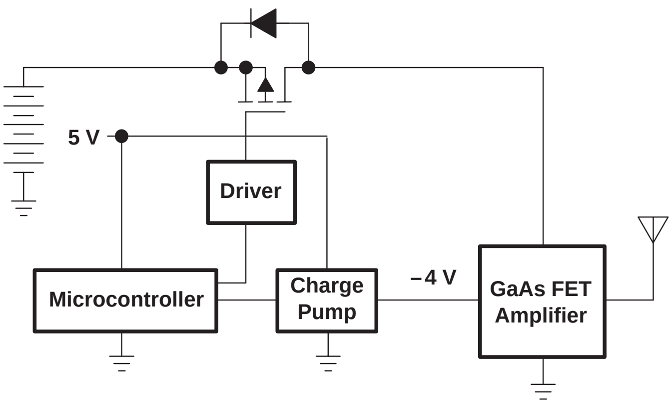


Figure 15. Cellular Phone Output Drive

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