- **80-mΩ High-Side MOSFET Switch**
- **250 mA Continuous Current per Channel**
- **Independent Thermal and Short-Circuit Protection With Overcurrent Logic Output**
- **Operating Range . . . 2.7-V to 5.5-V**
- **CMOS- and TTL-Compatible Enable Inputs**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **10 µA Maximum Standby Supply Current**
- **Bidirectional Switch**
- **Available in 8-Pin and 16-Pin SOIC Packages**
- **Ambient Temperature Range, 0°C to 85°C**
- **ESD Protection**

TPS2090, TPS2091, AND TPS2092
D PACKAGE
(TOP VIEW)

GND	1	8	$\overline{OC}$
IN1	2	7	OUT1
IN2	3	6	OUT2
EN1†	4	5	EN2†

† See Available Options table

TPS2095, TPS2096 AND TPS2097
D PACKAGE
(TOP VIEW)

GNDA	1	16	$\overline{OCA}$
IN1	2	15	OUT1
IN2	3	14	OUT2
EN1†	4	13	EN2†
GNDB	5	12	$\overline{OCB}$
IN3	6	11	OUT3
IN4	7	10	OUT4
EN3†	8	9	EN4†

† See Available Options table

description

The TPS2090, TPS2091, and TPS2092 dual and the TPS2095, TPS2096 and TPS2097 quad power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS209x devices incorporate 80-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by an independent logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS209x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. The TPS209x devices are designed to current limit at 0.5-A load.

GENERAL SWITCH CATALOG

33 mW, single	80 mW, dual	80 mW, dual	80 mW, triple	80 mW, quad	80 mW, quad
TPS201xA 0.2 A – 2 A TPS202x 0.2 A – 2 A TPS203x 0.2 A – 2 A	TPS2042 500 mA TPS2052 500 mA TPS2046 250 mA TPS2056 250 mA	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043 500 mA TPS2053 500 mA TPS2047 250 mA TPS2057 250 mA	TPS2044 500 mA TPS2054 500 mA TPS2048 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA
80 mW, single TPS2014 600 mA TPS2015 1 A TPS2041 500 mA TPS2051 500 mA TPS2045 250 mA TPS2055 250 mA	**260 mW** (IN1, IN2, OUT) **1.3 W** TPS2100/1 IN1 500 mA IN2 10 mA TPS2102/3/4/5 IN1 500 mA IN2 100 mA				

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

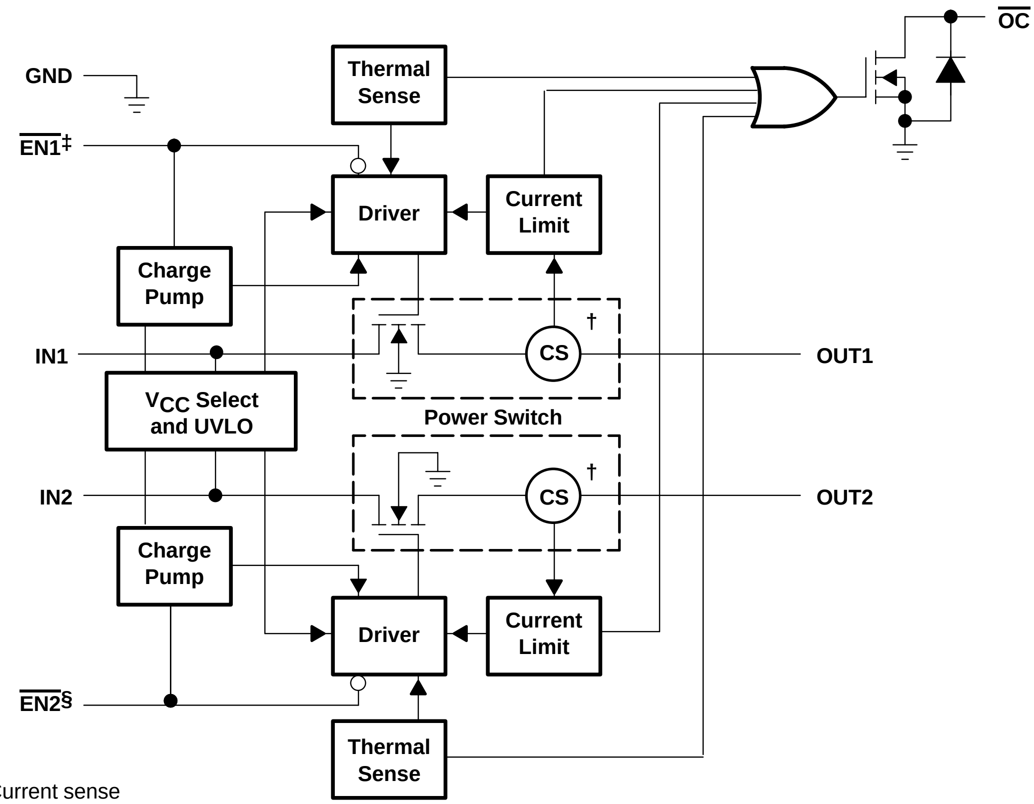
AVAILABLE OPTIONS

DUAL POWER DISTRIBUTION SWITCHES					
T_A	ENABLE		RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES
	EN1	EN2			SMALL OUTLINE (D)†
0°C to 85°C	Active high	Active high	0.25	0.5	TPS2090D
	Active high	Active low			TPS2091D
	Active low	Active low			TPS2092D

QUAD POWER DISTRIBUTION SWITCHES							
T_A	ENABLE				RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES
	EN1	EN2	EN3	EN4			SMALL OUTLINE (D)†
0°C to 85°C	Active high	Active high	Active high	Active high	0.25	0.5	TPS2095D
	Active high	Active low	Active high	Active low			TPS2096D
	Active low	Active low	Active low	Active low			TPS2097D

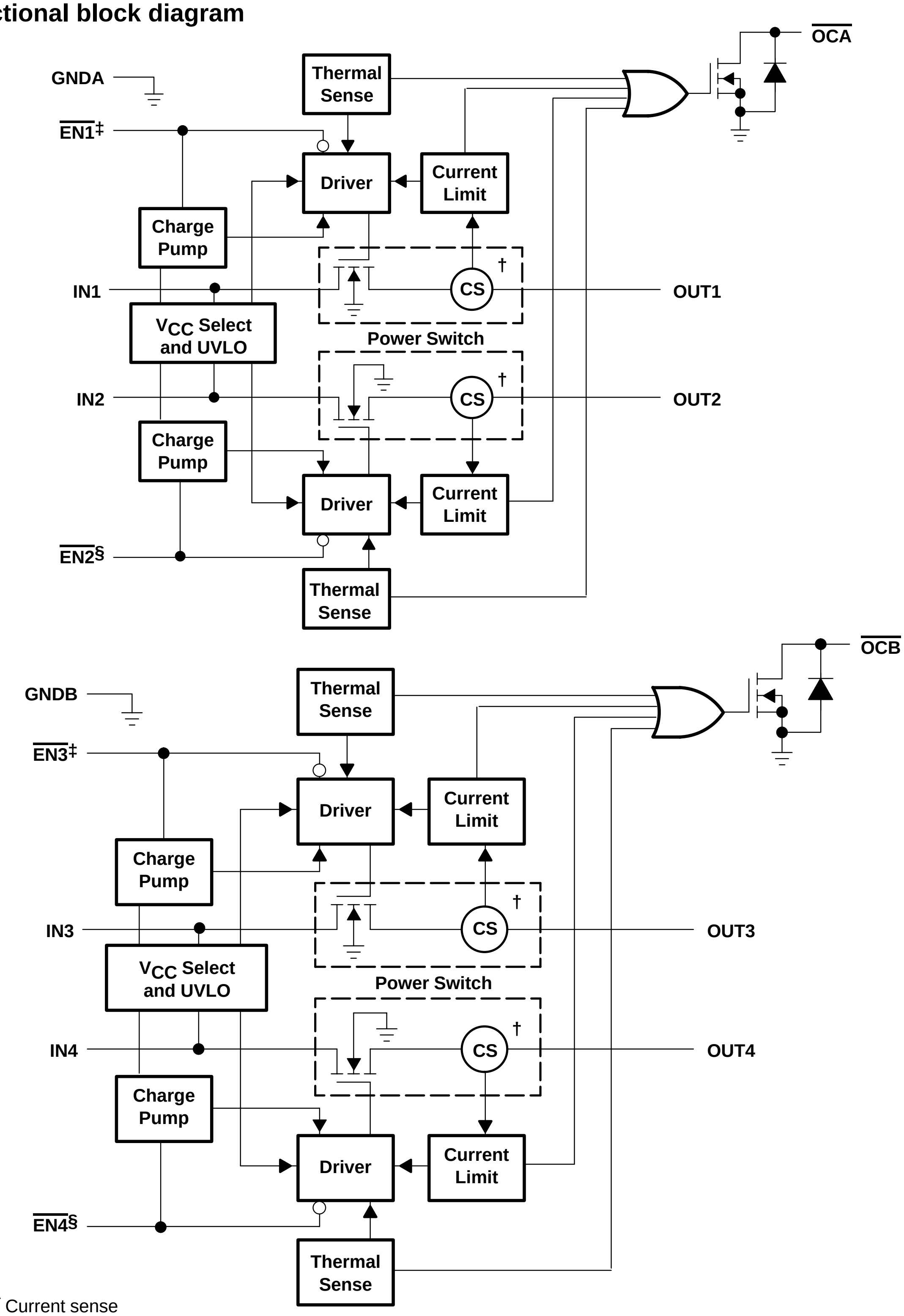
† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2091DR)

TPS2092 functional block diagram



† Current sense
‡ Active high for TPS2090 and TPS2091
§ Active high for TPS2090

TPS2097 functional block diagram



† Current sense
‡ Active high for TPS2095 and TPS2096
§ Active high for TPS2095

Terminal Functions

DUAL POWER-DISTRIBUTION SWITCHES

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	TPS2090	TPS2091	TPS2092		
$\overline{EN1}$			4	I	Enable input. Active low turns on power switch.
$\overline{EN2}$		5	5	I	Enable input. Active low turns on power switch.
EN1	4	4		I	Enable input. Active high turns on power switch.
EN2	5			I	Enable input. Active high turns on power switch.
GND	1	1	1	I	Ground
IN1	2	2	2	I	N-Channel MOSFET Drain
IN2	3	3	3	I	N-Channel MOSFET Drain
$\overline{OC}$	8	8	8	O	Overcurrent. Open drain output active low
OUT1	7	7	7	O	Power-switch output
OUT2	6	6	6	O	Power-switch output

QUAD POWER-DISTRIBUTION SWITCHES

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	TPS2095	TPS2096	TPS2097		
$\overline{EN1}$			4	I	Enable input. Active low turns on power switch.
$\overline{EN2}$		13	13	I	Enable input. Active low turns on power switch.
$\overline{EN3}$			8	I	Enable input. Active low turns on power switch.
$\overline{EN4}$		9	9	I	Enable input. Active low turns on power switch.
EN1	4	4		I	Enable input. Active high turns on power switch.
EN2	13			I	Enable input. Active high turns on power switch.
EN3	8	8		I	Enable input. Active high turns on power switch.
EN4	9			I	Enable input. Active high turns on power switch.
GNDA	1	1	1		Ground for IN1 and IN2 switch and circuitry
GNDB	5	5	5		Ground for IN3 and IN4 switch and circuitry
IN1	2	2	2	I	N-channel MOSFET drain
IN2	3	3	3	I	N-channel MOSFET drain
IN3	6	6	6	I	N-channel MOSFET drain
IN4	7	7	7	I	N-channel MOSFET drain
$\overline{OCA}$	16	16	16	O	Overcurrent indicator for switch 1 and switch 2. Active-low open drain output.
$\overline{OCB}$	12	12	12	O	Overcurrent indicator for switch 3 and switch 4. Active low open drain output
OUT1	15	15	15	O	Power-switch output
OUT2	14	14	14	O	Power-switch output
OUT3	11	11	11	O	Power-switch output
OUT4	10	10	10	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch supplies a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic high is present on $\overline{\text{ENx}}$ or a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS209x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) . . . . –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note 1) . . . . –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ . . . . –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ . . . . internally limited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . 0°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Electrostatic discharge (ESD) protection: Human body model . . . . 2 kV
Machine model . . . . 200 V
Charged device model (CDM) . . . . 750 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW
D-16	1123 mW	9 mW/°C	719 mW	584 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	V
Continuous output current, I_O (per switch)	0	250	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = $V_{I(INx)}$ (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	$V_{I(\overline{ENx})} = V_{I(IN)}$, $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.025	1	µA
			–40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	$V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)} = V_{I(IN)}$	T_J = 25°C		85	110	µA
			–40°C ≤ T_J ≤ 125°C		100		
Leakage current	OUT connected to ground	$V_{I(\overline{ENx})} = V_{I(IN)}$, $V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C		100		µA
Reverse leakage current	INx = high impedance	$V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)} = V_{I(IN)}$	T_J = 125°C		0.3		µA

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = $V_{I(INx)}$ (unless otherwise noted) (continued)

power switch

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V, T_J = 25°C, I_O = 0.25 A		80	100	mΩ
		$V_{I(IN)}$ = 5 V, T_J = 85°C, I_O = 0.25 A		90	120	
		$V_{I(IN)}$ = 5 V, T_J = 125°C, I_O = 0.25 A		100	135	
		$V_{I(IN)}$ = 3.3 V, T_J = 25°C, I_O = 0.25 A		90	125	
		$V_{I(IN)}$ = 3.3 V, T_J = 85°C, I_O = 0.25 A		110	145	
		$V_{I(IN)}$ = 3.3 V, T_J = 125°C, I_O = 0.25 A		120	165	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 μF, R_L=20 Ω		2.5		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 μF, R_L=20 Ω		3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 μF, R_L=20 Ω		4.4		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 μF, R_L=20 Ω		2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V≤ $V_{I(IN)}$ ≤ 4.5 V			0.4	
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V and $V_{I(ENx)}$ = $V_{I(IN)}$, or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$ and $V_{I(ENx)}$ = 0 V	–0.5		0.5	μA
t_{on}	Turnon time	C_L = 100 μF, R_L=20 Ω			20	ms
t_{off}	Turnoff time	C_L = 100 μF, R_L=20 Ω			40	

current limit

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit	0.3	0.5	0.7	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	T_J = 25°C		100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sink current†	V_O = 5 V			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1	μA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

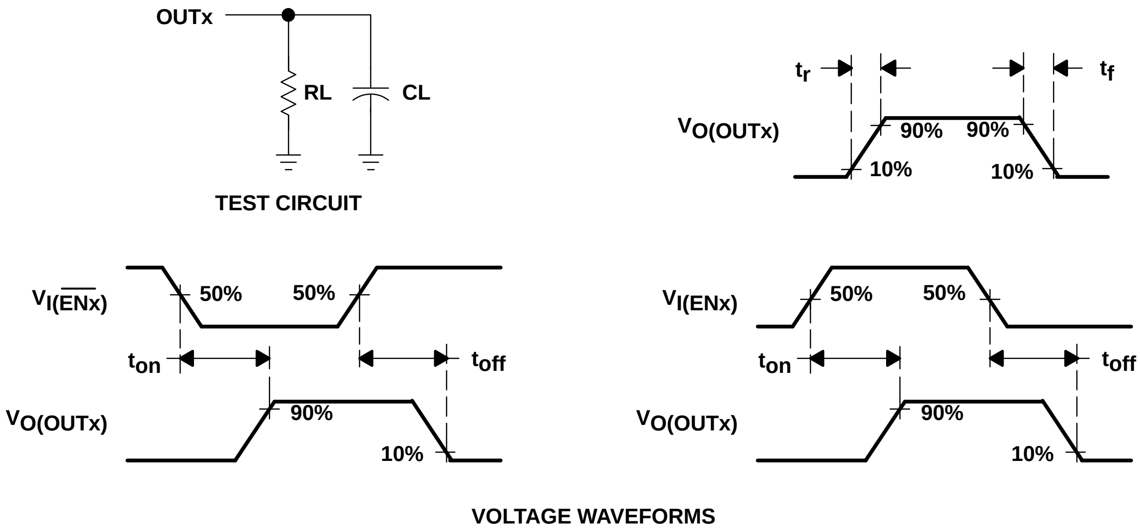


Figure 1. Test Circuit and Voltage Waveforms

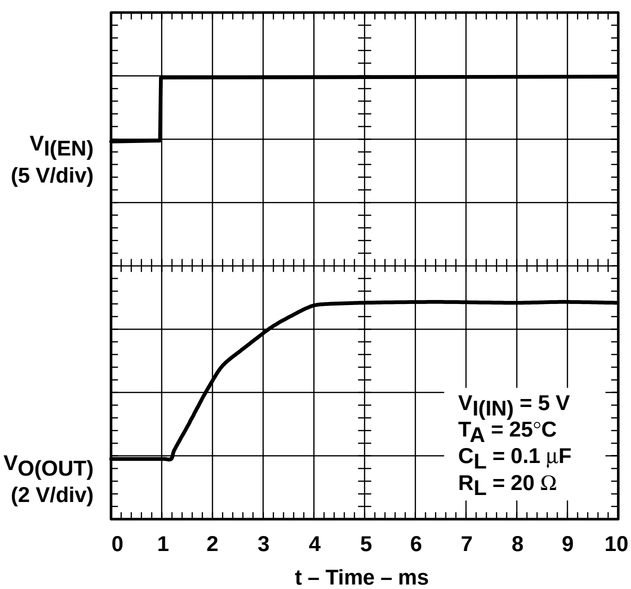


Figure 2. Turnon Delay and Rise Time With 0.1-μF Load

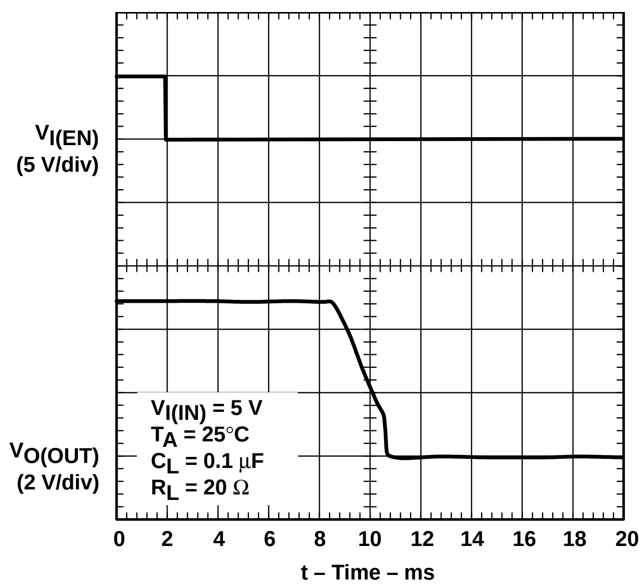


Figure 3. Turnoff Delay and Fall Time With 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

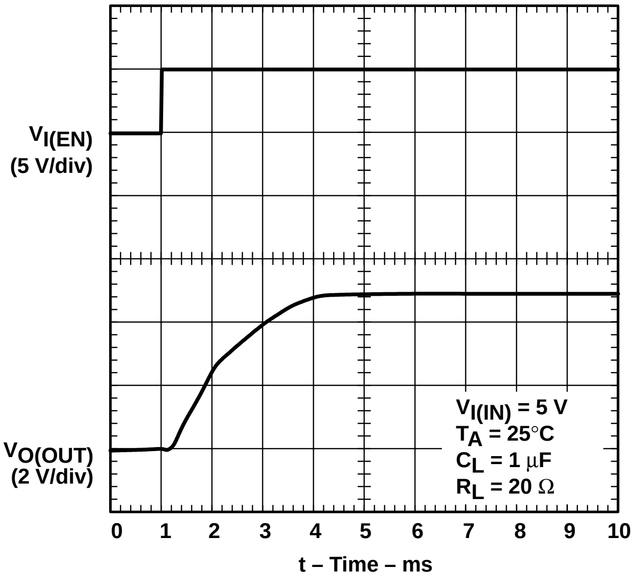


Figure 4. Turnon Delay and Rise Time With 1-µF Load

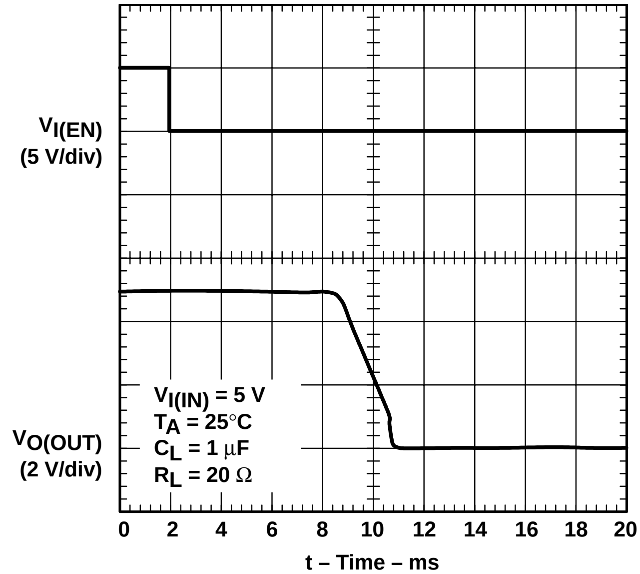


Figure 5. Turnoff Delay and Fall Time With 1-µF Load

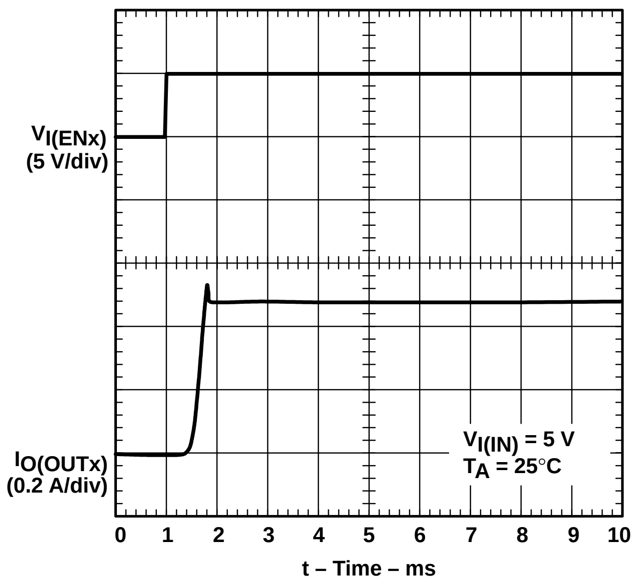


Figure 6. TPS2090, Short-Circuit Current, Device Enabled Into Short

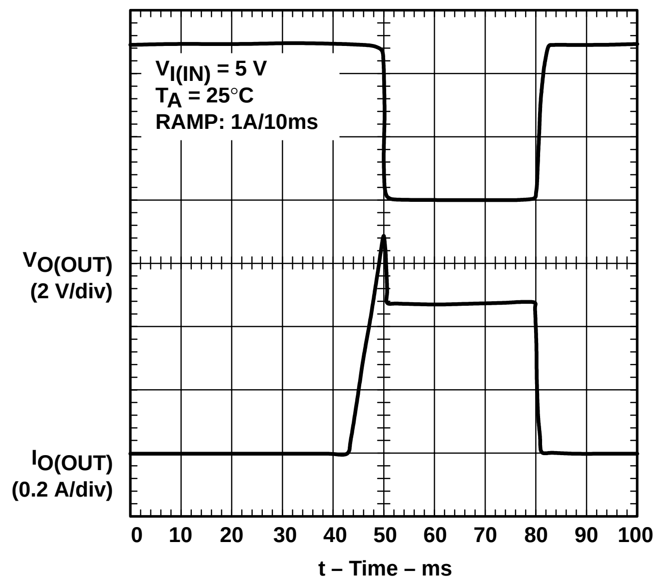


Figure 7. TPS2090, Threshold Trip Current With Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

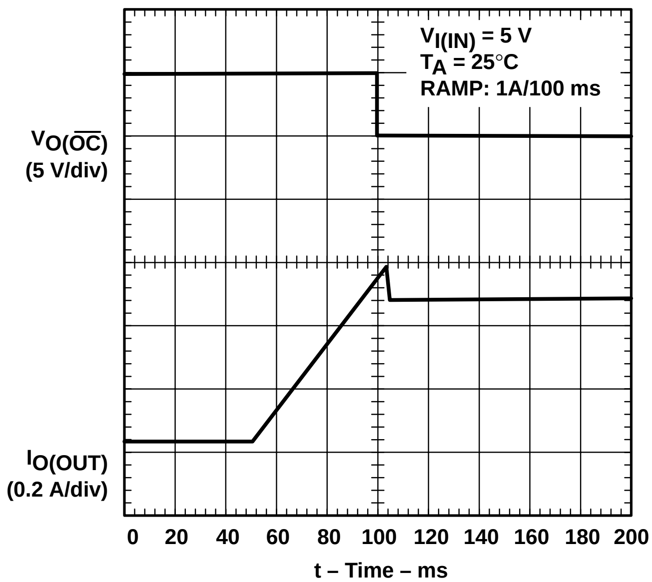


Figure 8. Ramped Load on Enabled Device

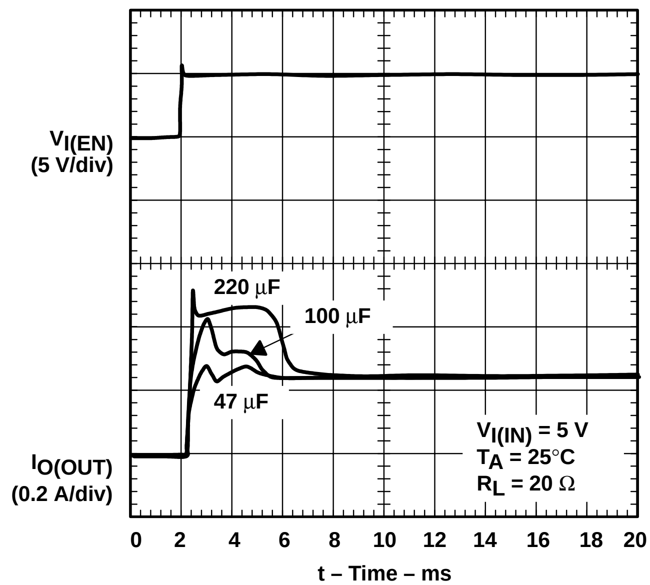


Figure 9. Inrush Current With 47-µF, 100-µF and 220-µF Load Capacitance

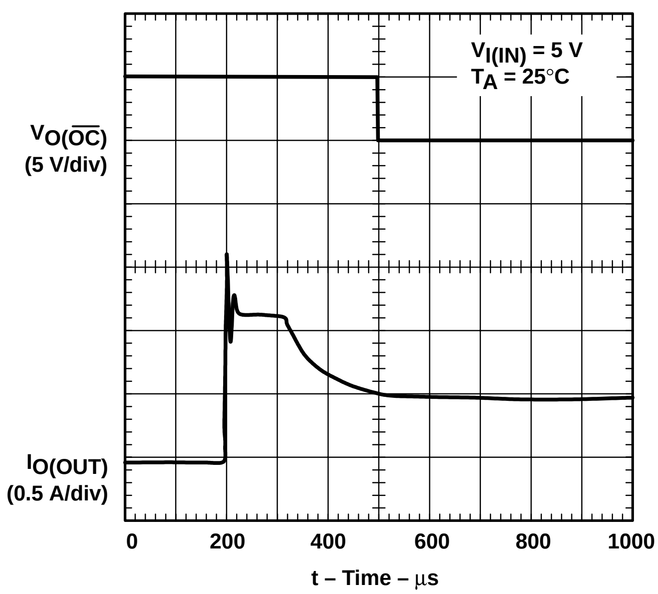


Figure 10. 4-Ω Load Connected to Enabled Device

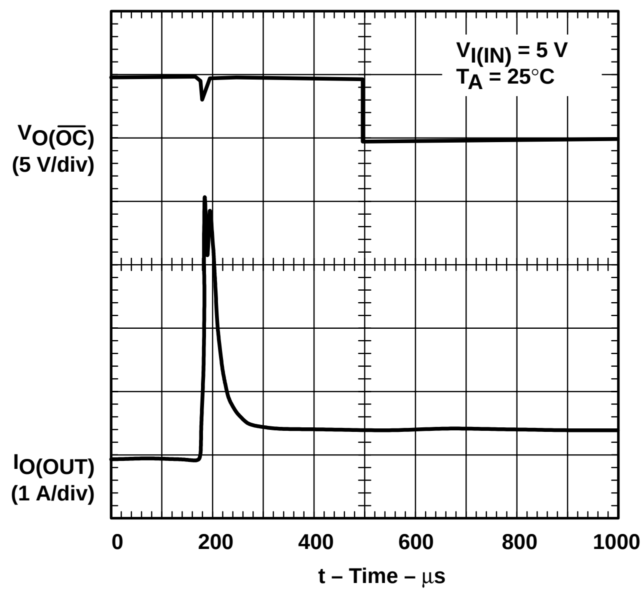


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY TIME vs INPUT VOLTAGE

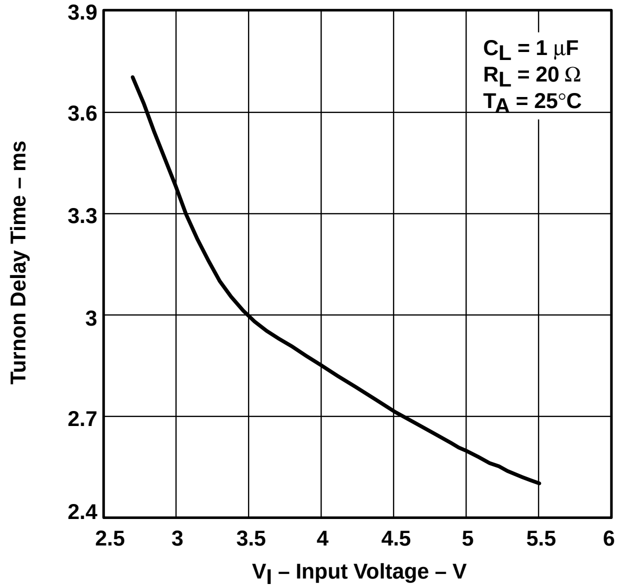


Figure 12

TURNOFF DELAY TIME vs INPUT VOLTAGE

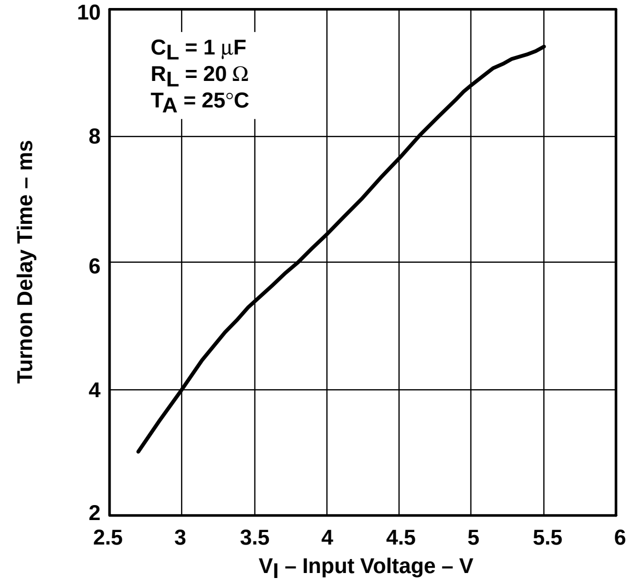


Figure 13

RISE TIME vs INPUT VOLTAGE

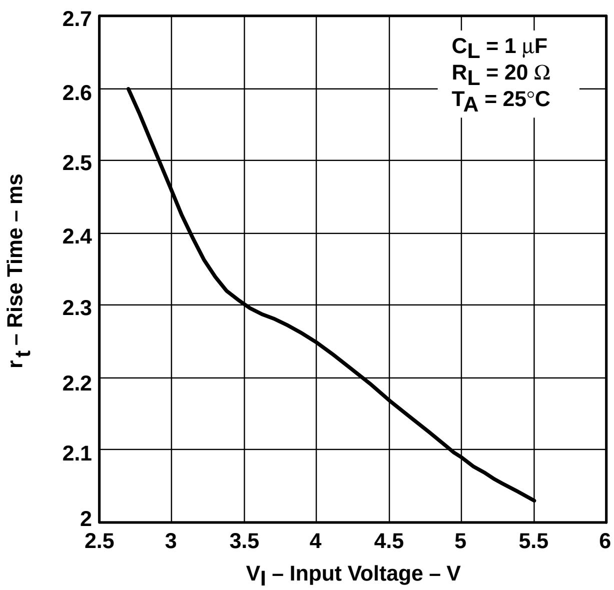


Figure 14

FALL TIME vs INPUT VOLTAGE

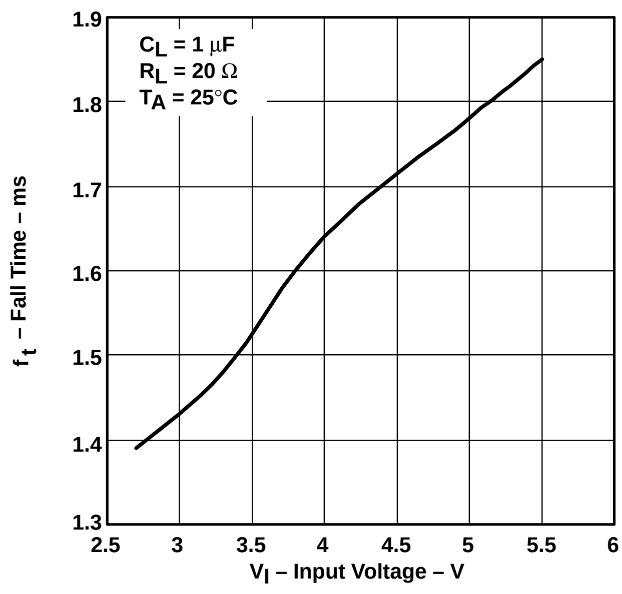


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

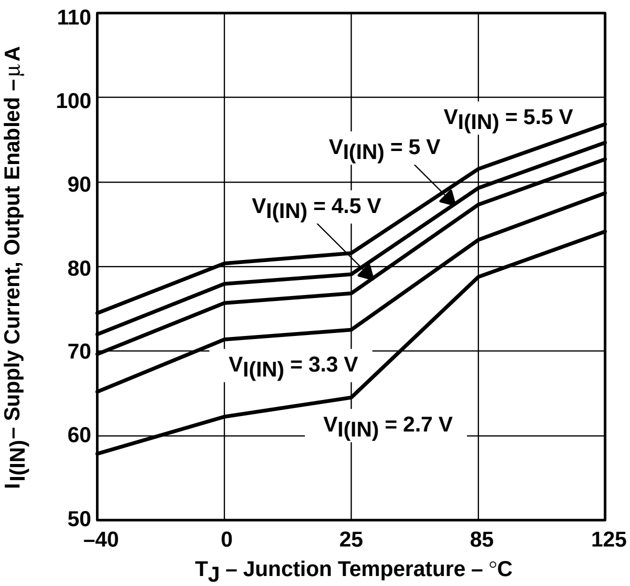


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

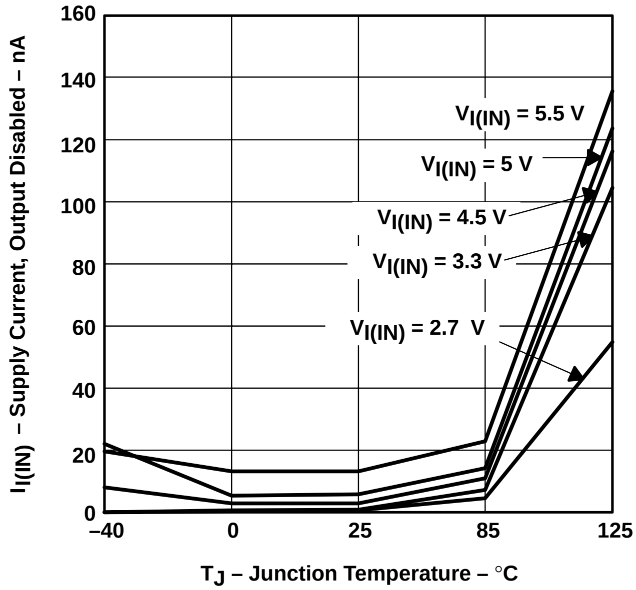


Figure 17

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

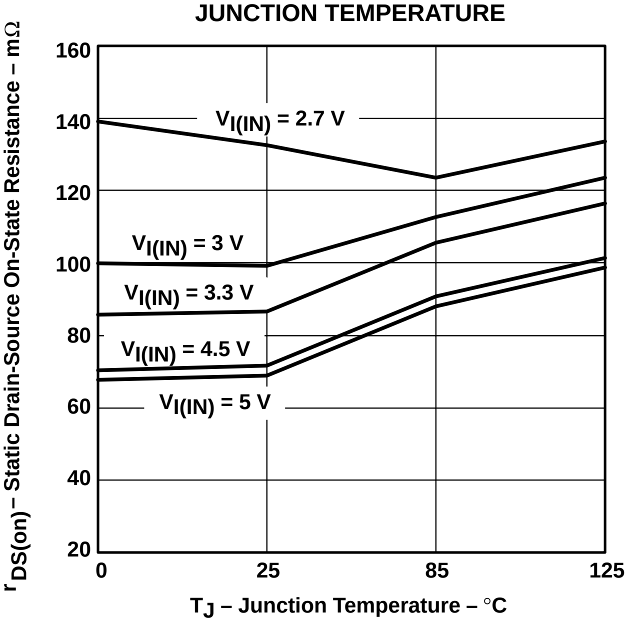


Figure 18

INPUT-TO-OUTPUT VOLTAGE vs LOAD CURRENT

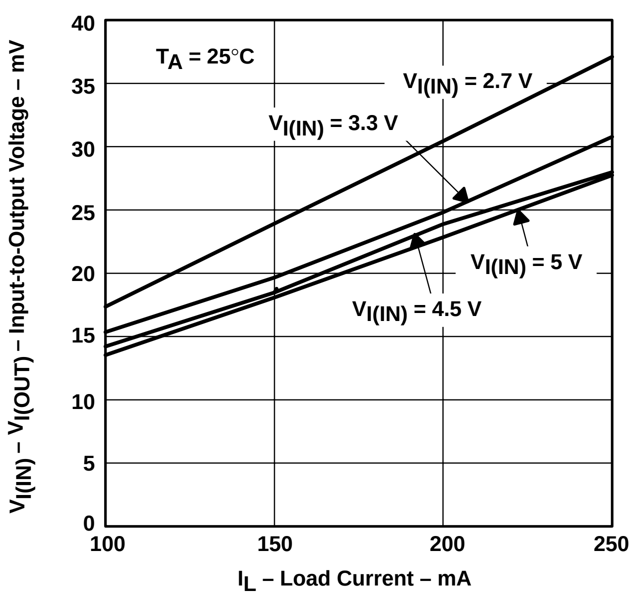


Figure 19

TYPICAL CHARACTERISTICS

**SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE**

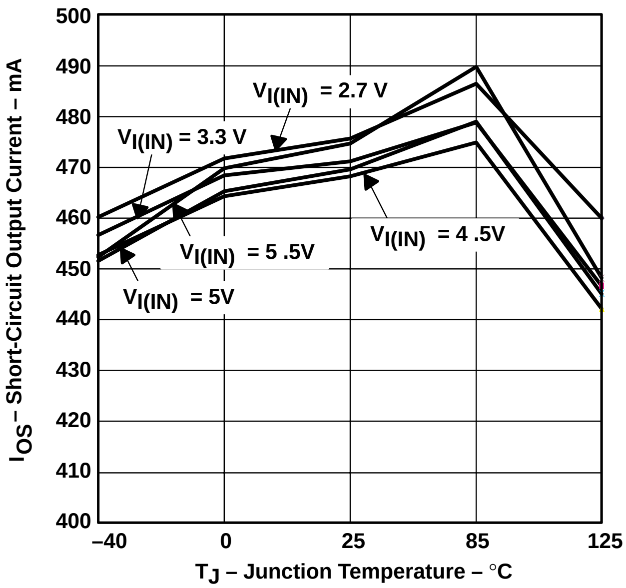


Figure 20

**THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE**

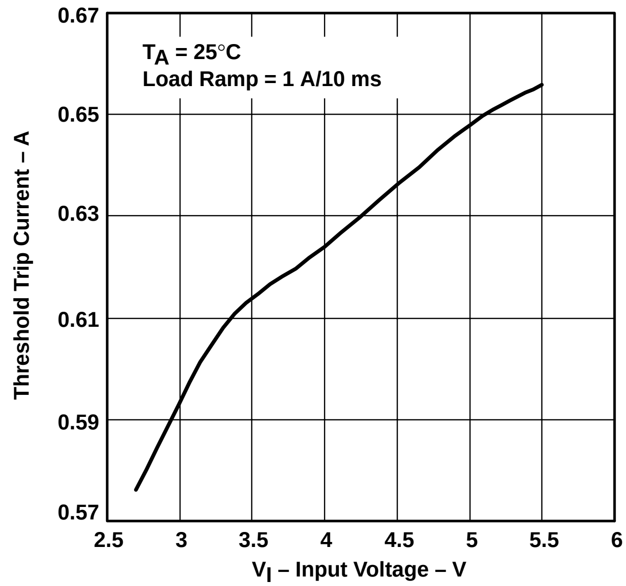


Figure 21

**UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE**

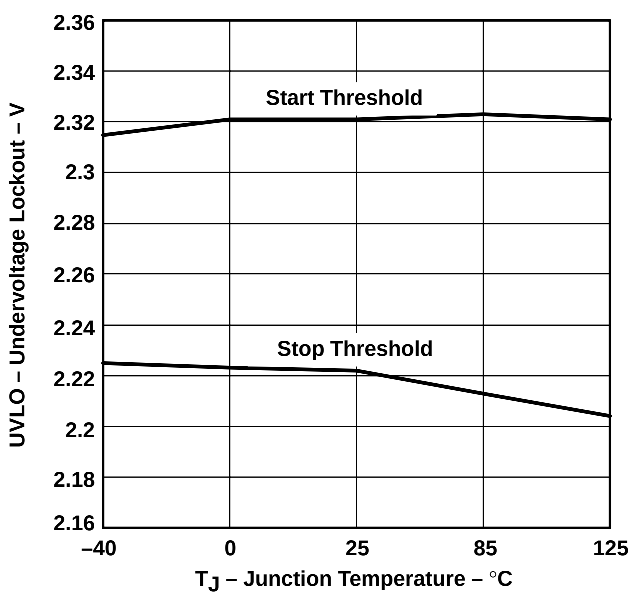


Figure 22

**CURRENT LIMIT RESPONSE
vs
PEAK CURRENT**

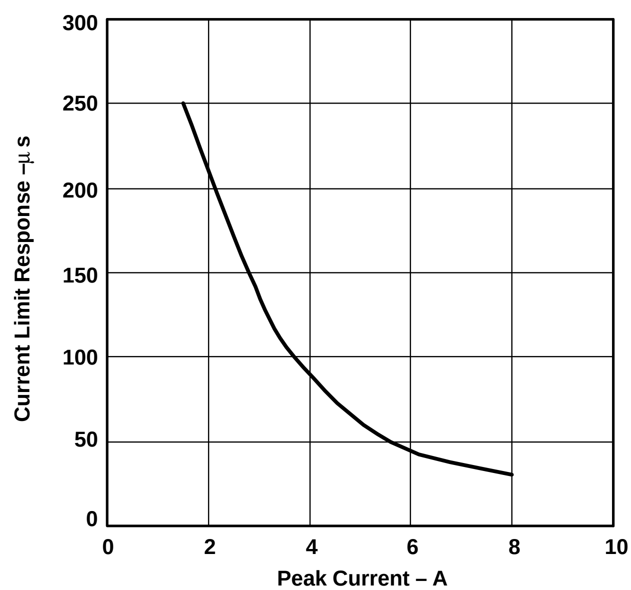


Figure 23

APPLICATION INFORMATION

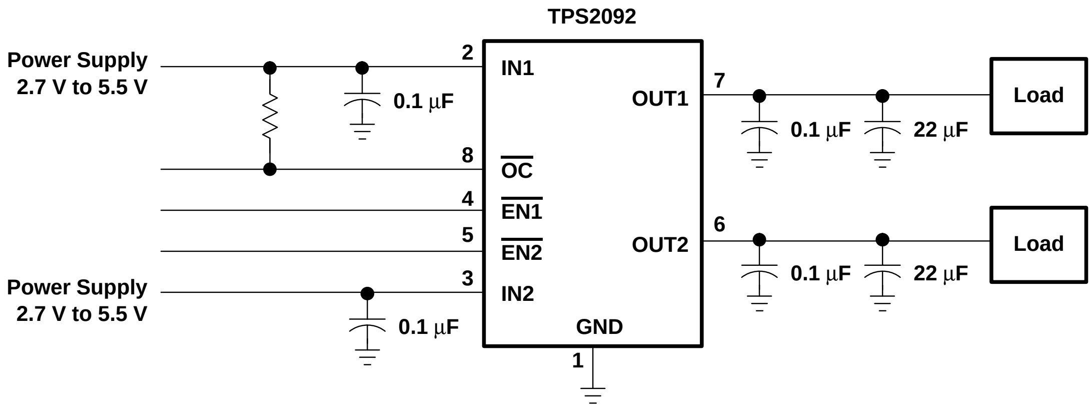


Figure 24. Typical Application

power-supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS209x senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figure 10 and 11). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 8). The TPS209x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. The TPS209x devices are designed to reduce false overcurrent reporting. An internal overcurrent transient filter eliminates the need to use external components to remove unwanted pulses. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

$\overline{OC}$ response (continued)

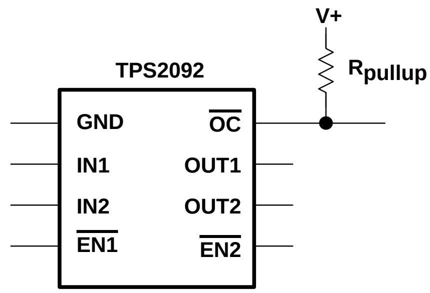


Figure 25. Typical Circuit for $\overline{OC}$ Pin

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the total number of switches being used, to get the total power dissipation coming from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W (for 8 pin), 111°C/W (for 16 pin)
P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS209x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

APPLICATION INFORMATION

thermal protection (continued)

The TPS209x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{\text{OC}}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

generic hot-plug applications (see Figure 26)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS209x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS209x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

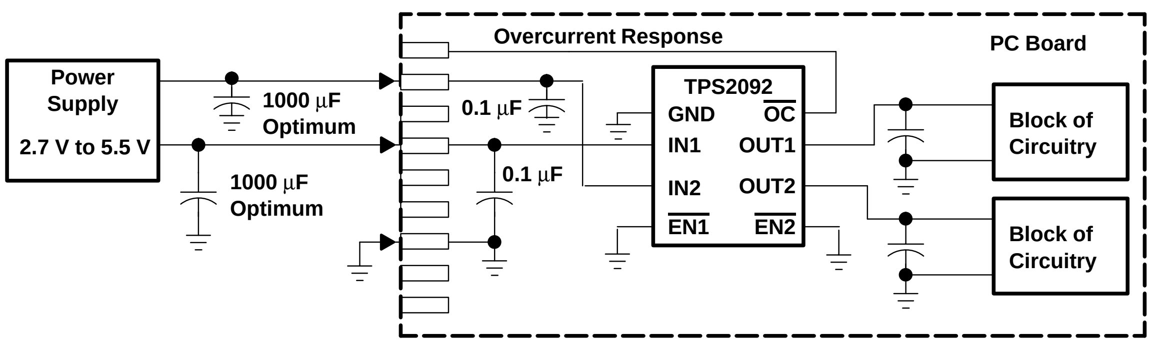


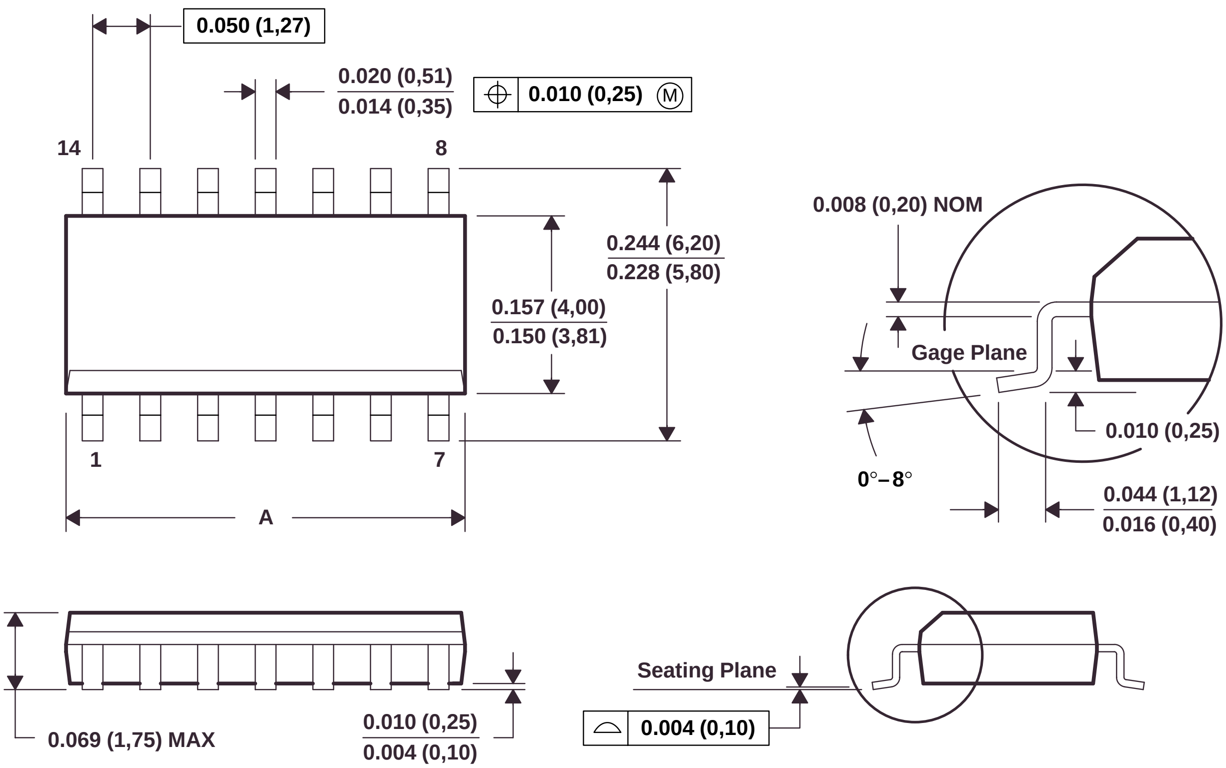
Figure 26. Typical Hot-Plug Implementation

By placing the TPS209x between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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