agere systems

Product Brief
September 2001

TETH0110G 10 Gbit/s Ethernet Serial LAN PHY

Overview

The TETH0110G is a physical layer device that implements the physical coding sublayer (PCS) and physical media attachment (PMA) functions for an *IEEE*® 802.3ae 10 Gbit/s Ethernet serial local area network (LAN) PHY. This device includes many features optimized for XENPAK optical modules. At the system interface (host or switch), the TETH0110G supports 10 Gbit attachment unit interface (XAUI) chip-to-chip interconnects. At the line interface, TETH0110G provides 10.3125 Gbits/s serial I/Os to interface directly to the laser driver and optical receiver. The TETH0110G has a 10 GHz clock output, an internal limiting amplifier, a LASI-Link alarm status interrupt, and a serial interface to an external electrically erasable programmable read-only memory (EEPROM). The TETH0110G is designed using low-power, 0.16 µm SiGe technology and operates from 3.3 V and 1.5 V power supplies.

Features

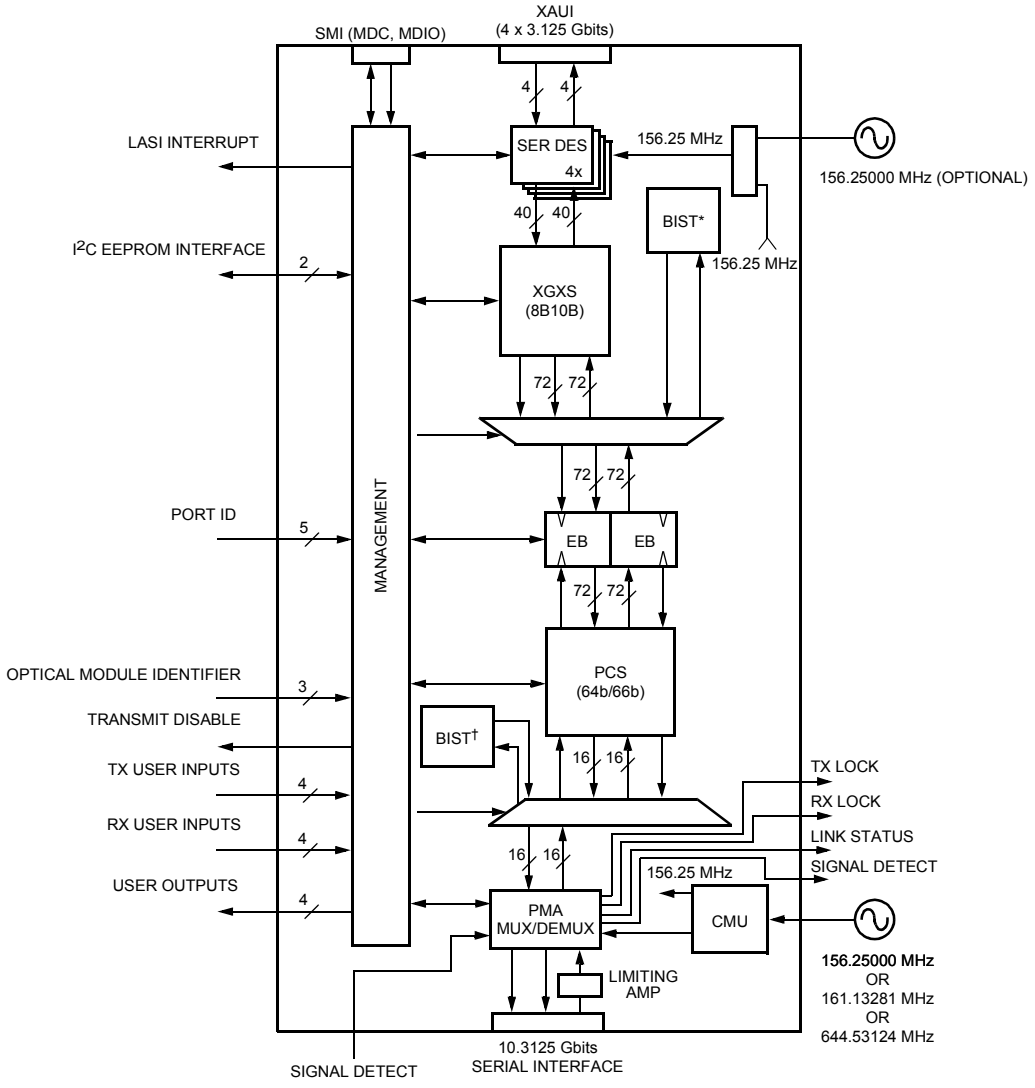
- Designed for *IEEE* 802.3ae standard, serial LAN PHY.
- Designed for XENPAK multisource agreement (MSA) specification.
- Designed for XGP MSA specification.
- 10GBASE-R PMA functions:
  - — Integrated 10.3125 Gbit/s serializer/deserializer.
  - — 10 GHz clock output, when combined with a clocked laser driver it eliminates data dependent jitter.
  - — Serial data loopback.
  - — Loss of lock indicator.
  - — Low output jitter.
- 10GBASE-R PCS and PMA functions:
  - — 64b/66b encoder/decoder.
  - — $x^{59} + x^{39} + 1$ scrambler with bypass.
  - — 66:16 gearbox.
  - — Loopback mode for system test.
- XAUI high-speed, low pin-count, long-reach interface:
  - — Four differential transmit (TX) pairs.
  - — Four differential receive (RX) pairs.
  - — 3.125 Gbits/s per lane.
  - — 8b/10b encoder/decoder.
  - — Low jitter output.
  - — Lane-by-lane synchronization function.
  - — Lane deskew function.
  - — Randomized idle pattern for reduced electromagnetic interface (EMI).
  - — Loopback mode for systems test.

Features (continued)

- Elastic buffers between XAUI macro and 64b/66b macro for jitter removal and clock tolerance compensation.
- Serial management interface:
  — Management data clock (MDC) and management data input/output (MDIO).
  — Support applicable serial LAN register set defined in *IEEE* 802.3ae clause 45.
- Serial I^2C EEPROM interface:
  — Supports serial interface to external EEPROM so that data can be downloaded into the TETH0110G registers and read by the standard serial management interface.
  — Supports any other standard I^2C interface peripherals such as: analog to digital converters and temperature monitors.
- Provides link alarm status interrupt output.
- Provides user-defined I/O pins with corresponding user-defined registers:
  — Simplifies interface to optical module.
- Optical module interface signals:
  — TX_DISABLE output.
  — Signal detect input.
- Flexible external reference clock input frequencies of 156.25 MHz, 161.1328 MHz, or 644.53124 MHz. Includes internal clock multiplier unit to generate other clock frequencies.
- Built-in limiting amplifier function, no external limiting amplifier needed.
- Built-in self-test modes, simplifies system diagnostics:
  — Packet data generator and error checker, for function testing of chip, module, or module-to-module.
  — Pseudorandom data generator and error checker for 10 Gbit testing.
- XAUI and 10.3125 Gbit/s loopback modes.
- Packaged in a 19 mm x 19 mm 324-ball plastic ball grid array (PBGA).
- Power supplies:
  — 3.3 V and 1.5 V for low power dissipation.

Description

Block Diagram



* This is a packet generator and checker.

† This is a pseudorandom data generator and checker.

Figure 1. TETH0110G Block Diagram

Description (continued)

Functional Block Diagram

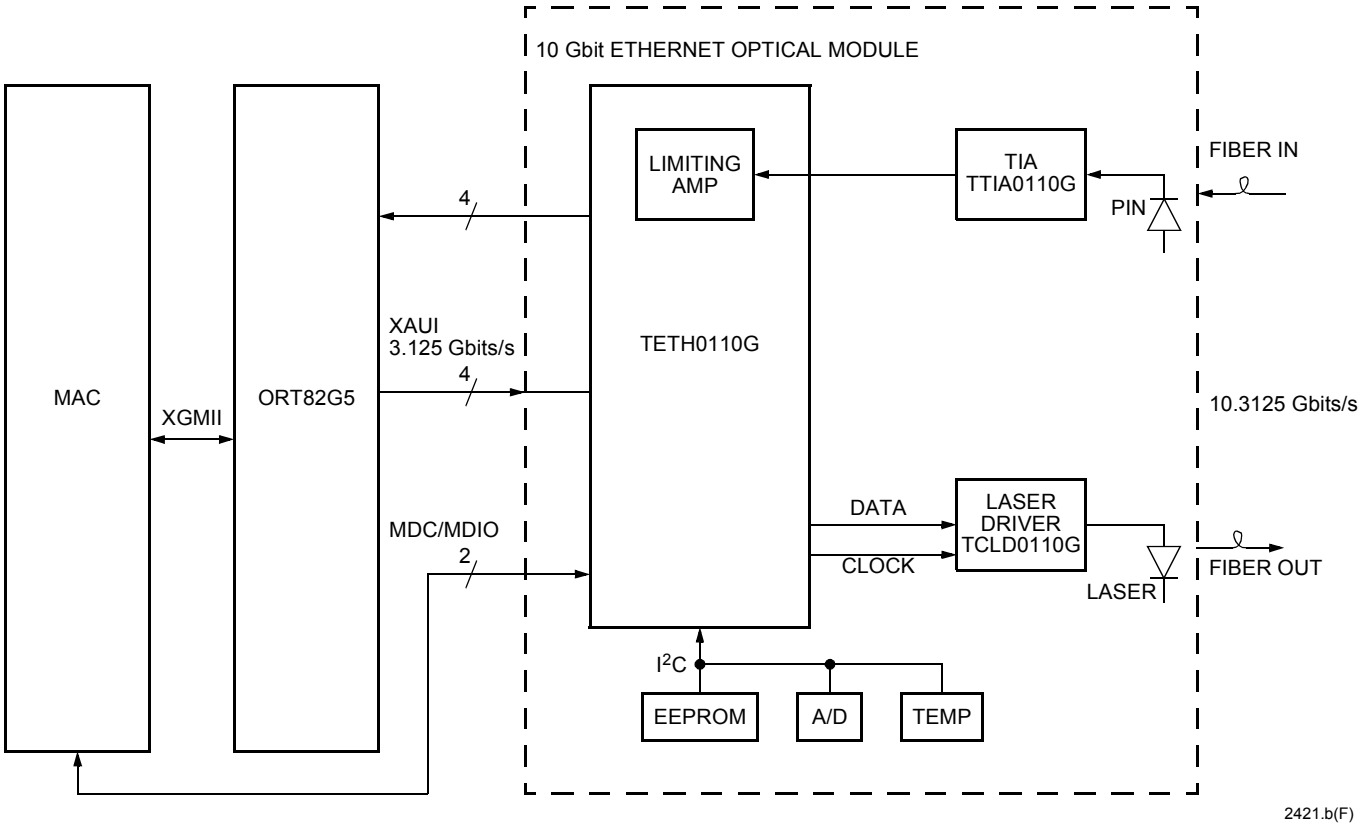


Figure 2. TETH0110G Functional Block Diagram

TETH0110G is a low-power, 0.16 µm SiGe physical layer IC for *IEEE* 802.3ae applications. The TETH0110G can be used in a 10 Gbit/s Ethernet serial LAN optical module or on a line card. The TETH0110G includes: a XAUI interface, a 10 Gbit extender sublayer (XGXS) 8b/10b encoder/decoder, a PCS elastic buffer and 64b/66b encoder/decoder, and a 10.3125 Gbits/s serial PMA and management interface. A single 156.25 MHz, 161.1328 MHz, or 644.53124 MHz clock input is required. An on-chip clock multiplier unit is utilized to generate all of the required internal frequencies. The 10.3125 GHz serial receiver input includes a built-in limiting amplifier to eliminate the need for a separate limiting amplifier in many applications. The TETH0110G includes a built-in self test capability to simplify module testing and system testing.

XAUI Interface

The XAUI interface is comprised of a quad serializer/deserializer (SERDES) and the XGXS block. The interface to the media access control (MAC) or switch controller uses the XAUI interface. XAUI is a low pin count (four differential pairs) alternative for the pin intensive (32-bit bus) 10 Gbit media independent interface (XGMII). This is a four lane wide 3.125 GHz, ac coupled, differential, 8b/10b encoded interface. XAUI extends the interconnect between TETH0110G and the host to be up to 20 in. using standard low-cost FR-4 printed wiring board material. The XAUI block includes: lane-by-lane synchronization and deskewing, idle symbol randomizer, 8b/10b encoder/decoder, and internal loopback function.

Description (continued)

Physical Coding Sublayer (PCS) Block

The PCS block provides connectivity between the XAUI and the multiplexer/demultiplexer (MUX/deMUX). It also provides 64b/66b encoding/decoding of eight data octets and converts the data in a gear box to a 16-bit wide bus for the MUX/deMUX. The PCS also determines when a functional link has been established.

Physical Media Attachment (PMA) Block

The PMA block is comprised of a 10.3125 Gbit/s MUX/deMUX. The built-in limiting amplifier accepts signals directly from a transimpedance amplifier. The function of this block is to convert from a 10.3125 Gbits/s differential CML serial data stream to a 16-bit wide data stream for the PCS to process. The MUX provides a serial differential 10.3125 Gbits/s data output and a 10.3125 GHz differential clock output for clocked laser drivers. The deMUX provides a loss-of-lock indication.

Clock Multiplier Unit (CMU)

The TETH0110G provides an internal clock multiplier block to generate all of the required internal frequencies. An external 156.25 MHz, 161.1328 MHz, or 644.53124 MHz input is needed to the CMU. The CMU will generate the 10.3125 GHz clock for the MUX/deMUX, 156.25 MHz clock required by the XAUI block as well as all other internally required clocks.

Built-in Self Test (BIST)

Several built-in self test features have been included in this device. The XAUI block includes a BIST packet generator and error checker as well as an internal loopback mode. The PCS block provides a BIST pseudo-random bit sequence (PRBS) data generator for 10 Gbit/s jitter testing. A 10.3125 Gbit/s serial data loopback is also provided.

Serial Management Interface

The TETH0110G provides an *IEEE* 802.3ae clause 45 standard management interface. A serial EEPROM interface is also provided so that 256 bytes of EEPROM data that can be downloaded into the TETH0110G register space. The serial management interface can then be used to read this data out of the device.

Agere Systems 10 Gbit Ethernet System Solution

The TETH0110G combined with the TMOD0110G 10 Gbit modulator/laser driver, the TTIA0110G 10 Gbit transimpedance amplifier, the ORT82G5 field programmable gate array with XGMII to XAUI port, and a 10 Gbit Ethernet media access control (EMAC), will make Agere's optical receiver and transmitter provide an end-to-end 10 Gbit Ethernet systems solution.

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