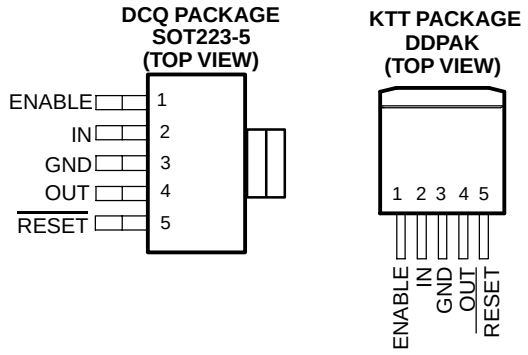
# LOW INPUT VOLTAGE, 1-A LOW-DROPOUT LINEAR REGULATORS WITH SUPERVISOR

## FEATURES

- **1-A Output Current**
- **Available in 1.5-V, 1.6-V, 1.8-V, 2.5-V Fixed-Output (For Adjustable Versions Refer to TPS72501)**
- **Input Voltage Down to 1.8 V**
- **Low 170-mV Dropout Voltage at 1 A (TPS72625)**
- **Stable With Any Type/Value Output Capacitor**
- **Integrated Supervisor (SVS) With 200-ms $\overline{\text{RESET}}$ Delay Time**
- **Low 210-μA Ground Current at Full Load (TPS72625)**
- **Less than 1-μA Standby Current**
- **±2% Output Voltage Tolerance Over Line, Load, and Temperature (–40°C to 125°C)**
- **Integrated UVLO**
- **Thermal and Overcurrent Protection**
- **5-Lead SOT223–5 or DDPAK Surface Mount Package**

## APPLICATIONS

- **PCI Cards**
- **Modem Banks**
- **Telecom Boards**
- **DSP, FPGA, and Microprocessor Power Supplies**
- **Portable, Battery Powered Applications**




Note: Tab is GND for both packages

## DESCRIPTION

The TPS726xx family of 1-A low-dropout (LDO) linear regulators has fixed voltage options available that are commonly used to power the latest DSPs, FPGAs, and microcontrollers. The integrated supervisory circuitry provides an active low $\overline{\text{RESET}}$ signal when the output falls out of regulation. The no capacitor/any capacitor feature allows the customer to tailor output transient performance as needed. Therefore, compared to other regulators capable of providing the same output current, this family of regulators can provide a stand alone power supply solution or a post regulator for a switch mode power supply.

These regulators are ideal for higher current applications. The family operates over a wide range of input voltages (1.8 V to 6 V) and has very low dropout (170 mV at 1-A).

Ground current is typically 210 μA at full load and drops to less than 80 μA at no load. Standby current is less than 1 μA.

Each regulator option is available in either a SOT223–5 or DDPAK package. With a low input voltage and properly heatsinked package, the regulator dissipates more power and achieves higher efficiencies than similar regulators requiring 2.5 V or more minimum input voltage and higher quiescent currents. These features make it a viable power supply solution for portable, battery powered equipment.

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-μF output capacitor.

Unlike some regulators that have a minimum current requirement, the TPS726 family is stable with no output load current. The low noise capability of this family, coupled with its high current operation and ease of power dissipation, make it ideal for telecom boards, modem banks, and other noise sensitive applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_J$ | VOLTAGE(1)(4) | SOT223–5(2) | SYMBOL | DDPAK(3) | SYMBOL |
|---|---|---|---|---|---|
| –40°C to 125°C | 1.5 V | TPS72615DCQ | PS72615 | TPS72615KTT | TPS72615 |
| | 1.6 V | TPS72616DCQ | PS72616 | TPS72616KTT | TPS72616 |
| | 1.8 V | TPS72618DCQ | PS72618 | TPS72618KTT | TPS72618 |
| | 2.5 V | TPS72625DCQ | PS72625 | TPS72625KTT | TPS72625 |

(1) Other voltage options are available upon request from the manufacturer.
(2) To order a taped and reeled part, add the suffix R to the part number (e.g., TPS72151DCQR).
(3) To order a taped and reeled part, add the suffix T to the part number (e.g., TPS72615KTTT).
(4) Refer to TPS72501 for adjustable version.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | UNIT |
|---|---|---|
| Input voltage, $V_I$(2) | –0.3 to 7 | V |
| Voltage range at EN, FB | –0.3 to $V_I$ + 0.3 | V |
| Voltage on OUT, $\overline{\text{RESET}}$ | 6 | V |
| ESD rating, HBM | 2 | kV |
| Continuous total power dissipation | See Dissipation Rating Table | |
| Operating junction temperature range, $T_J$ | –50 to 150 | °C |
| MAximum junction temperature range, $T_J$ | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 to 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Input voltage, $V_I$(1) | 1.8 | | 6 | V |
| Continuous output current, $I_O$ | 0 | | 1 | A |
| Operating junction temperature, $T_J$ | –40 | | 125 | °C |

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}(max^load)$

## PACKAGE DISSIPATION RATINGS

| PACKAGE | BOARD | $R_{\theta JC}$ | $R_{\theta JA}$ |
|---|---|---|---|
| DDPAK | High K(1) | 2 °C/W | 23 °C/W |
| SOT223 | Low K(2) | 15 °C/W | 53 °C/W |

(1) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), two-layer board with 2 ounce copper traces on top of the board.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, $I_O$= 1 mA, EN = IN, $C_o$ = 1 µF, $C_i$ = 1 µF(unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | Bandgap voltage reference | | | | 1.177 | 1.220 | 1.263 | V |
| $V_O$ | Output voltage | TPS72615 | $T_J$ = 25°C | | | 1.5 | | V |
| | | | 0 µA< $I_O$ < 1 A | 1.8 V ≤ $V_I$ ≤ 5.5 V | 1.47 | | 1.53 | |
| | | TPS72616 | $T_J$ = 25°C | | | 1.6 | | |
| | | | 0 µA< $I_O$ < 1 A | 2.6 V ≤ $V_I$ ≤ 5.5 V | 1.568 | | 1.632 | |
| | | TPS72618 | $T_J$ = 25°C | | | 1.8 | | |
| | | | 0 µA< $I_O$ < 1 A | 2.8 V ≤ $V_I$ ≤ 5.5 V | 1.764 | | 1.836 | |
| | | TPS72625 | $T_J$ = 25°C | | | 2.5 | | |
| | | | 0 µA< $I_O$ < 1 A | 3.5 V ≤ $V_I$ ≤ 5.5 V | 2.45 | | 2.55 | |
| I | Ground current | | $I_O$ = 0 µA | | | 75 | 120 | µA |
| | | | $I_O$ = 1 A | | | 210 | 300 | |
| | Standby current | | EN < 0.4 V | $T_J$ = 25°C | | 0.2 | | µA |
| | | | EN < 0.4 V | | | | 1 | |
| $V_n$ | Output noise voltage | | BW = 200 Hz to 100 kHz, $T_J$ = 25°C, | $C_o$ = 10 µF, $I_O$ = 1 mA | | 150 | | µV |
| PSRR | Ripple rejection | | f = 1 kHz, $C_o$ = 10 µF, | $T_J$ = 25°C | | 60 | | dB |
| | Current limit(1) | | | | 1.1 | 1.6 | 2.3 | A |
| | Output voltage line regulation ($\Delta V_O/V_O$)(2) | | $V_O$ + 1 V < $V_I$ ≤ 5.5 V | | –0.15 | 0.02 | 0.15 | %/V |
| | Output voltage load regulation | | 0 µA< $I_O$ < 1 A | | –0.25 | 0.05 | 0.25 | %/A |
| $V_{IH}$ | EN high level input | | | | 1.3 | | | V |
| $V_{IL}$ | EN low level input | | | | –0.2 | | 0.4 | |
| $I_I$ | EN input current | | EN = 0 V or $V_I$ | | | 0.01 | 100 | nA |
| | UVLO threshold | | $V_{CC}$ rising | | 1.45 | 1.57 | 1.70 | V |
| | UVLO hysteresis | | $T_J$ = 25°C, $V_{CC}$ rising | | | 50 | | mV |
| | UVLO deglitch | | $T_J$ = 25°C, $V_{CC}$ rising | | | 10 | | µs |
| | UVLO delay | | $T_J$ = 25°C, $V_{CC}$ rising | | | 100 | | µs |

(1) Test condition includes, output voltage $V_O = V_O$ – 15% and pulse duration = 10 ms.
(2) $V_{Imin} = (V_O + 1)$ or 1.8 V whichever is greater.

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(5.5\ V - V_{Imin}\right)}{100} \times 1000$$

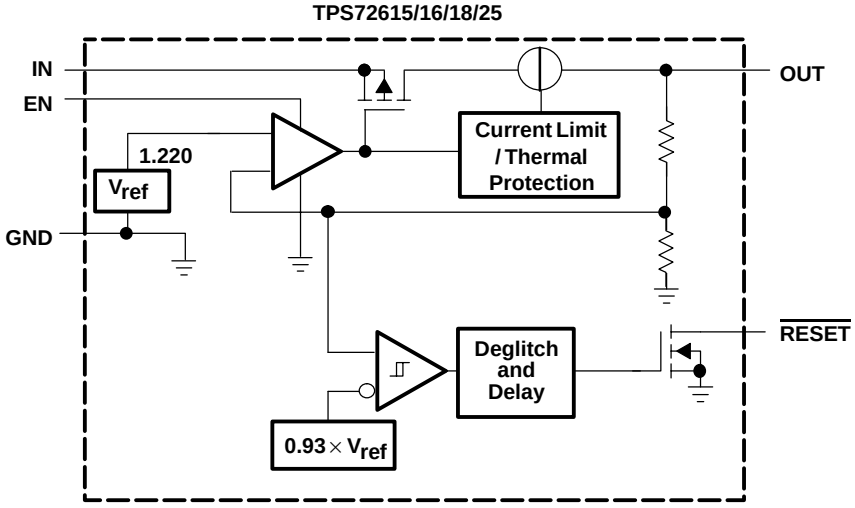
## ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, $I_O$= 1 mA, EN = IN, $C_O$ = 1 µF, $C_i$ = 1 µF(unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{DO}$ | Dropout voltage | TPS72625(1) | $I_O$ = 1 A | $T_J$ = 25°C | | 170 | | mV |
| | | | $I_O$ = 1 A | | | | 280 | |
| | | TPS72618(1) | $I_O$ = 1 A | $T_J$ = 25°C | | 210 | | |
| | | | $I_O$ = 1 A | | | | 320 | |
| $\overline{RESET}$ | Minimum input voltage for valid $\overline{RESET}$ | | | | 1.3 | | | V |
| | Trip threshold voltage | | | | 90 | 93 | 96 | %$V_O$ |
| | Hysteresis voltage | | | | | 10 | | mV |
| | $t_{(RESET)}$ delay time | | | | 100 | 200 | 300 | ms |
| | Rising edge deglitch | | | | | 10 | | µs |
| | Output low voltage (at 700 µA) | | | | –0.3 | | 0.4 | V |
| | Leakage current | | | | | | 100 | nA |

(1) Dropout voltage is defined as the differential voltage between $V_O$ and $V_I$ when $V_O$ drops 100 mV below the value measured with $V_I = V_O + 1$ V.

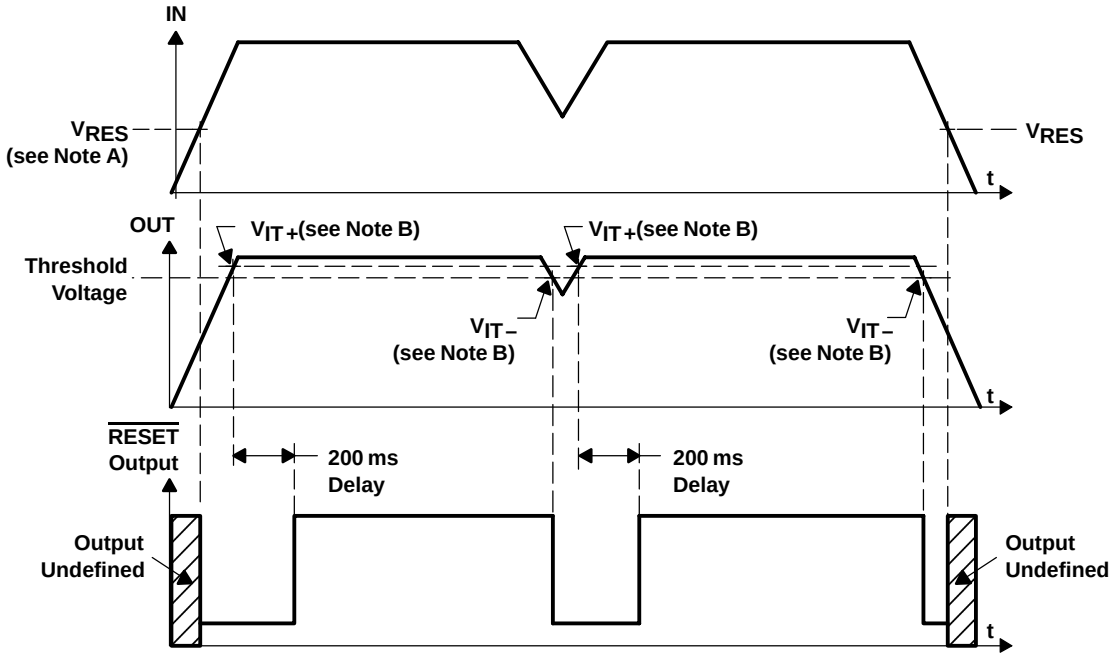
## FUNCTIONAL BLOCK DIAGRAM




### Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| GND | 3 | | Ground |
| ENABLE | 1 | I | Enable input |
| IN | 2 | I | Input supply voltage |
| $\overline{RESET}$ | 5 | O/I | This terminal is the $\overline{RESET}$ output terminal. When used with a pullup resistor, this open-drain output provides the active low $\overline{RESET}$ signal when the regulator output voltage drops more than 5% below its nominal output voltage. The $\overline{RESET}$ delay time is typically 200 ms. |
| OUT | 4 | O | Regulated output voltage |

## $\overline{\text{RESET}}$ TIMING DIAGRAM




NOTES:A. $V_{RES}$ is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol $V_{RES}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. $V_{IT}$ –Trip voltage is typically 7% lower than the output voltage (93%$V_O$) $V_{IT-}$ to $V_{IT+}$ is the hysteresis voltage.

## TYPICAL CHARACTERISTICS

**TPS72618**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

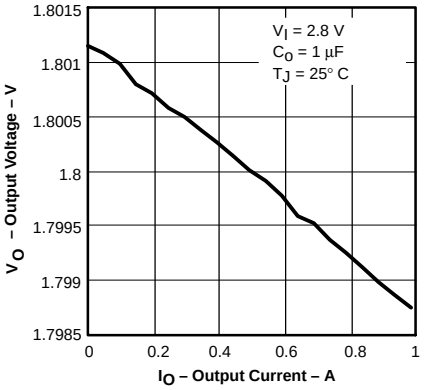



Figure 1

**TPS72618**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

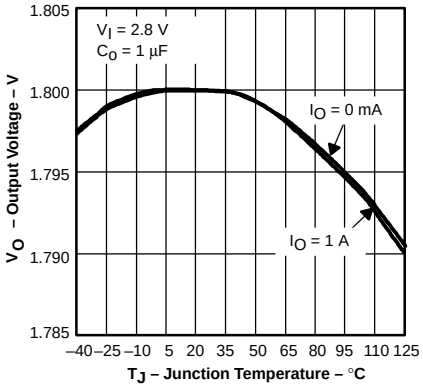



Figure 2

**TPS72618**
**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**

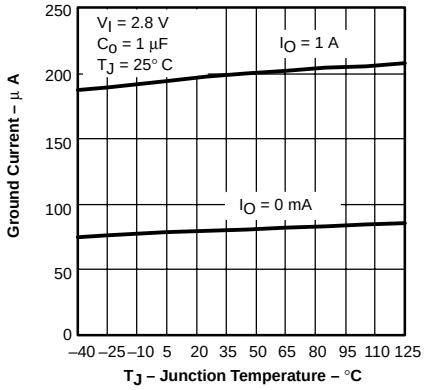



Figure 3

TPS72618
GROUND CURRENT
vs
OUTPUT CURRENT

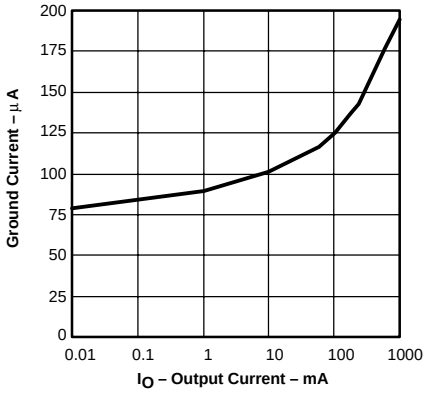



Figure 4

TPS72625
DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

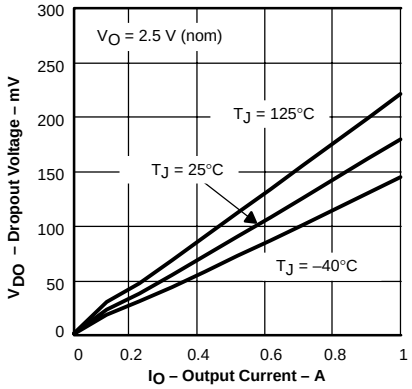



Figure 5

TPS72618
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

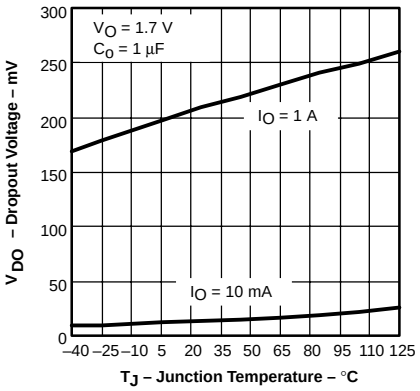



Figure 6

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

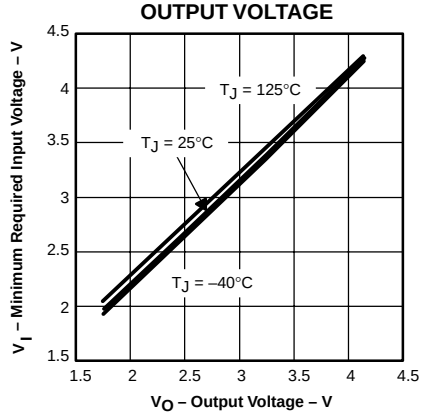



Figure 7

TPS72618
LINE TRANSIENT RESPONSE

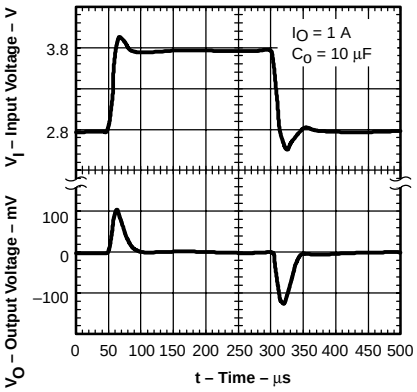



Figure 8

TPS72618
LOAD TRANSIENT RESPONSE

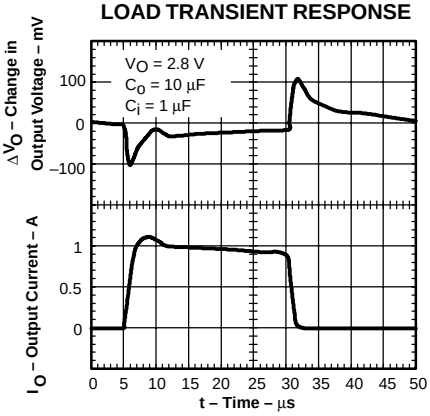



Figure 9

TPS72618
LOAD TRANSIENT RESPONSE

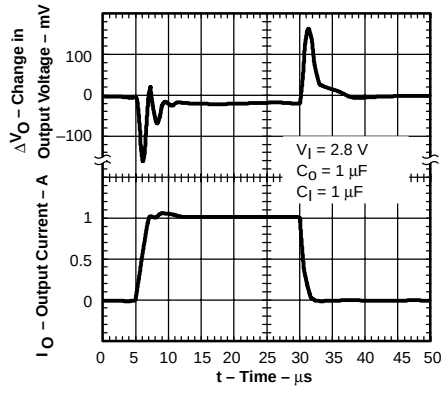



Figure 10

TPS72618
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

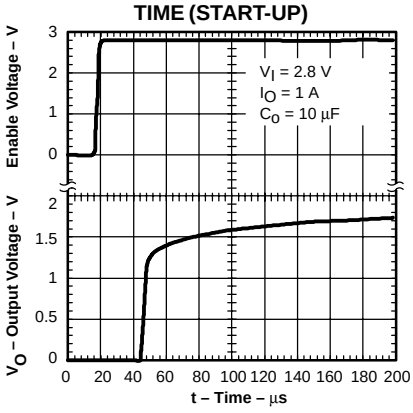



Figure 11

TPS72618
POWER UP/POWER DOWN

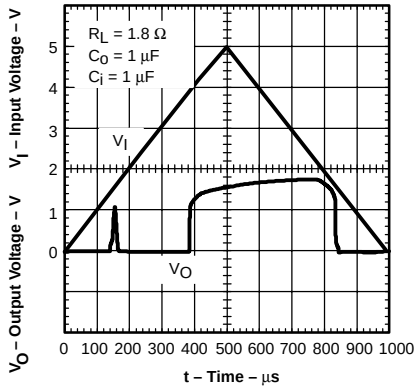



Figure 12

**TPS72618**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**

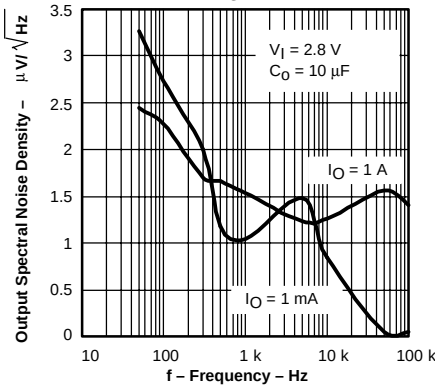



**Figure 13**

**OUTPUT IMPEDANCE**
**vs**
**FREQUENCY**

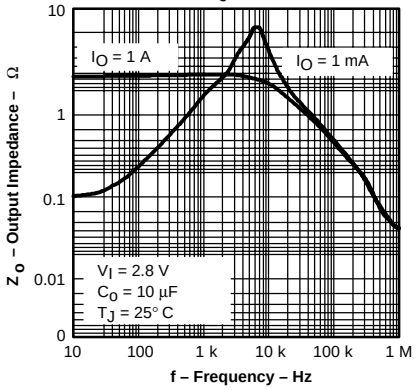



**Figure 14**

**TPS72618**
**RIPPLE REJECTION**
**vs**
**FREQUENCY**

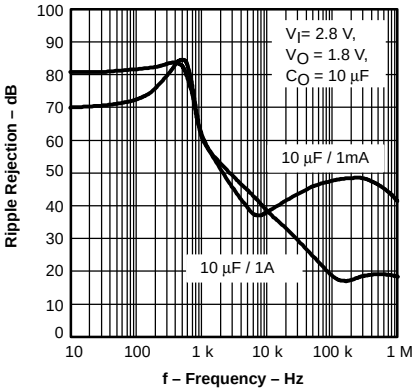



**Figure 15**

**CURRENT LIMIT**
**vs**
**INPUT VOLTAGE**

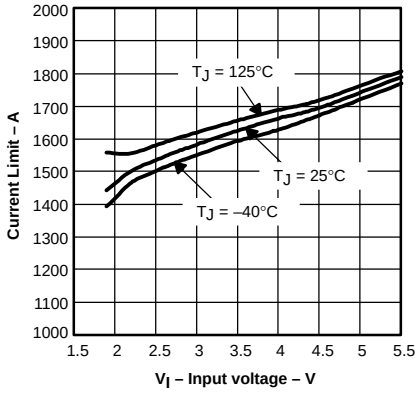



**Figure 16**

**TPS72615**
**GROUND CURRENT**
**vs**
**INPUT VOLTAGE**

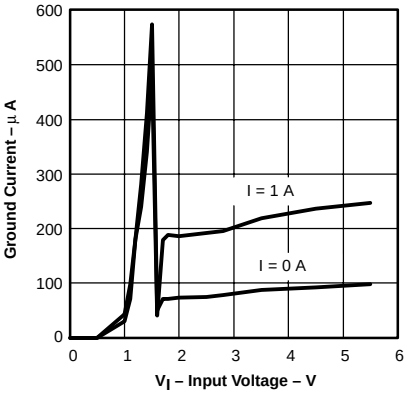



**Figure 17**

**DROPOUT VOLTAGE**
**vs**
**INPUT VOLTAGE**

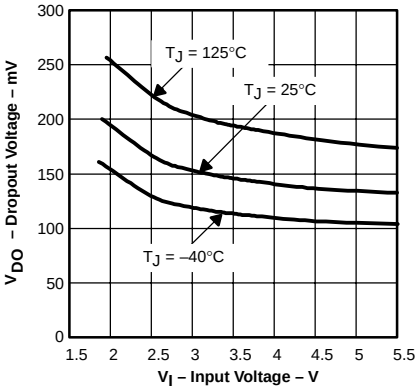



**Figure 18**

## APPLICATION INFORMATION

The TPS726xx family of low-dropout (LDO) regulators have numerous features that make it apply to a wide range of applications. The family operates with very low input voltage (≥1.8 V) and low dropout voltage (typically 200 mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. Both the active low $\overline{\text{RESET}}$ and 1-A output current, make the TPS726xx family ideal for powering processor and FPGA supplies. The TPS726xx family also has low output noise (typically 150 $\mu V_{RMS}$ with 10-μF output capacitor), making it ideal for use in telecom equipment.

## EXTERNAL CAPACITOR REQUIREMENTS

A 1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS725xx, is required for stability. To improve transient response, noise rejection, and ripple rejection, an additional 10-μF or larger, low ESR capacitor is recommended. A higher-value, low ESR input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.8 V is used.

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-μF output capacitor.

## REGULATOR PROTECTION

The TPS726xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS726xx also features internal current limiting and thermal protection. During normal operation, the TPS726xx limits output current to approximately 1.6 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 145°C, regulator operation resumes.

## THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature ($T_J$) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D\text{max} = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \quad (3)$$

Where:

$V_{I(avg)}$ is the average input voltage.

$V_{O(avg)}$ is the average output voltage.

$I_{O(avg)}$ is the average output current.

$I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature ($T_A$) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 19 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

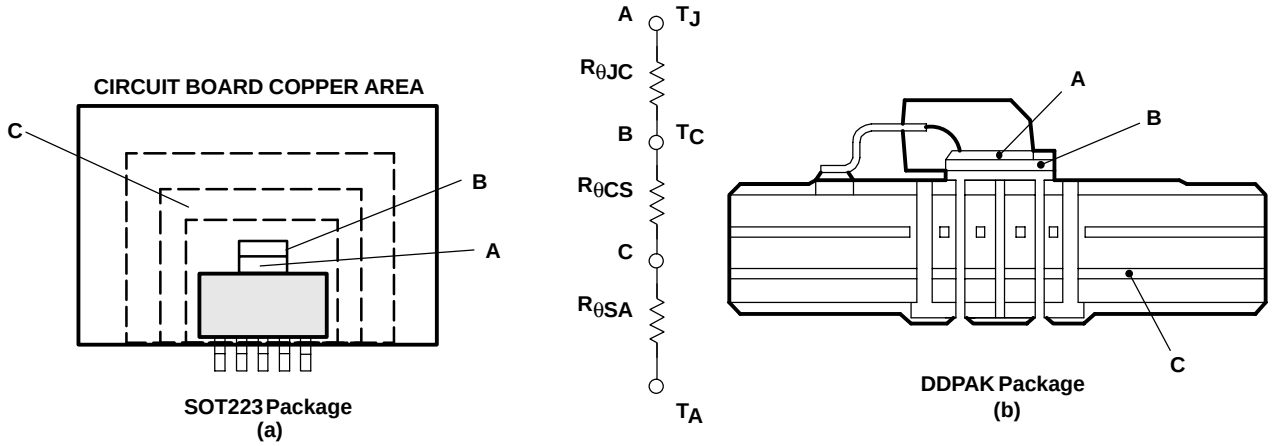



**Figure 19. Thermal Resistances**

## THERMAL INFORMATION

Equation 4 summarizes the computation:

$$T_J = T_A + P_D\text{max} \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (4)$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 4 simplifies into equation 5:

$$T_J = T_A + P_D\text{max} \times R_{\theta JA} \quad (5)$$

Rearranging equation 5 gives equation 6:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D\text{max}} \quad (6)$$

Using equation 5 and the computer model generated curves shown in Figure 20 and Figure 23, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

## THERMAL INFORMATION

### DDPAK POWER DISSIPATION

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

To illustrate, the TPS72625 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (5 - 2.5)\ \text{V} \times 1\ \text{A} = 2.5\ \text{W} \quad (7)$$

Substituting $T_J\text{max}$ for $T_J$ into equation 6 gives equation 8:

$$R_{\theta JA}\text{max} = (125 - 55)^\circ\text{C}/2.5\ \text{W} = 28^\circ\text{C/W} \quad (8)$$

From Figure 20, DDPAK Thermal Resistance vs Copper Heatsink Area, the ground plane needs to be 1 $cm^2$ for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 20 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 21 shows the side view of the operating environment used in the computer model.

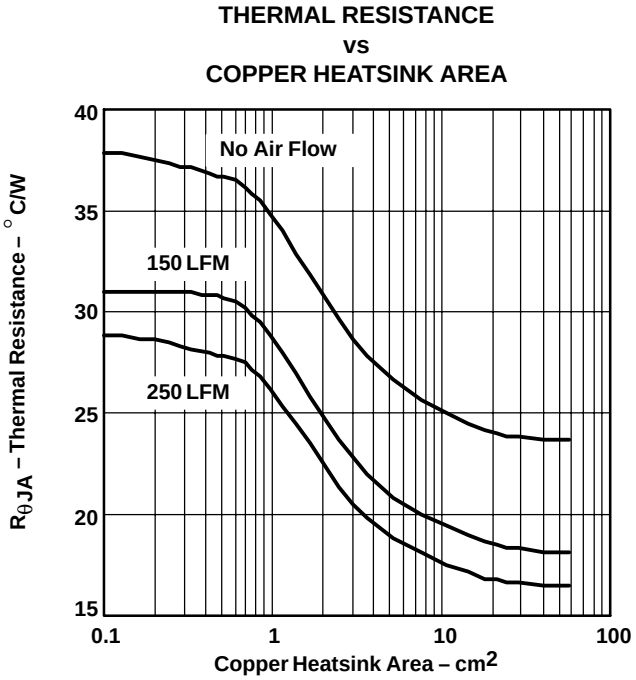



**Figure 20. DDPAK Thermal Resistance vs Copper Heatsink Area**

## THERMAL INFORMATION

### DDPAK POWER DISSIPATION (CONTINUED)

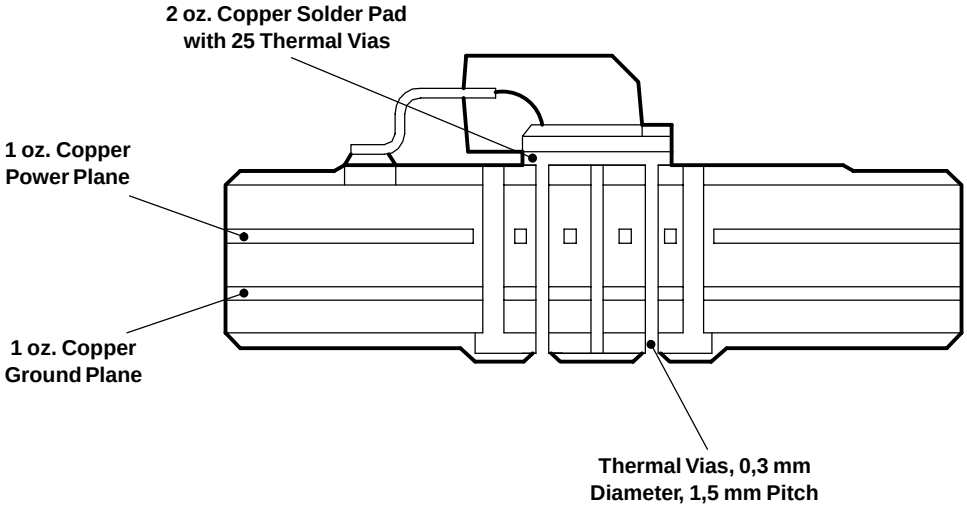



**Figure 21. DDPAK Thermal Resistance**

From the data in Figure 22 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

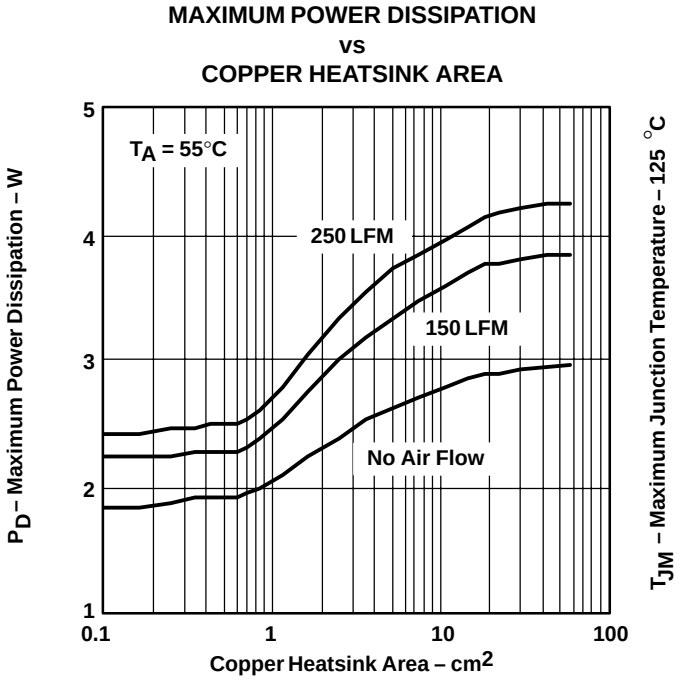



**Figure 22. Maximum Power Dissipation vs Copper Heatsink Area**

## THERMAL INFORMATION

### SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS72625 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (3.3 - 2.5)\ \text{V} \times 1\ \text{A} = 800\ \text{mW} \quad (9)$$

Substituting $T_J\text{max}$ for $T_J$ into equation 6 gives equation 10:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/800\ \text{mW} = 87.5°\text{C/W} \quad (10)$$

From Figure 23, $R_{\theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55 $in^2$ for the part to dissipate 800 mW. The operating environment used to construct Figure 23 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

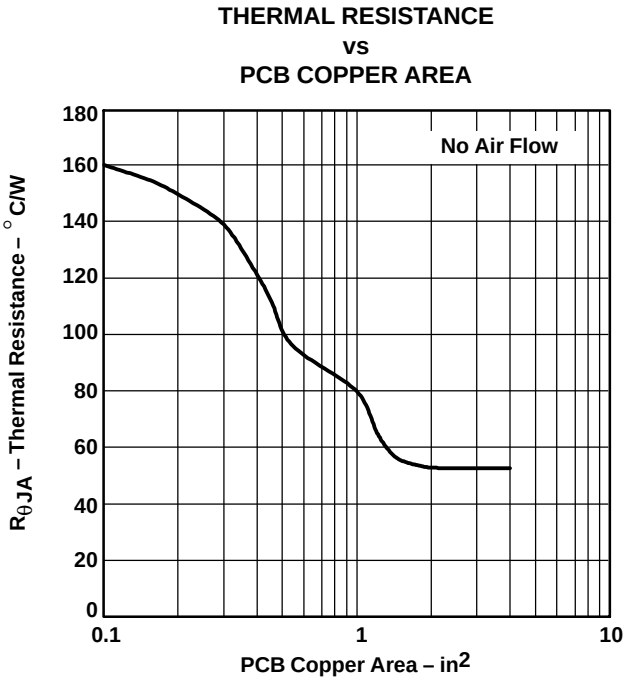



**Figure 23. SOT223 Thermal Resistance vs PCB AREA**

## THERMAL INFORMATION

### SOT223 POWER DISSIPATION (CONTINUED)

From the data in Figure 23 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 24).

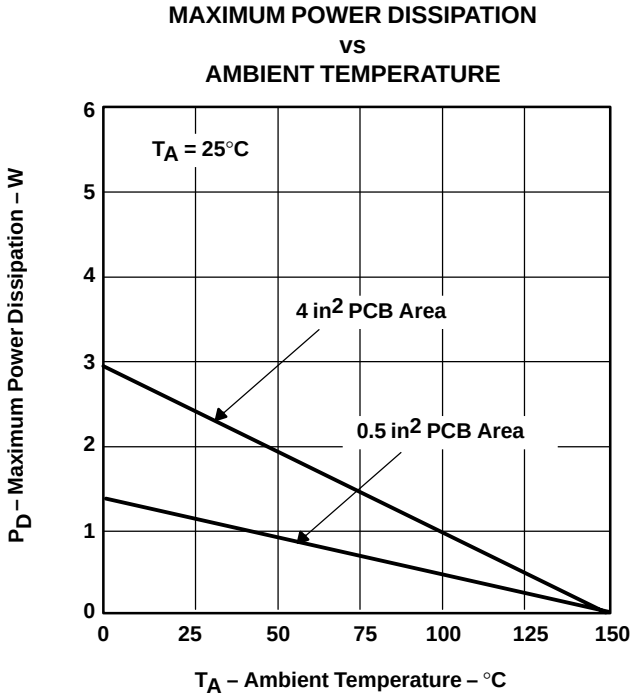
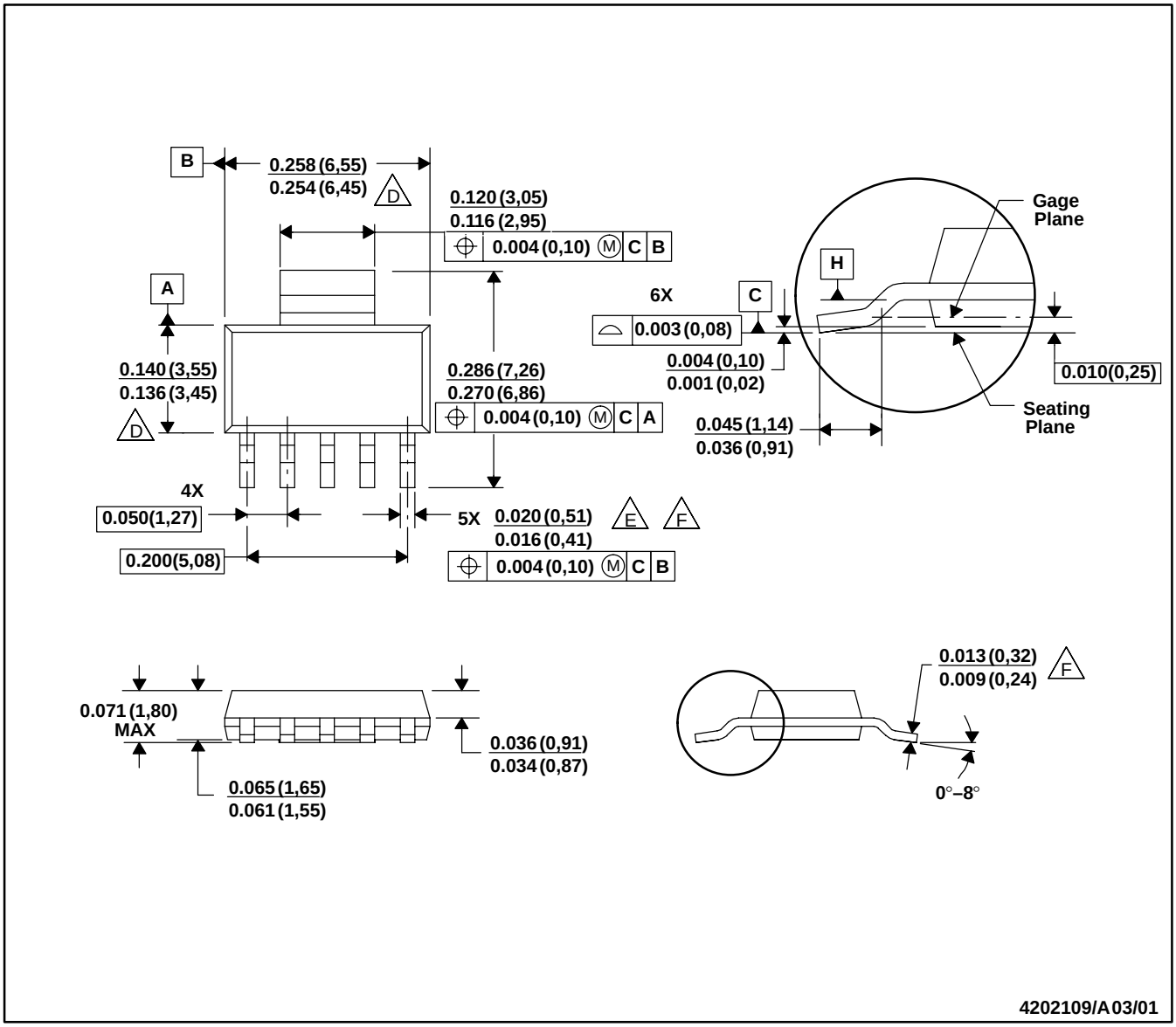



**Figure 24. SOT223 Power Dissipation**

## MECHANICAL DATA

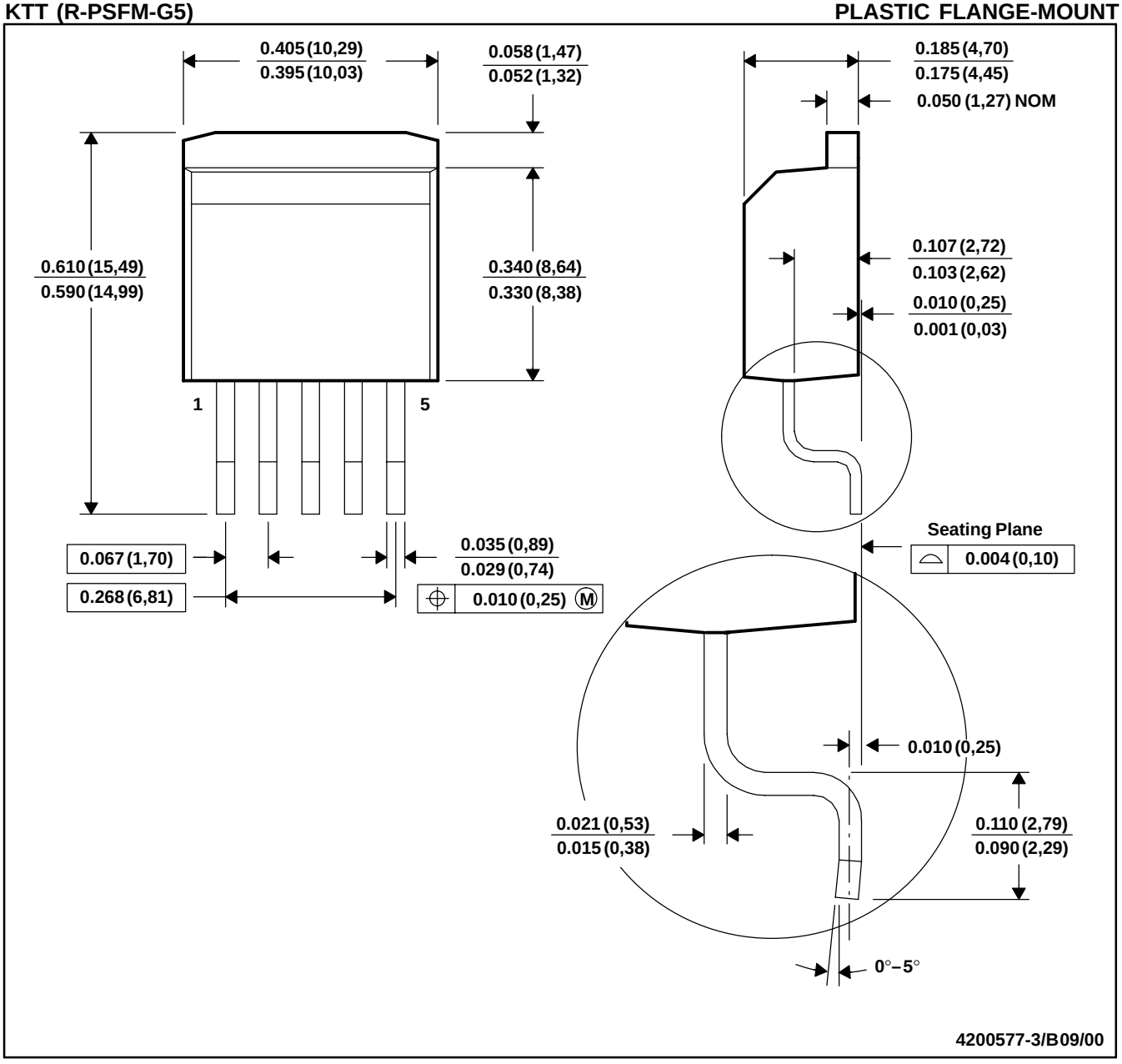
**DCQ (R-PDSO-G6)** **PLASTIC SMALL-OUTLINE**




NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches
D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
E. Lead width dimension does not include dambar protrusion.
F. Lead width and thickness dimensions apply to solder plated leads.
G. Interlead flash allow 0.008 inch max.
H. Gate burr/protrusion max. 0.006 inch.

## MECHANICAL DATA

**KTT (R-PSFM-G5)** **PLASTIC FLANGE-MOUNT**




NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

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