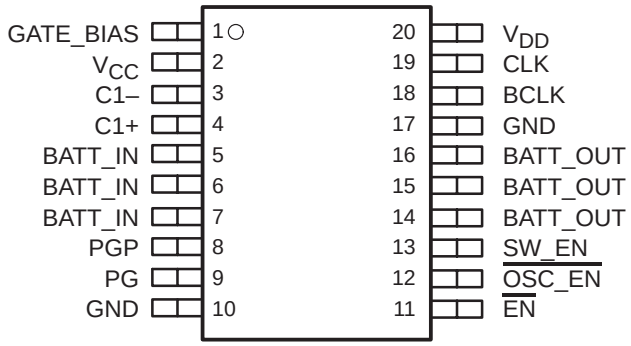
- **Charge Pump Provides Negative Gate Bias for Depletion-Mode GaAs Power Amplifiers**
- **Buffered Clock Output to Drive Additional External Charge Pump**
- **135-mΩ High-Side Switch Controls Supply Voltage to the GaAs Power Amplifier**
- **Power-Good Circuitry Prevents High-Side Switch Turn-on Until Negative Gate Bias is Present**
- **Charge Pump Can Be Driven From the Internal Oscillator or An External Clock**
- **10-μA Maximum Standby Current**
- **Low-Profile (1.2-mm Max Height), 20-Pin TSSOP Package**

PW PACKAGE
(TOP VIEW)



description

The TPS9103 is a highly integrated power supply for depletion-mode GaAs power amplifiers (PA) in cellular handsets and other wireless communications equipment. Functional integration and low-profile packaging combine to minimize circuit-board area and component height requirements. The device includes: a p-channel MOSFET configured as a high-side switch to control the application of power to the PA; a driver for the high-side switch with a logic-compatible input; a charge pump to provide negative gate-bias voltage; and logic to prevent turn-on of the high-side switch until gate bias is present. The high-side switch has a typical on-state resistance of 135 mΩ.

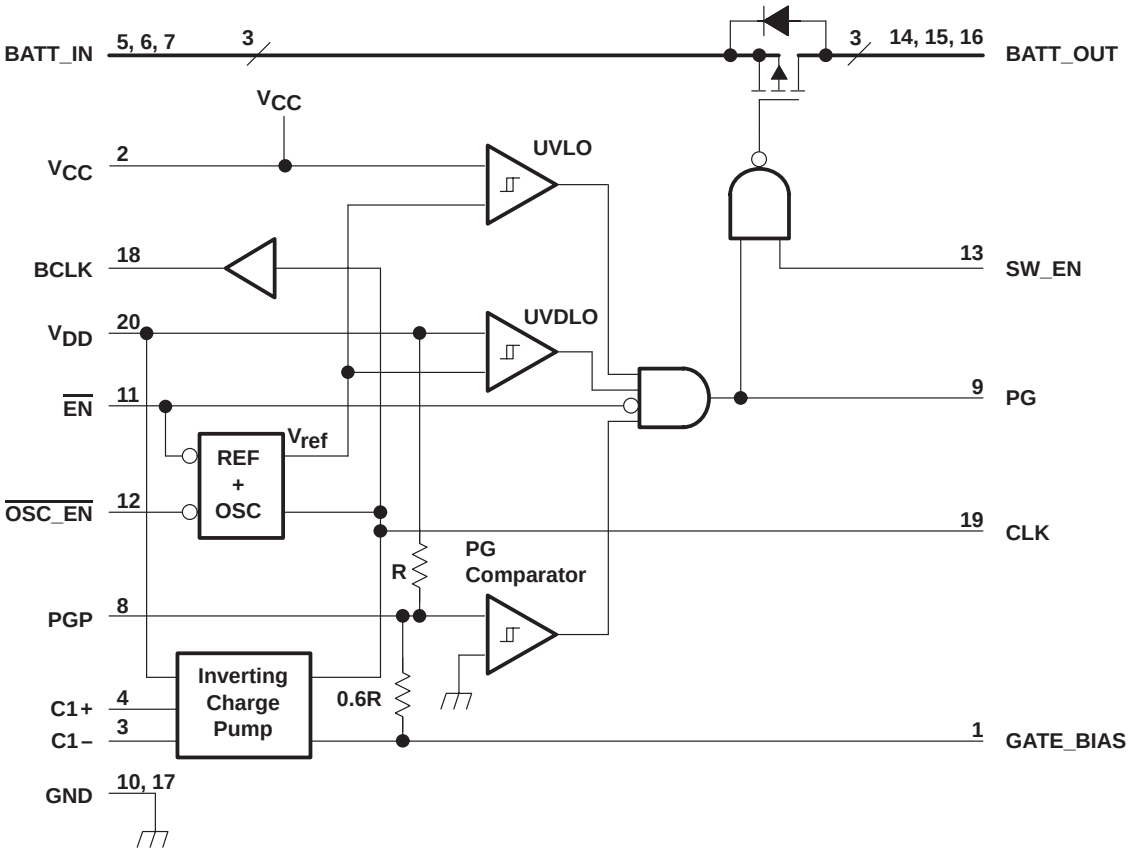
The TPS9103 is available in a 20-pin thin shrink small-outline package (TSSOP) or in chip form. Contact factory for die sales. The device operates over a junction temperature range of –25°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM (Y)
	TSS0P (PW)	
–25°C to 85°C	TPS9103PWLE	TPS9103Y

The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type).

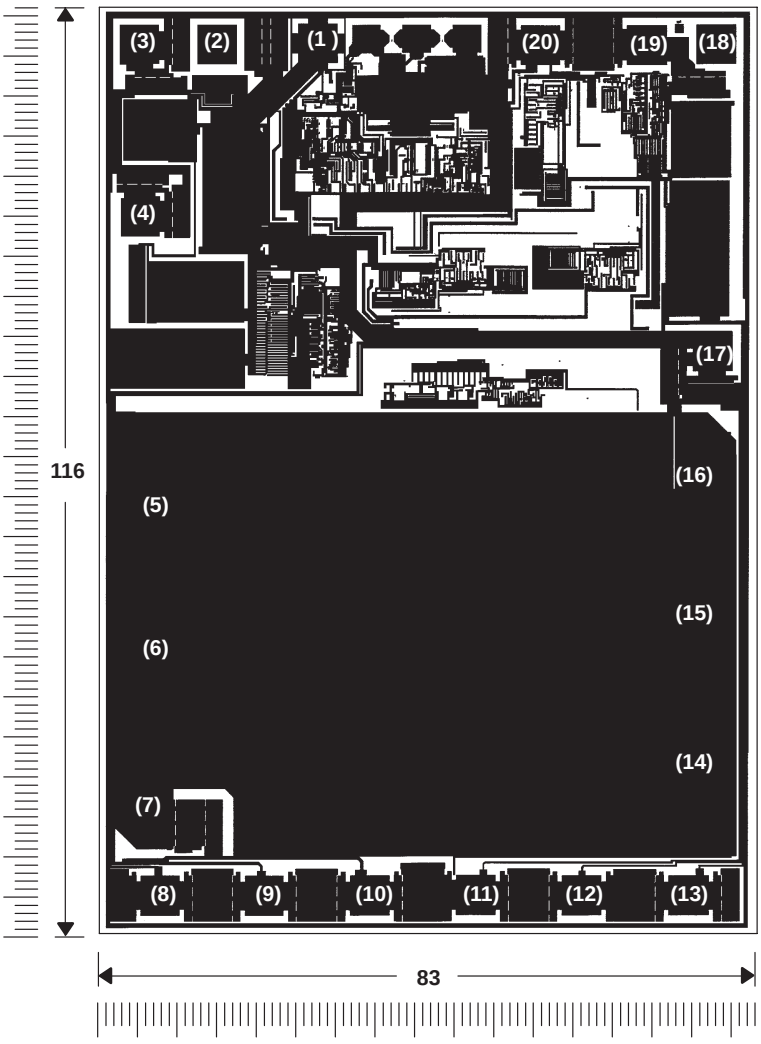
functional block diagram

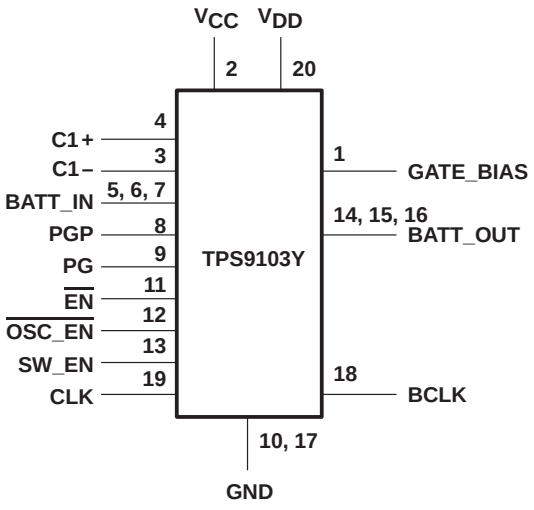


TPS9103Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS9103. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GATE_BIAS	1	Negative gate-bias output voltage
V_{CC}	2	Logic supply voltage
C1–	3	External capacitor connection (inverting charge pump)
C1+	4	External capacitor connection (inverting charge pump)
BATT_IN	5	High-side switch input voltage
BATT_IN	6	High-side switch input voltage
BATT_IN	7	High-side switch input voltage
PGP	8	Program input for power-good threshold
PG	9	Power-good output
GND	10	Ground
$\overline{EN}$	11	Chip-enable input
$\overline{OSC\_EN}$	12	Oscillator-enable input
SW_EN	13	High-side switch enable input
BATT_OUT	14	High-side switch output voltage
BATT_OUT	15	High-side switch output voltage
BATT_OUT	16	High-side switch output voltage
GND	17	Ground
BCLK	18	Buffered clock output
CLK	19	Clock (bidirectional)
V_{DD}	20	Charge-pump supply voltage

detailed description

high-side switch and driver (BATT_IN, BATT_OUT, SW_EN)

The high-side switch is a p-channel MOSFET with a maximum on-state resistance of 180 mΩ ($V_{I(BATT\_IN)}$ = 6 V and V_{CC} = 3.3 V). The driver pulls the gate of the high-side switch to GATE_BIAS instead of ground to reduce the MOSFET on-state resistance. Gate breakdown considerations limit the voltage between BATT_IN and GATE_BIAS to 15 V. Extremely fast switching times are not required in this application, and the high-side switch/driver is designed to provide 2 μs maximum switching times with minimum power consumption. The GaAs depletion-mode MOSFETs in the PA are protected from damage at power-up by internal logic that inhibits the driver until negative gate bias is available. The control input SW_EN is compatible with 3-V and 5-V CMOS logic; a logic-high input turns the high-side switch on.

oscillator ($\overline{\text{OSC\_EN}}$, CLK)

The internal oscillator drives the charge pump at 50 kHz with a nominal duty cycle of 50% when both the $\overline{\text{EN}}$ and $\overline{\text{OSC\_EN}}$ inputs are logic lows. CLK outputs the internal oscillator signal (no buffer). A logic-high input to $\overline{\text{OSC\_EN}}$ disables the internal oscillator and allows the charge pump to operate from an external clock connected to CLK. When an external clock with negative overshoot is applied, a Schottky diode must be added to limit the amplitude of the overshoot.

charge pump (GATE_BIAS, C1+, C1–)

The inverting charge pump generates the negative gate-bias voltage output at GATE_BIAS.

chip enable ($\overline{\text{EN}}$)

A logic high on $\overline{\text{EN}}$ shuts down the internal functions of the TPS9103 and turns the bias system off, reducing the supply current to less than 10 μA. A low input on $\overline{\text{EN}}$ causes normal operation to resume.

power good (PG, PGP)

PG output is logic high when GATE_BIAS is in regulation. PG output is logic low when GATE_BIAS is not in regulation. The high-side switch is disabled and PG is forced to logic low whenever the magnitude of GATE_BIAS is less than 0.6 × V_{DD}. A modified threshold for the power-good function can be achieved by programming PGP with an external resistor.

undervoltage lockout for V_{CC} and V_{DD} (UVLO and UVDLO)

Undervoltage lockout prevents operation at supply voltages too low for proper operation. When UVLO or UVDLO is active, all power-switch drives are forced to the off state and bias is removed from unneeded functions. Hysteresis is provided to minimize cycling on and off because of source impedance loading when the supply voltage is close to the threshold.

buffered clock output (BCLK)

The buffered clock output is a driver for an external charge pump. When the optional external charge pump is not needed, BCLK should be left unconnected. For more details, see the application section.

supply input for inverting charge pump (V_{DD})

V_{DD} is the supply voltage for the inverting charge pump. In normal operation, V_{DD} is connected to V_{CC}. If the negative gate-bias needs to be larger than V_{CC} (i.e., more negative), then a higher voltage supply needs to be connected to V_{DD}. This can be supplied from an external charge pump driven from BCLK.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	645 mW	6.5 mW/°C	353 mW	255 mW

Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 154°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

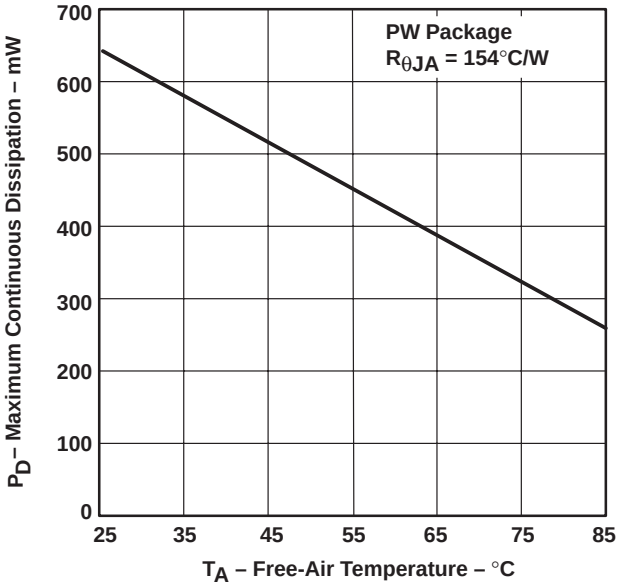


Figure 1. Dissipation vs Free-Air Temperature

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

High-side switch input voltage range, BATT_IN (see Note 1) . . . . . –0.3 V to 15 V
Supply voltage range, V_{CC}, V_{DD} . . . . . –0.3 V to 7 V
Differential voltage, |BATT_IN|–|GATE_BIAS| . . . . . 15 V
Input voltage range, SW_EN, $\overline{EN}$, CLK, $\overline{OSC\_EN}$, PG . . . . . –0.3 V to V_{CC} + 0.3 V
GATE_BIAS . . . . . –5.5 V
Output current, PG . . . . . 5 mA
Output current, BCLK . . . . . 50 mA
Output current, GATE_BIAS . . . . . 10 mA
Output current, BATT_OUT . . . . . 2 A
Peak output current, BATT_OUT . . . . . 4 A
Maximum external clock frequency, CLK . . . . . 100 kHz
Continuous total power dissipation . . . . . See Dissipation Rating Table
Junction temperature range, T_J . . . . . –25°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to device GND.
2. Differential voltage calculated: $|V_I max| + |GATE\_BIAS|$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Input voltage, BATT_IN		3		9	V
Supply voltage, V_{CC}, V_{DD}		2.7		5.5	V
Output voltage, GATE_BIAS, V_O		–2		–5	V
Continuous output current, GATE_BIAS		0		10	mA
Continuous output current, BATT_OUT		0		2	A
Charge-pump capacitor value at C1+/C1–			0.33		µF
External clock frequency, CLK		25		75	kHz
High-level input voltage, V_{IH}	SW_EN, $\overline{EN}$, $\overline{OSC\_EN}$, CLK	2			V
Low-level input voltage, V_{IL}				0.8	V
Input current, I_I		–1		1	µA
Operating junction temperature, T_J		–25		125	°C

electrical characteristics over recommended operating junction temperature range, $\overline{BATT\_IN}$ = 6 V, V_{CC} = V_{DD} = 3.3 V, $I_{O(BATT\_OUT)}$ = 0.5 A, $I_{O(GATE\_BIAS)}$ = 2 mA, $\overline{EN}$ = $\overline{OSC\_EN}$ = 0 V, SW_EN = V_{CC}, C1 = 0.33 µF (unless otherwise noted)

charge pump

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage		–3	–3.10	–3.3	V
Output resistance			95		Ω

high-side switch

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Dran-to-source on-state resistance	T_A = 25°C				135	180	mΩ
	T_A = –25°C to 85°C					210	
	T_A = 25°C,	$V_{I(BATT\_IN)}$ = 3 V			160	220	
	T_A = –25°C to 85°C,	BATT_IN = 3 V				260	
Leakage current	T_A = 25°C,	$V_{I(BATT\_IN)}$ = 9 V,	SW_EN = 0 V			1	µA
	T_A = 85°C,	$V_{I(BATT\_IN)}$ = 9 V,	SW_EN = 0 V			10	
Delay to high-level output	SW_EN from 0 to V_{CC}				0.2	2	µs
Delay to low-level output	SW_EN from V_{CC} to 0				0.9	2	µs

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	V_{CC} = 2.7 V to 5.5 V	35	50	60	kHz
Duty cycle	V_{CC} = 2.7 V to 5.5 V	40%	50%	60%	

buffered clock output (BCLK)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output resistance				10	Ω
High-level output voltage	I(BCLK) = 30 mA	V_{CC} –0.3			V
Low-level output voltage	I(BCLK) = 30 mA			0.3	V

power good (PG)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Threshold voltage	V_{DD} = 2.7 V to 5.5 V		0.60 × V_{DD}		V
On-state voltage	$I_{O(PG)}$ = 500 µA, V_{CC} = 2.7 V to 5.5 V			0.3	V
Off-state voltage	$I_{O(PG)}$ = –500 µA, V_{CC} = 2.7 V to 5.5 V	V_{CC} – 0.3			V
Hysteresis			130		mV

power good (PGP)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance		85			kΩ

undervoltage lockout (UVLO + UVDLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage	V_{CC} increasing	2.4		2.7	V
Hysteresis			130		mV

supply current (I_{CC} and I_{DD})

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby mode	$\overline{EN}$ = V_{CC}		1	10	µA
Undervoltage lockout	V_{CC} = V_{DD} < 2.3 V		35	50	µA
Operating mode	No load		300	500	µA

PARAMETER MEASUREMENT INFORMATION

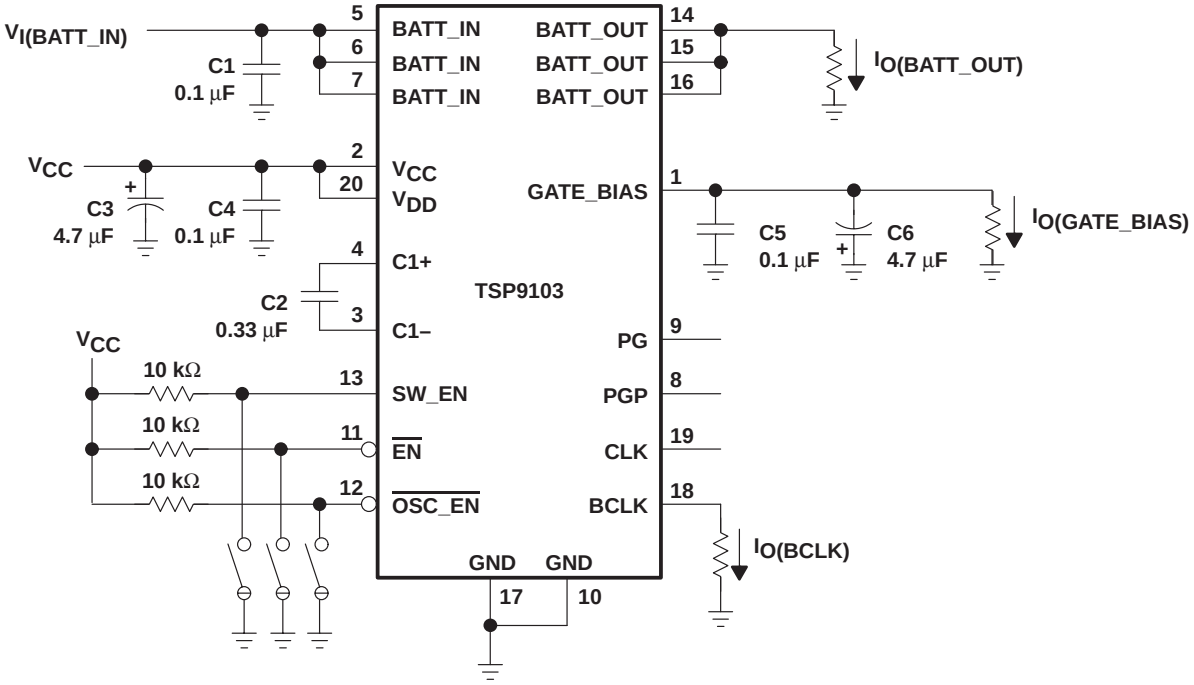


Figure 2. Test Circuit

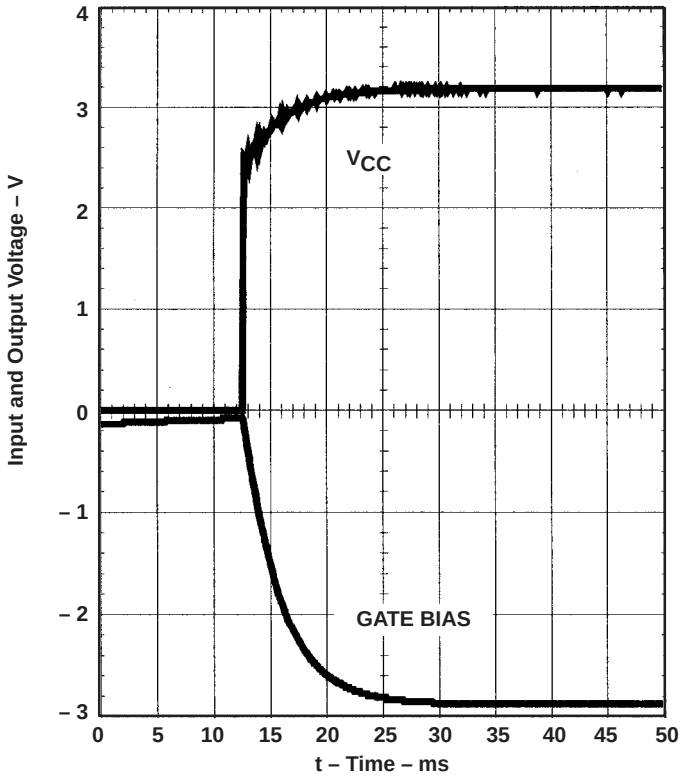


Figure 3. GATE_BIAS Output Voltage Rise Time

PARAMETER MEASUREMENT INFORMATION

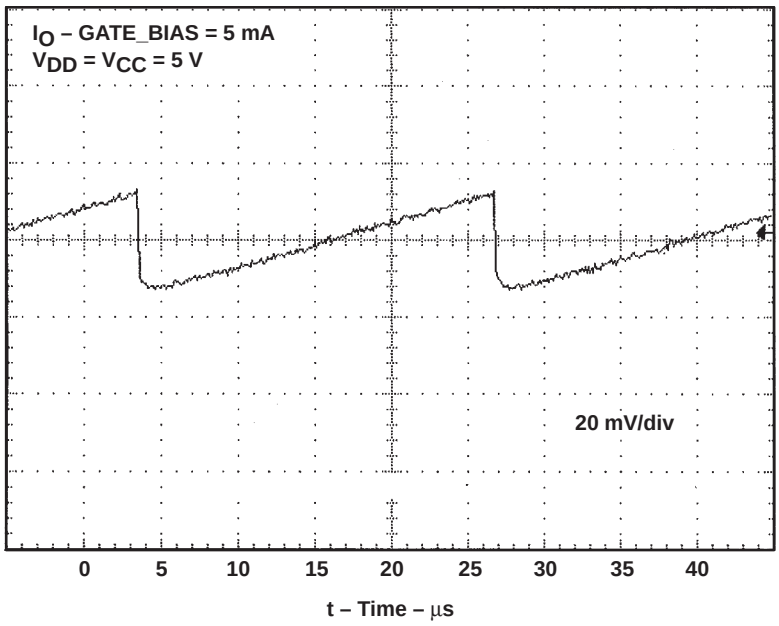


Figure 4. Ripple on GATE_BIAS

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance	vs Gate-source voltage, dc	5
		vs Temperature	6
F_{osc}	Oscillator frequency	vs Supply voltage	7
		vs Temperature	8
V_O	Output voltage	vs Output current	9
		vs CLK frequency	10
V_{IT}	Threshold voltage	vs Temperature	11
	Supply current (I_{CC} + I_{DD})	vs Supply voltage	12
		vs Temperature	13

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
GATE-SOURCE VOLTAGE,
dc ($V_{O(GATE\_BIAS)}$ −$V_{I(BATT\_IN)}$)

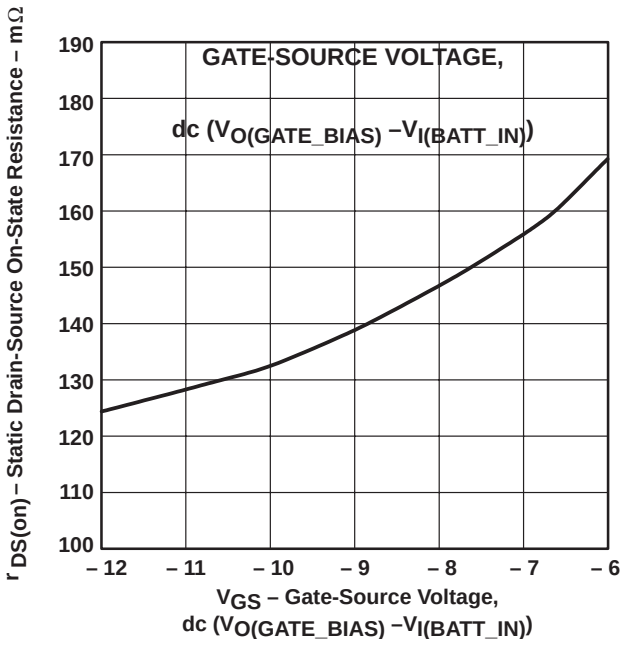


Figure 5

HIGH-SIDE SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
TEMPERATURE

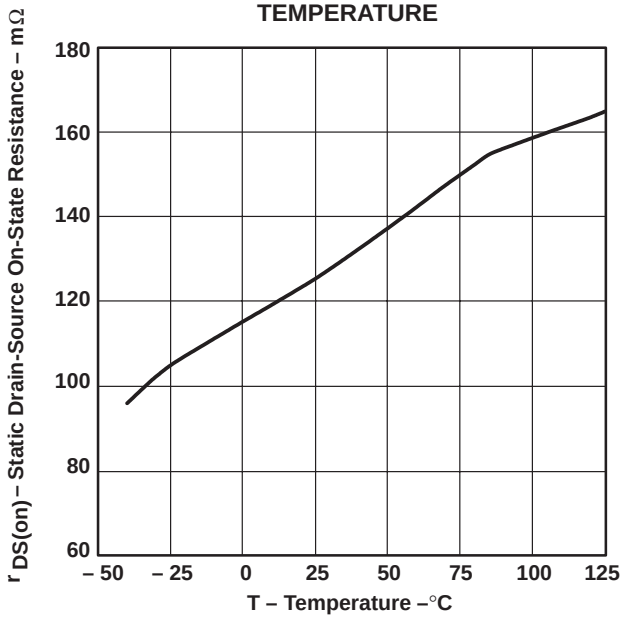


Figure 6

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

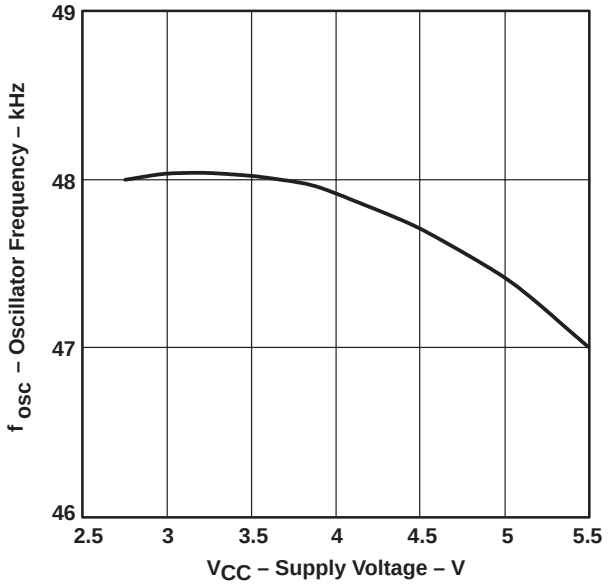


Figure 7

OSCILLATOR FREQUENCY vs TEMPERATURE

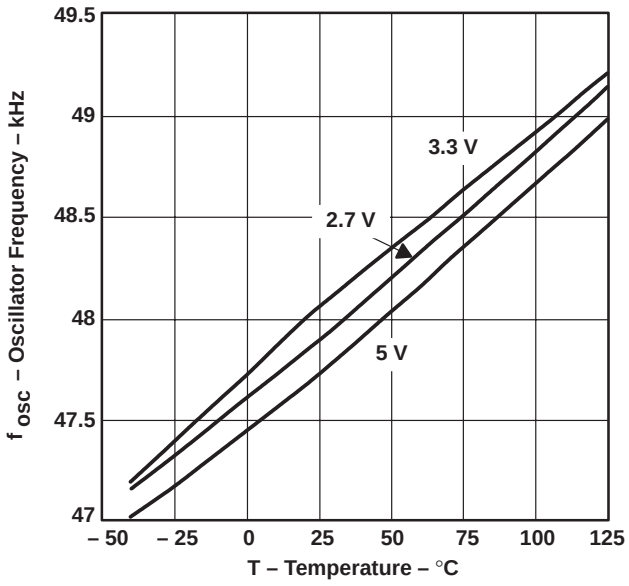


Figure 8

GATE BIAS OUTPUT VOLTAGE vs OUTPUT CURRENT

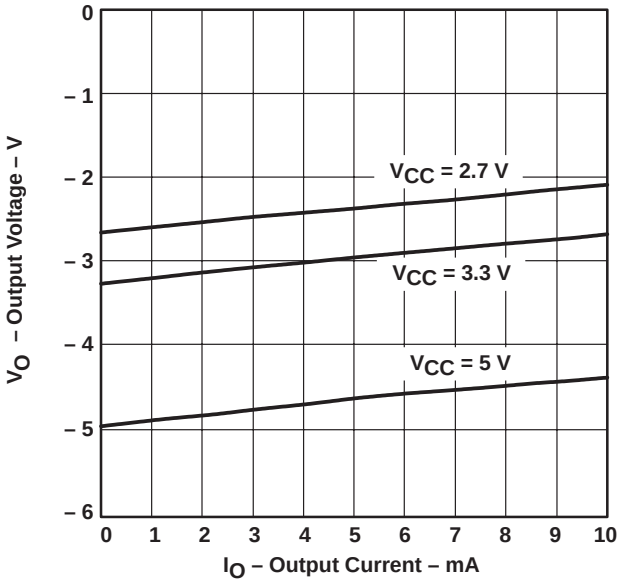


Figure 9

GATE BIAS OUTPUT VOLTAGE vs CLK FREQUENCY

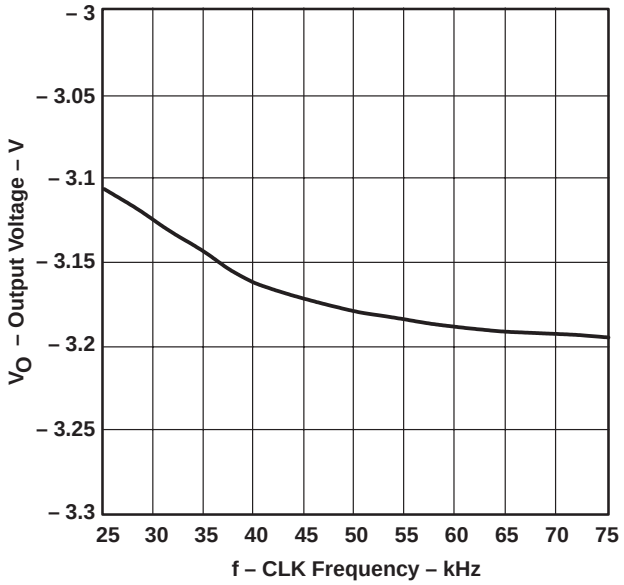


Figure 10

TYPICAL CHARACTERISTICS

UNDERVOLTAGE LOCKOUT (V_{CC}, V_{DD})
THRESHOLD VOLTAGE
vs
TEMPERATURE

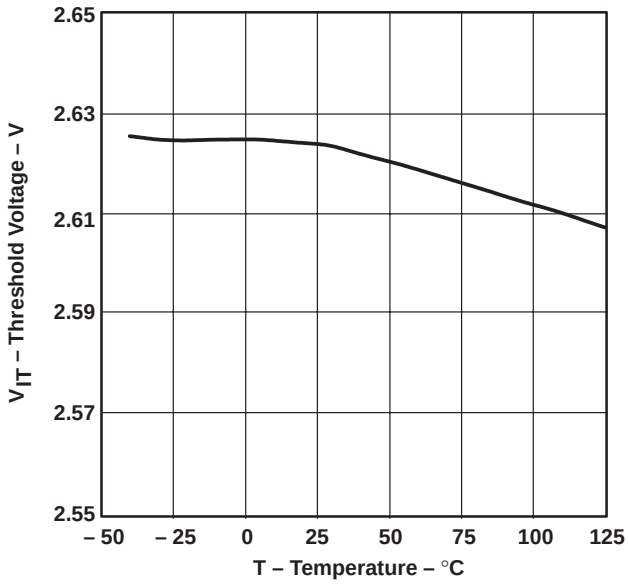


Figure 11

SUPPLY CURRENT (I_{CC} + I_{DD})
vs
SUPPLY VOLTAGE

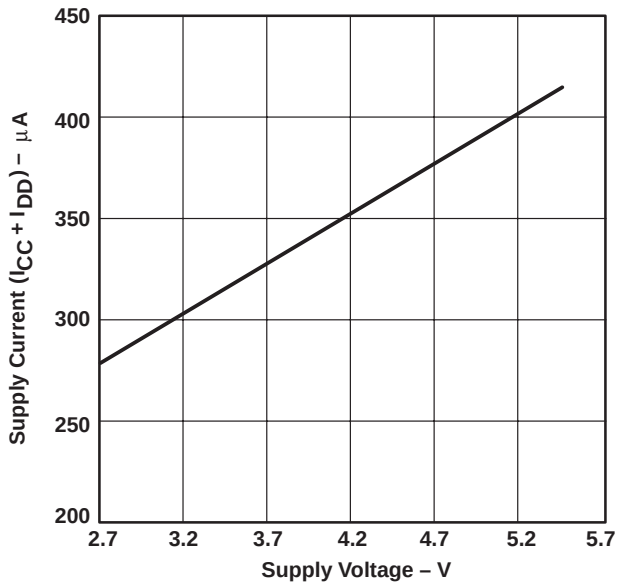


Figure 12

SUPPLY CURRENT (I_{CC} + I_{DD})
vs
TEMPERATURE

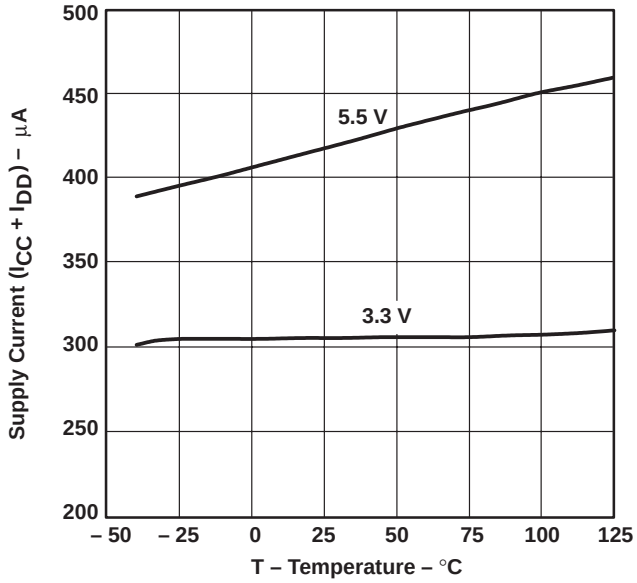


Figure 13

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in to the system

Using the given $R_{\theta JA}$ for this IC, the maximum power dissipation can be calculated with the equation:

$$P_D max = \frac{T_J max - T_A}{R_{\theta JA}}$$

For the TPS9103, the power dissipation is in the PMOSFET. To calculate the power, use: $I^2 \times R$ where I is the current through the device and R is the internal resistance as shown in the electrical characteristics table.

For a V_I of 6 V, the resistance at 85°C is 0.210 Ω. At a current of 2 A, the peak power dissipation is:

$$P_D = 2^2 \times 0.210 = 0.84 \text{ W}$$

Assuming a duty cycle of 1/8 or 0.125, the average power is:

$$0.84 \text{ W} \times 0.125 = 0.105 \text{ W}$$

The change in temperature is:

$$\Delta T = 0.105 \text{ W} \times 154°C/W = 16.2°C$$

and the junction temperature is:

$$T_J = 85°C + 16.2°C = 101.2°C$$

APPLICATION INFORMATION

introduction

Traditionally the RF power amplifier (PA) is powered directly from the battery, with a switching arrangement for powering down when not in use. GaAs FET PAs require a negative bias voltage that must be present before the supply is connected, or there is risk of destroying the FET. Logic must be provided to ensure the presence of the negative bias voltage.

A secondary charge pump is necessary for systems in which the supply voltage is insufficiently high – the negative bias produced from the charge pump is inadequate. In mobile telephony a second charge pump (regulated or unregulated) may also be needed, e.g. for varicap diodes/VCOs and some preamplifiers. The need for larger dynamic range or control-voltage range can become critical in certain applications.

the TPS9103 approach

The TPS9103 integrates a P-channel MOSFET high-side switch together with a selectable oscillator and charge pump for the GaAs FET power-amplifier gate bias, which is monitored.

Complete precautions are taken to ensure that the PA supply is not enabled unless the gate bias is present while V_{CC} and V_{DD} are also good. This protects the PA from inadvertent damage–without a major system size/cost increase.

The bias regulation monitor is flexible, accommodating both fixed and programmable approaches. The fixed resistors, provided internally, set the trip voltage to $–0.6 \times V_{DD}$. If V_{DD} is 5 V, then the trip voltage is –3 V. Should another value be preferred, it can be set by applying voltage divider to PGP. See the section “dimensioning the external voltage divider” for more details.

The charge pump clock is also flexible. The on-chip oscillator runs at a nominal 50 kHz, or alternatively an external oscillator can be connected to CLK. When an external clock is used, $\overline{\text{OSC\_EN}}$ should be taken high to disable the oscillator. When $\overline{\text{OSC\_EN}}$ is low and the on-chip oscillator is used, CLK provides an unbuffered clock output.

The circuit provides for a secondary charge pump driver. The buffered BCLK output can be used (with four external components) to provide a higher supply, both for those system functions that require it and for those GaAs PAs that need a more negative bias than is made possible by inverting the existing supply. This is facilitated by use of single-cell Li-ion batteries.

Figure 14 shows the TPS9103 in a typical application.

APPLICATION INFORMATION

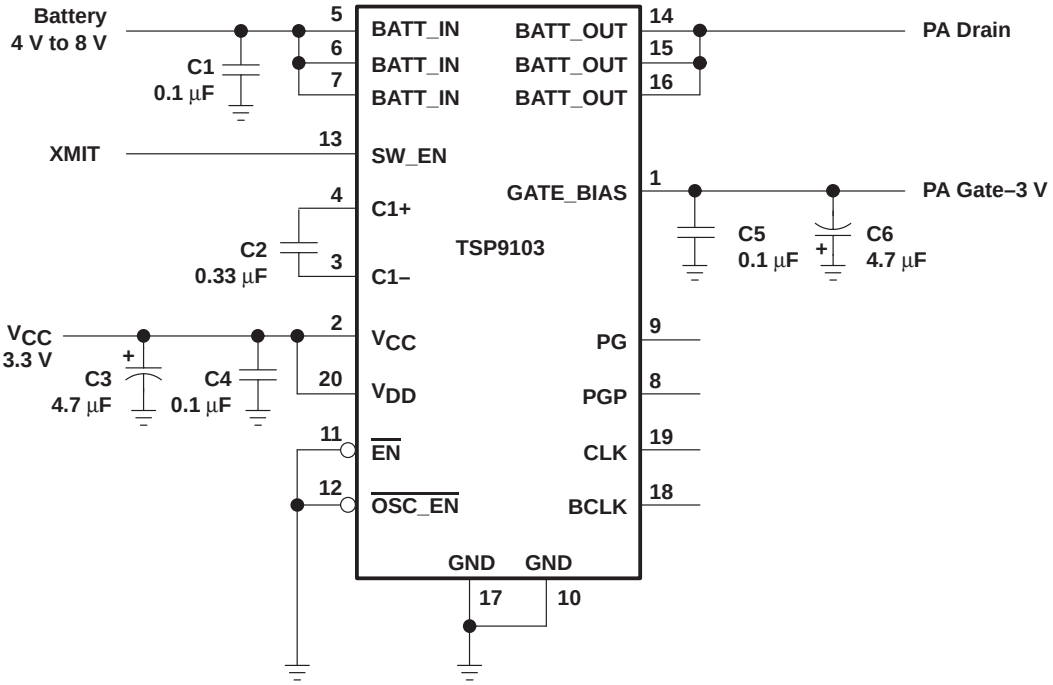


Figure 14. Typical Application

APPLICATION INFORMATION

capacitors of the internal inverting charge pump (see Figure 15)

This charge pump inverts the voltage at V_{DD} and provides a negative output voltage at GATE_BIAS.

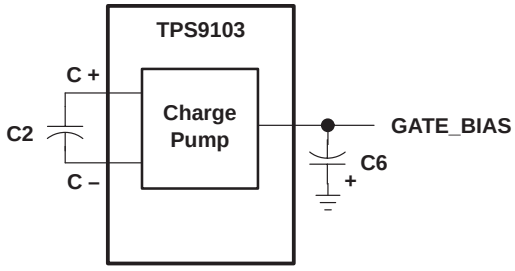


Figure 15. Internal Inverting Charge Pump

The output capacitor C6 limits the voltage ripple at GATE_BIAS:

$$V_{Ripple} = \frac{I_{O(GATE\_BIAS)}}{C6 \times f}$$

With a capacitor C6 of 4.7 μF and an output current of 10 mA, the voltage ripple at GATE_BIAS is 42 mV.

The capacitor C2 can be calculated using an equivalent resistance method:

$$R_{equivalent} = \frac{1}{C2 \times f}$$

Using 0.33 μF for C2, the equivalent resistance is:

$$R_{equivalent} = \frac{1}{0.33\ \mu F \times 50\ kHz} = 60.6\ \Omega$$

Add the internal resistance of the switches (35 Ω) to get a total resistance seen by the current:

$$R_{TOTAL} = 60 + 35 = 95\ \Omega$$

With a total resistance of 95 Ω and 10 mA flowing through it, a voltage drop of 0.95 V occurs. With 5 V on V_{DD}, the output is –4.05 V with a 42 mV ripple.

The capacitors should have a low equivalent series resistance (ESR) to maintain low ripple and low noise. Careful layout is required. In most instances it is advisable to add a small decoupling capacitor C5 close to the GATE_BIAS. An additional 0.1-μF capacitor at other locations may be necessary if the power amplifier is located away from the TPS9103.

APPLICATION INFORMATION

dimensioning of the external charge pump

For systems in which the bias voltage requirement is not met by inverting the power rail, the BCLK output can be used (with four passive components) to generate a higher $V_{DD.}$ The higher voltage is then inverted as before to produce the bias voltage. This voltage is also available for other parts of the main circuitry (see Figure 16).

With the TPS9103, an external charge pump could be used to increase the voltage at V_{DD}, thereby deriving a higher negative voltage at GATE_BIAS than would otherwise be available.

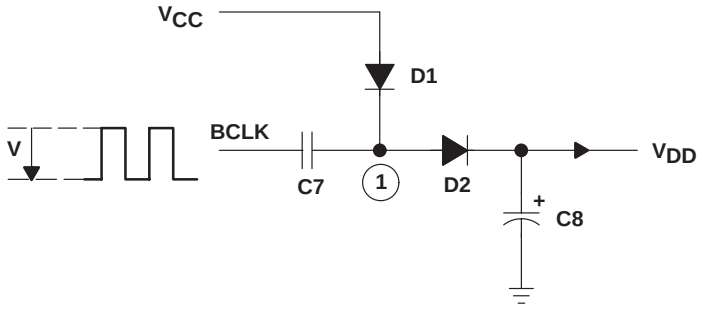


Figure 16. External Charge Pump

When BCLK is low, node 1 charges up to $V_{CC} – V_{diode}$. When BCLK goes high, node 1 is 2 $V_{CC} – V_{diode}$. The capacitor C8 charges up to 2 V_{CC} – 2 V_{diode}. This voltage can then be connected to V_{DD}.

The magnitude of V_{ripple} of V_{DD} is determined by the value of C8. Capacitor value must be large enough that the discharge during one period is not as great as the maximum voltage variation allowable. The discharge of C8 depends on the load current.

$$C8 = \frac{I_{O(GATE\_BIAS)}}{V_{ripple} \times f}$$

With a supply voltage of V_{CC} = 3.3 V, a maximum voltage variation (V_{ripple}) of 2% = 66 mV and a load of I_{CC} = 10 mA, the value of C8 is 3 μF. A 4.7 μF meets this requirement.

The capacitance of C7 can be calculated using an equivalent resistance method:

$$R_{equivalent} = \frac{1}{C7 \times f}$$

Using 0.22 μF for C7, the equivalent resistance is:

$$R_{equivalent} = \frac{1}{0.22\ \mu F \times 50\ kHz} = 90\,\Omega$$

Add the equivalent resistance to the internal resistance of the switch (10 Ω):

$$R_{TOTAL} = 90 + 10 = 100\ \Omega$$

With a total resistance of 100 Ω and with 10 mA flowing through it, a voltage drop of 1 V occurs. Thus with 3.3 V on V_{CC} the output is 4.2 V with a 42-mV ripple.

Care must be taken that the maximum voltages are not exceeded when using BCLK as a charge pump (see Figure 17).

APPLICATION INFORMATION

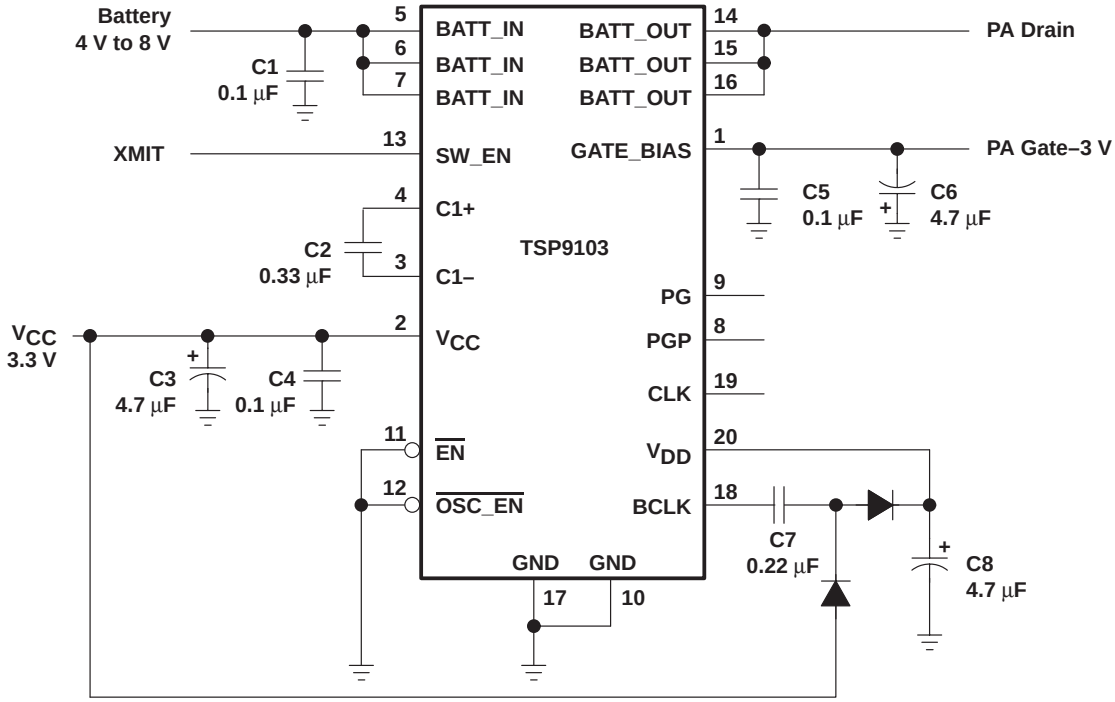


Figure 17. TPS9103 Configured With External Charge Pump

dimensioning the external voltage divider

Drain voltage should only be applied to the power amplifier when the complete negative voltage from the GATE_BIAS output is provided to the gate of the GaAs power amplifier. For that reason there is an internal voltage divider R/0.6R and a PG comparator in the TPS9103 (see Figure 15). When the voltage at the inverting input of the comparator reaches zero, the output goes high and the high-side MOSFET switches on, provided a SW_EN high signal is applied. For example, when the supply voltage at V_{DD} is 5 V, the high-side switch is switched on when the voltage at GATE_BIAS reaches –3 V.

This trip point can be changed to another value by using an external voltage divider connected between V_{DD}, GATE_BIAS, and PGP. The resistor values should be low enough to minimize the error that is present when the internal resistor values (typ R = 100 kΩ ± 30%) are taken into consideration. Therefore, the external resistor values, R1 and R2, are chosen within the 10-kΩ range.

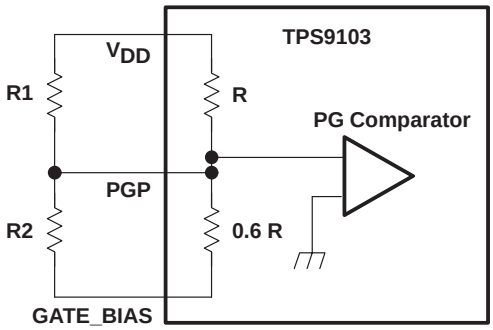


Figure 18. External Voltage Divider for Setting the Trip Point

R1 = 10 kΩ. The value of R2 can then be calculated using:

$$R2 = \frac{-0.6 \times R \times R1 \times V_{trip}}{0.6 \times V_{DD} \times [R1 + R] + V_{trip} \times R1}$$

where V_{DD} = supply voltage, and V_{trip} = chosen value to trip PG comparator.

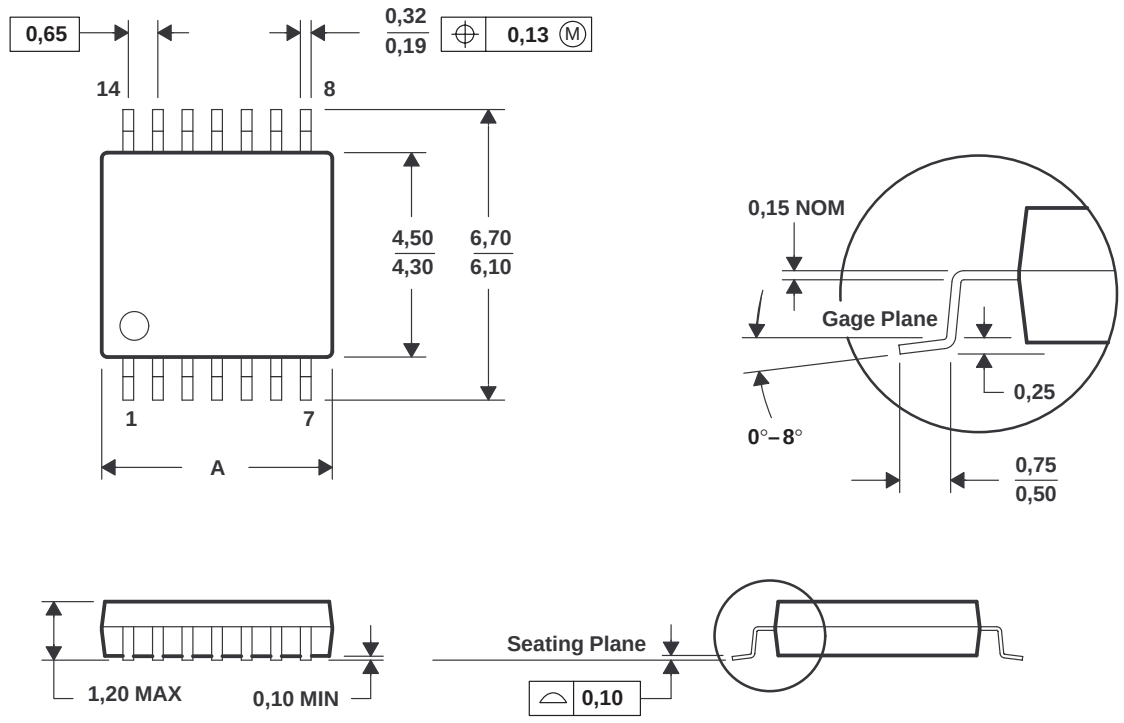
The values of the internal resistor can vary about 30%, and can move the trip point. In a worst-case condition, with a resistor variation of 30%, the shifting of the trip point can be calculated to:

$$\Delta V_{trip\_point} = V_{DD} \times \left(\frac{R1 + 1.3 \times R}{R1} \times \frac{0.6 \times R2}{R2 + 0.78 \times R} - \frac{R1 + R}{R1} \times \frac{0.6 \times R2}{R2 + 0.6 \times R} \right)$$

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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