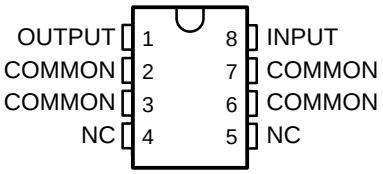
SLVS017Q – SEPTEMBER 1987 – REVISED MAY 2003

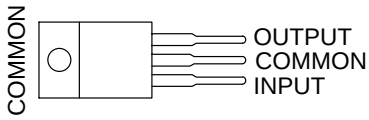
- **Very Low Dropout Voltage, Less Than 0.6 V at 150 mA**
- **Very Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751L Series**
- **60-V Load-Dump Protection**
- **Reverse Transient Protection Down To –50 V**
- **Internal Thermal-Overload Protection**
- **Overvoltage Protection**
- **Internal Overcurrent-Limiting Circuitry**
- **Less Than 500-μA Disable (TL751L Series)**

TL750L . . . D PACKAGE
(TOP VIEW)

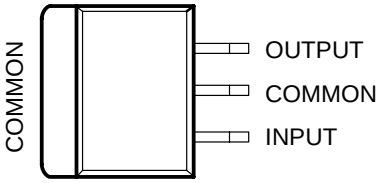


NC – No internal connection

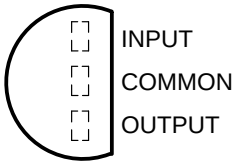
TL750L . . . KC PACKAGE
(TOP VIEW)



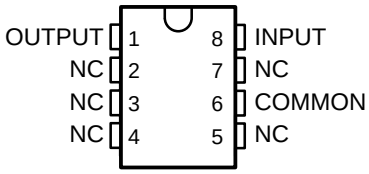
TL750L . . . KTE PACKAGE
(TOP VIEW)



TL750L . . . LP PACKAGE
(TO-92, TO-226AA)
(TOP VIEW)

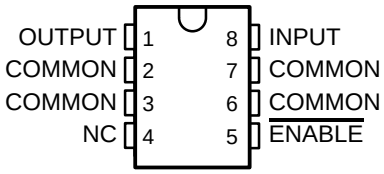


TL750L . . . P PACKAGE
(TOP VIEW)



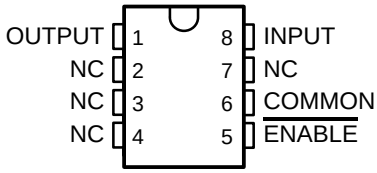
NC – No internal connection

TL751L . . . D PACKAGE
(TOP VIEW)



NC – No internal connection

TL751L . . . P PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable ($\overline{\text{ENABLE}}$) input. When $\overline{\text{ENABLE}}$ is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

description/ordering information (continued)

ORDERING INFORMATION

T_J	V_O TYP AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	Power Flex (KTE)	Reel of 2000	TL750L05CKTER	TL750L05C
		SOIC (D)	Tube of 75	TL750L05CD	50L05C
			Reel of 2500	TL750L05CDR	
			Tube of 75	TL751L05CD	51L05C
			Reel of 2500	TL751L05CDR	
		TO-92 (LP) TO-226AA (LP)	Bulk of 1000	TL750L05CLP	750L05C
			Reel of 2000	TL750L05CLPR	
		TO-220 (KC)	Tube of 50	TL750L05CKC	TL750L05C
	8 V	SOIC (D)	Tube of 75	TL750L08CD	50L08C
			Reel of 2500	TL750L08CDR	
		TO-92 (LP) TO-226AA (LP)	Bulk of 1000	TL750L08CLP	750L08C
	10 V	PDIP (P)	Tube of 50	TL751L10CP	TL751L10C
		SOIC (D)	Tube of 75	TL750L10CD	50L10C
			Reel of 2500	TL750L10CDR	
			Tube of 75	TL751L10CD	51L10C
			Reel of 2500	TL751L10CDR	
		TO-92 (LP) TO-226AA (LP)	Bulk of 1000	TL750L10CLP	750L10C
			Reel of 2000	TL750L10CLPR	
	12 V	SOIC (D)	Tube of 75	TL750L12CD	50L12C
			Reel of 2500	TL750L12CDR	
			Tube of 75	TL751L12CD	51L12C
			Reel of 2500	TL751L12CDR	
		TO-92 (LP) TO-226AA (LP)	Bulk of 1000	TL750L12CLP	750L12C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Continuous input voltage . . . . . 26 V
Transient input voltage, T_A = 25°C (see Note 1) . . . . . 60 V
Continuous reverse input voltage . . . . . –15 V
Transient reverse input voltage, t ≤ 100 ms . . . . . –50 V
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds . . . . . 260 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The transient input voltage rating applies to the waveform shown in Figure 1.

package thermal data (see Note 2)

PACKAGE	BOARD	θ_{JC}	θ_{JA}
PDIP (P)	High K, JESD 51-7	57°C/W	85°C/W
POWER-FLEX (KTE)	High K, JESD 51-5	3°C/W	23°C/W
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-92 (LP)	High K, JESD 51-7	55°C/W	140°C/W
TO-220 (KC)	High K, JESD 51-5	3°C/W	19°C/W

NOTE 2: Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

				MIN	MAX	UNITS
V_I	Input voltage		TL75xL05	6	26	V
			TL75xL08	9	26	
			TL75xL10	11	26	
			TL75xL12	13	26	
V_{IH}	High-level $\overline{\text{ENABLE}}$ input voltage		TL751Lxx	2	15	V
V_{IL}‡	Low-level ENABLE input voltage	T_J = 25°C	TL751Lxx	–0.3	0.8	V
		T_J = 0°C to 125°C	TL751Lxx	–0.15	0.8	
I_O	Output current range		TL75xLxx	0	150	mA
T_J	Operating virtual junction temperature		TL75xLxxC	0	125	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL750L05 TL751L05			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V,	I_O = 0 to 150 mA	T_J = 25°C	4.80	5	5.2	V
			T_J = 0°C to 125°C	4.75		5.25	
Input regulation voltage	V_I = 9 V to 16 V				5	10	mV
	V_I = 6 V to 26 V				6	30	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				20	50	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 6 V to 26 V,	I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL750L08 TL751L08			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V,	I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
			T_J = 0°C to 125°C	7.6		8.4	
Input regulation voltage	V_I = 10 V to 17 V				10	20	mV
	V_I = 9 V to 26 V				25	50	
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				40	80	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 9 V to 26 V,	I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL750L10 TL751L10			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
Input regulation voltage	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Input bias current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V, I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V				0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL750L12 TL751L12			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = 0°C to 125°C	11.4		12.6	
Input regulation voltage	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Input bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V				0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TYPICAL CHARACTERISTICS

TRANSIENT INPUT VOLTAGE vs TIME

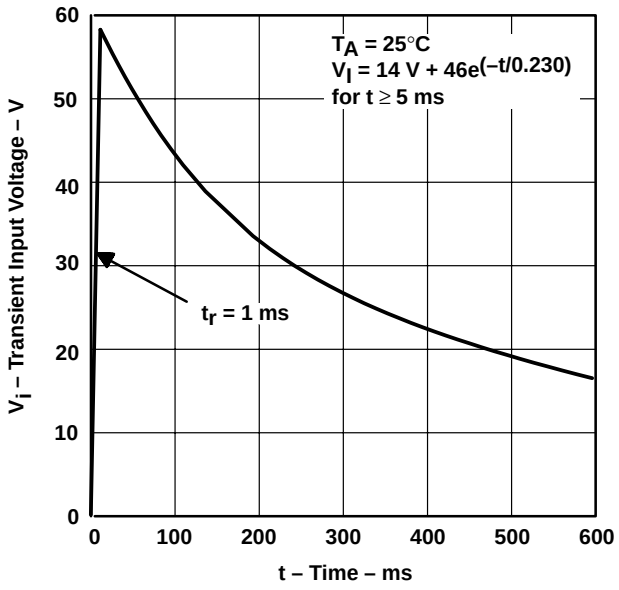


Figure 1

TL750L05 INPUT CURRENT vs INPUT VOLTAGE

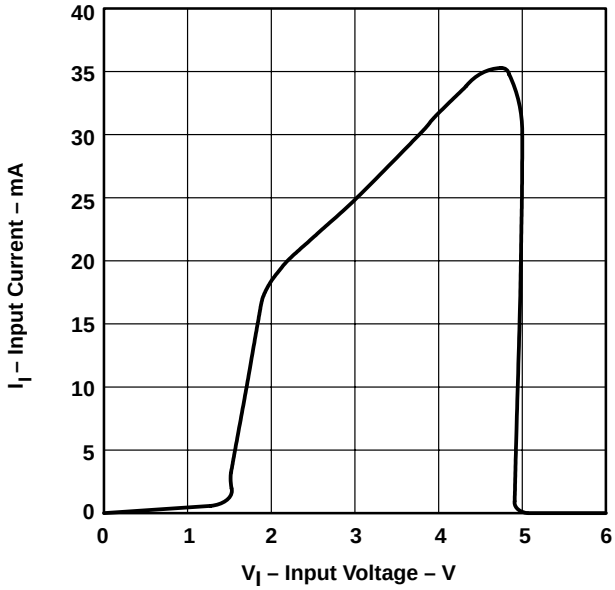


Figure 2

TL750L12 INPUT CURRENT vs INPUT VOLTAGE

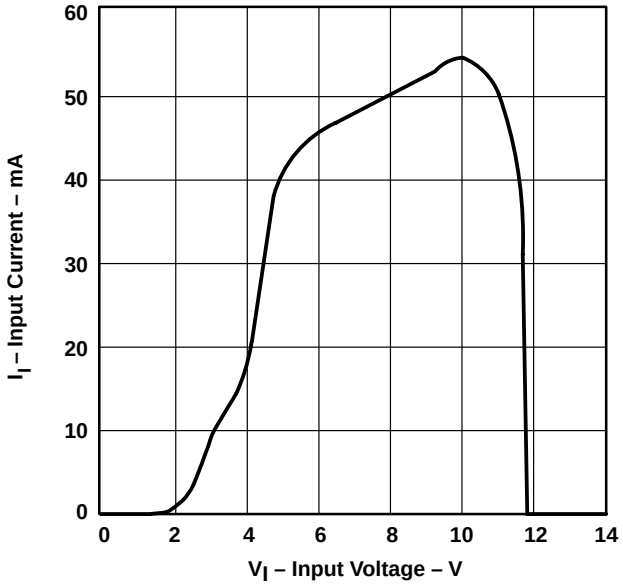


Figure 3

TYPICAL CHARACTERISTICS

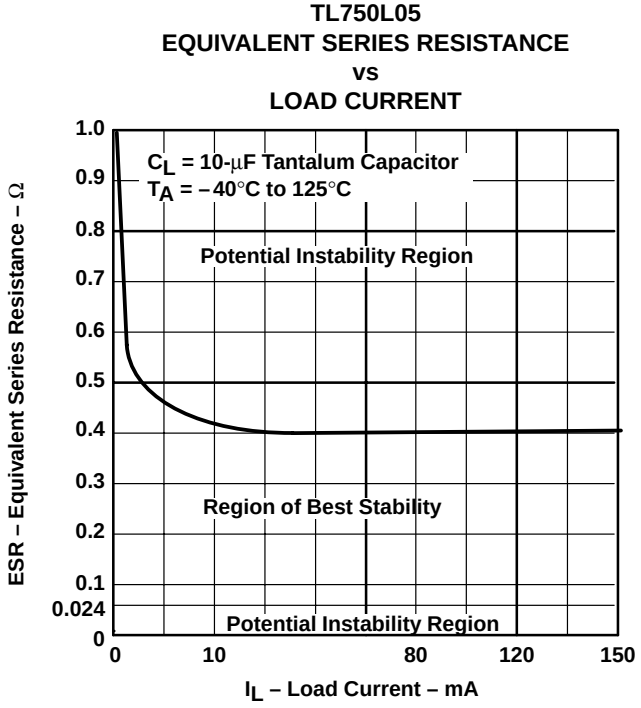
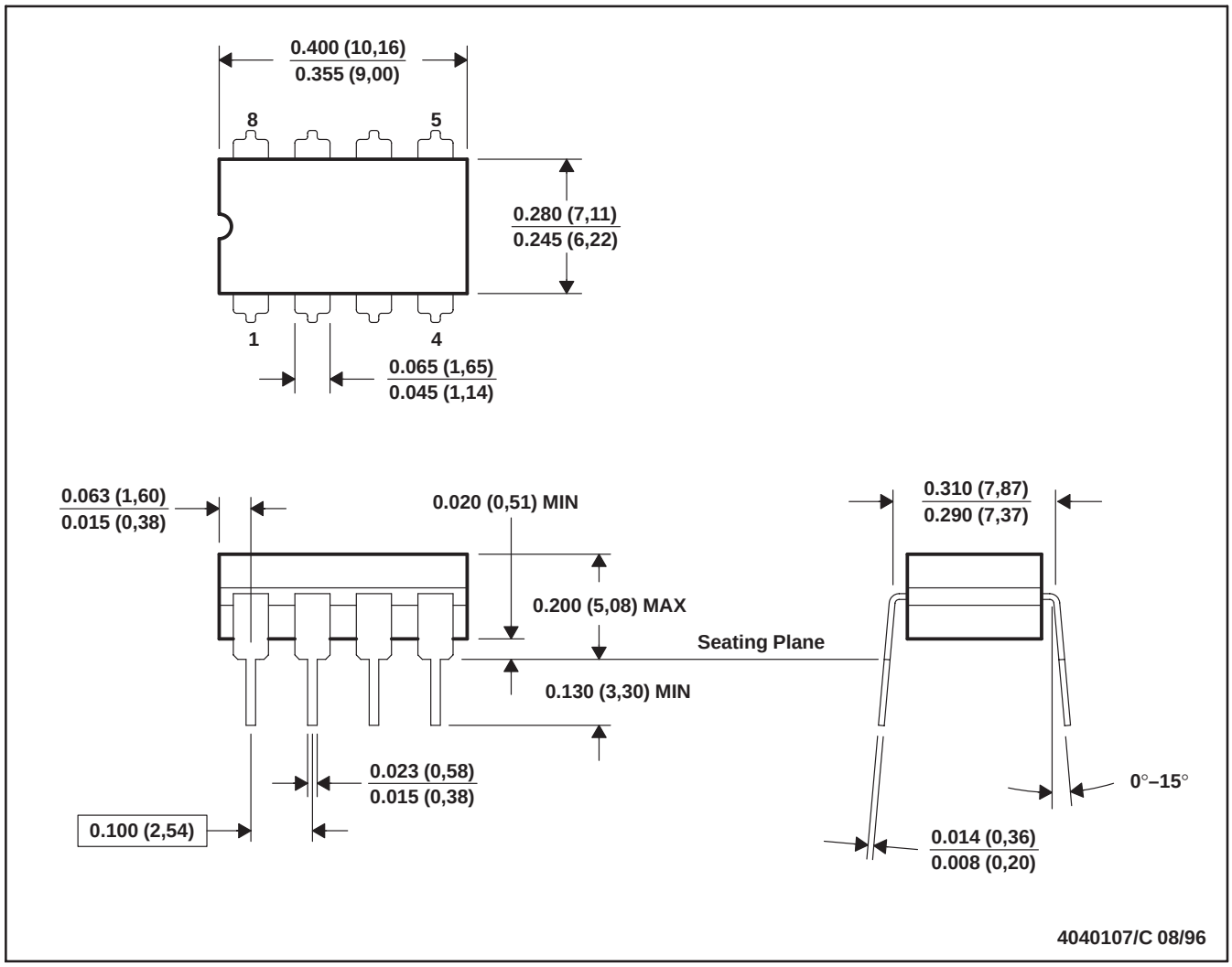


Figure 4

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

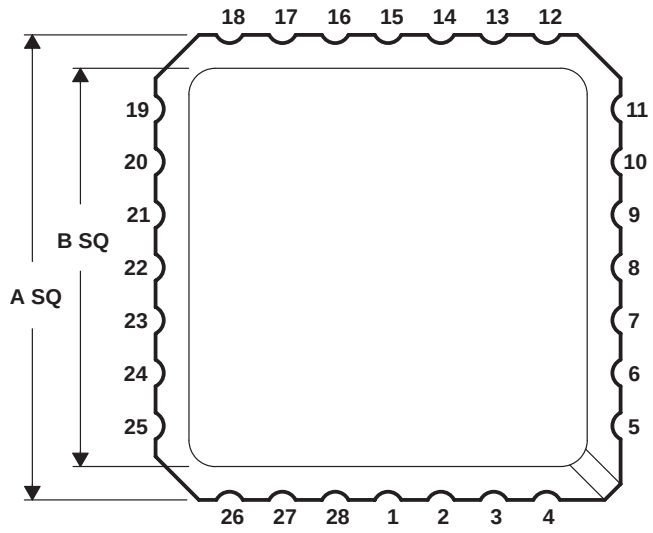


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

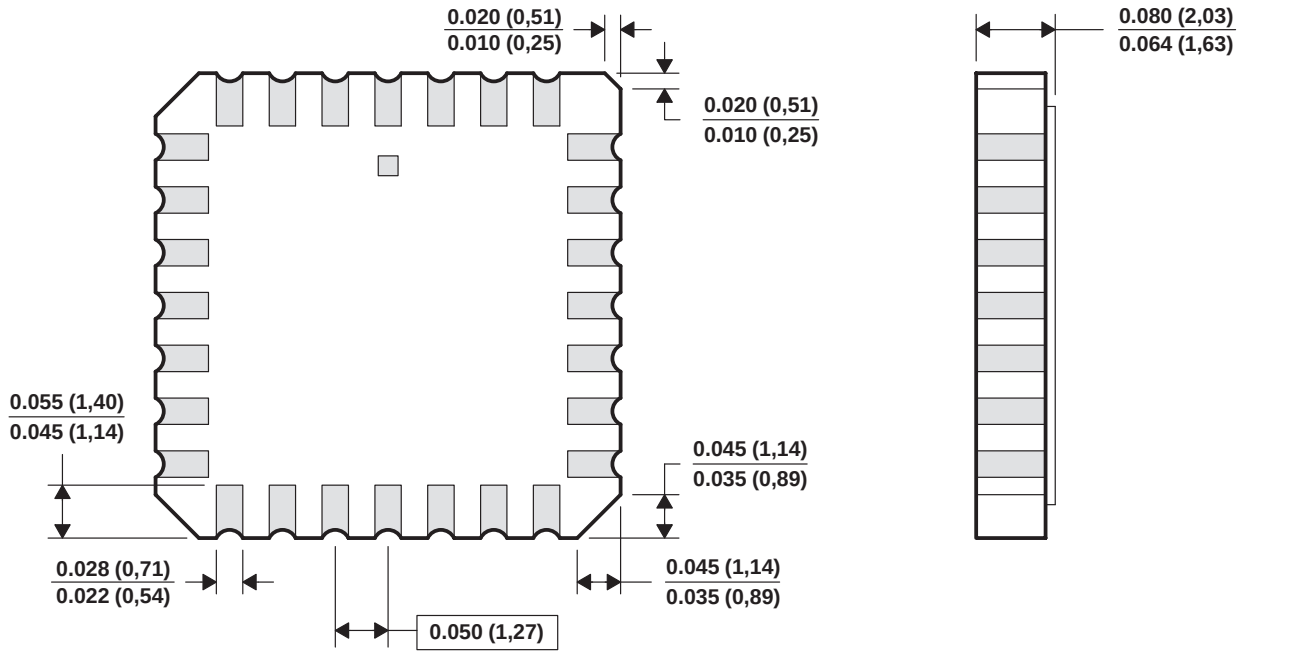
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

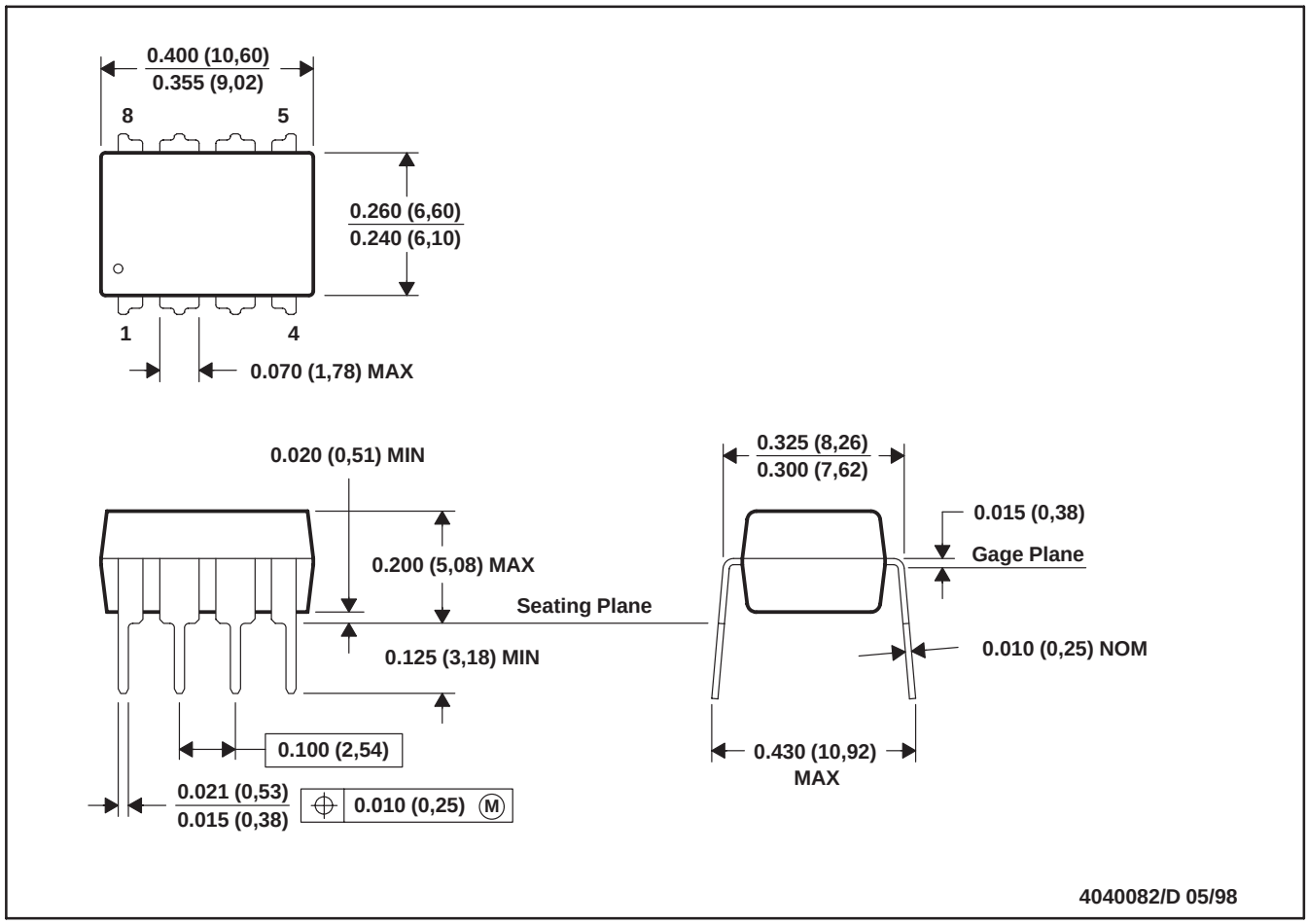


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**

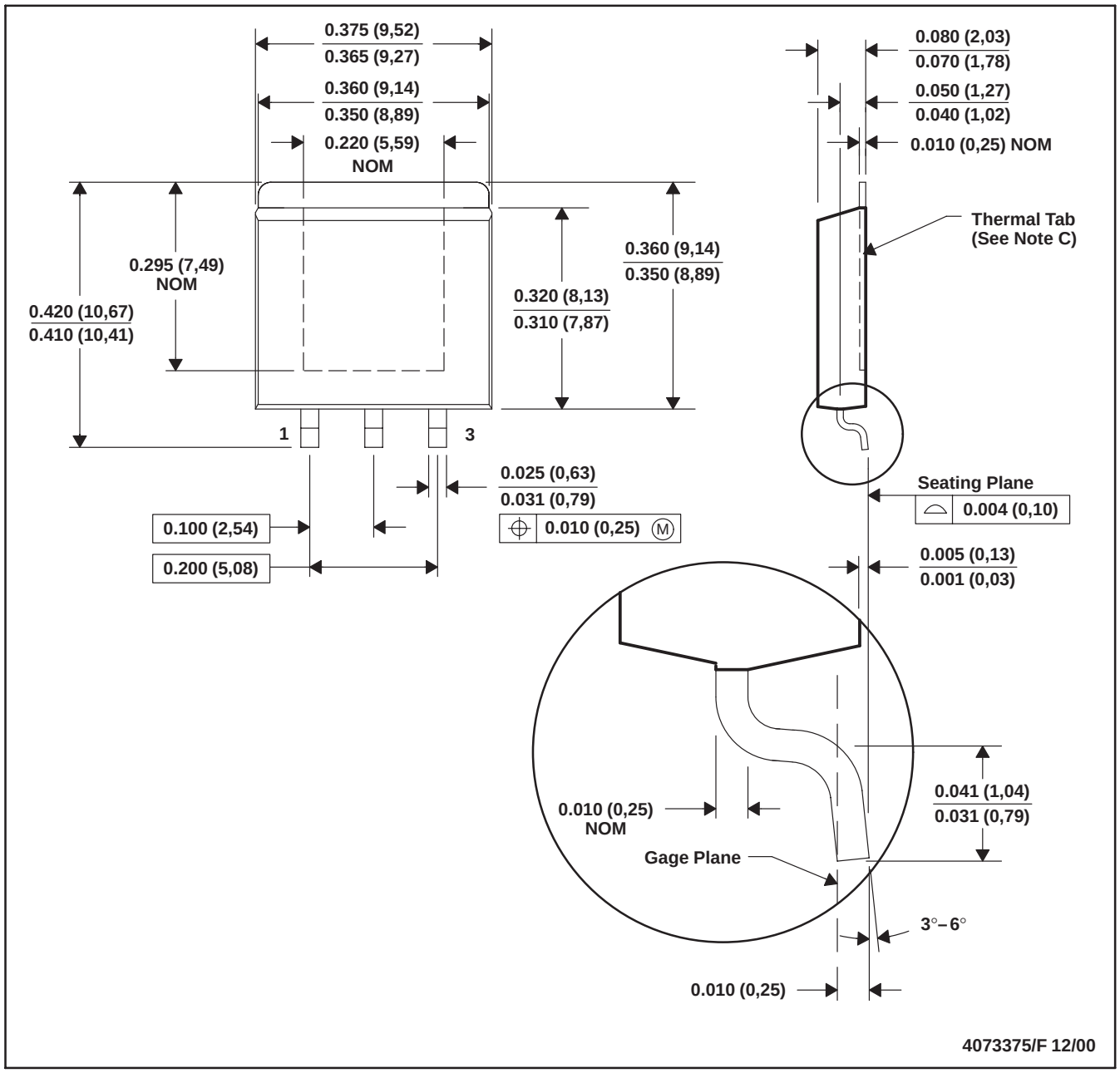


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

KTE (R-PSFM-G3) **PowerFLEX™ PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC MO-169

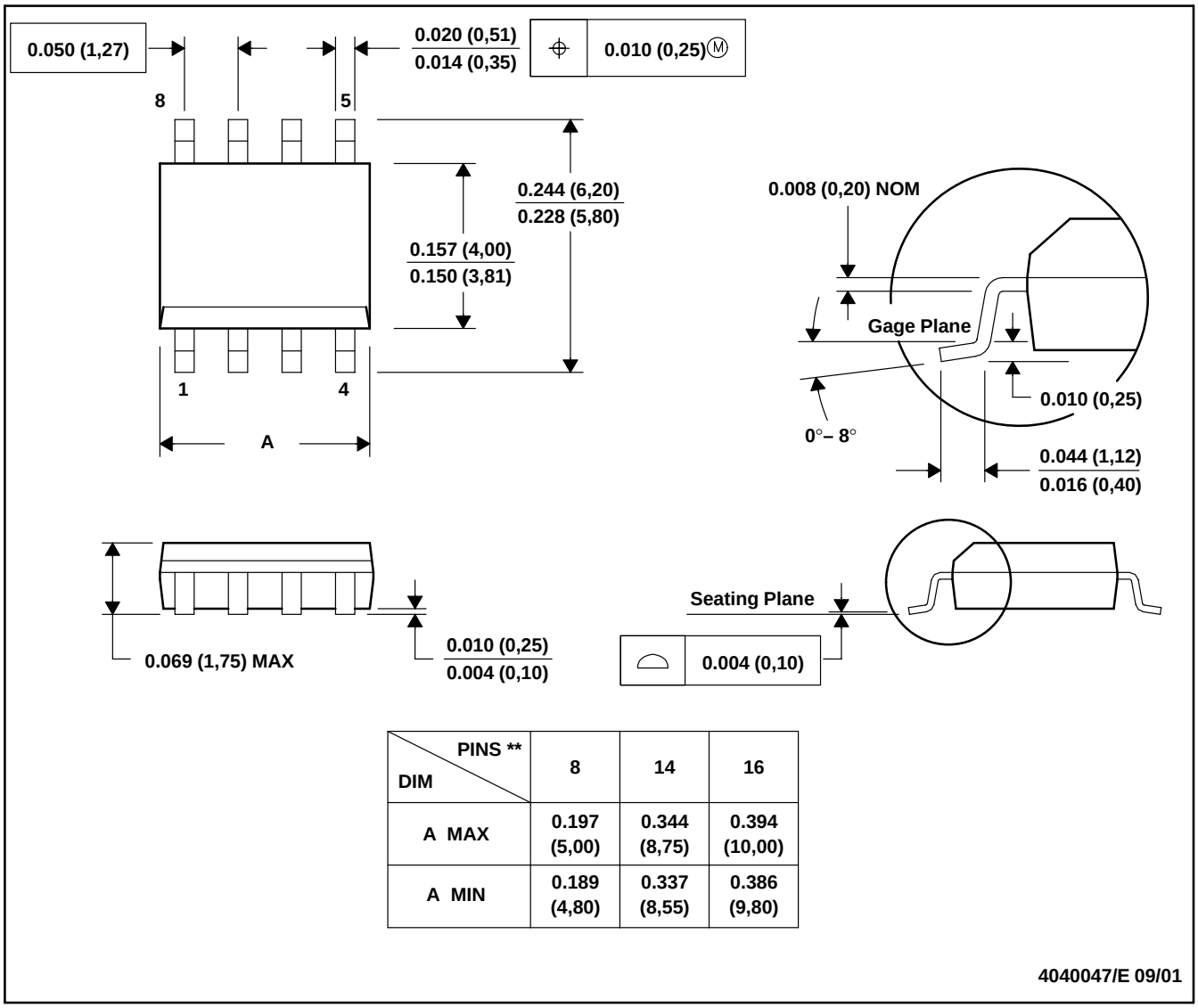
PowerFLEX is a trademark of Texas Instruments.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

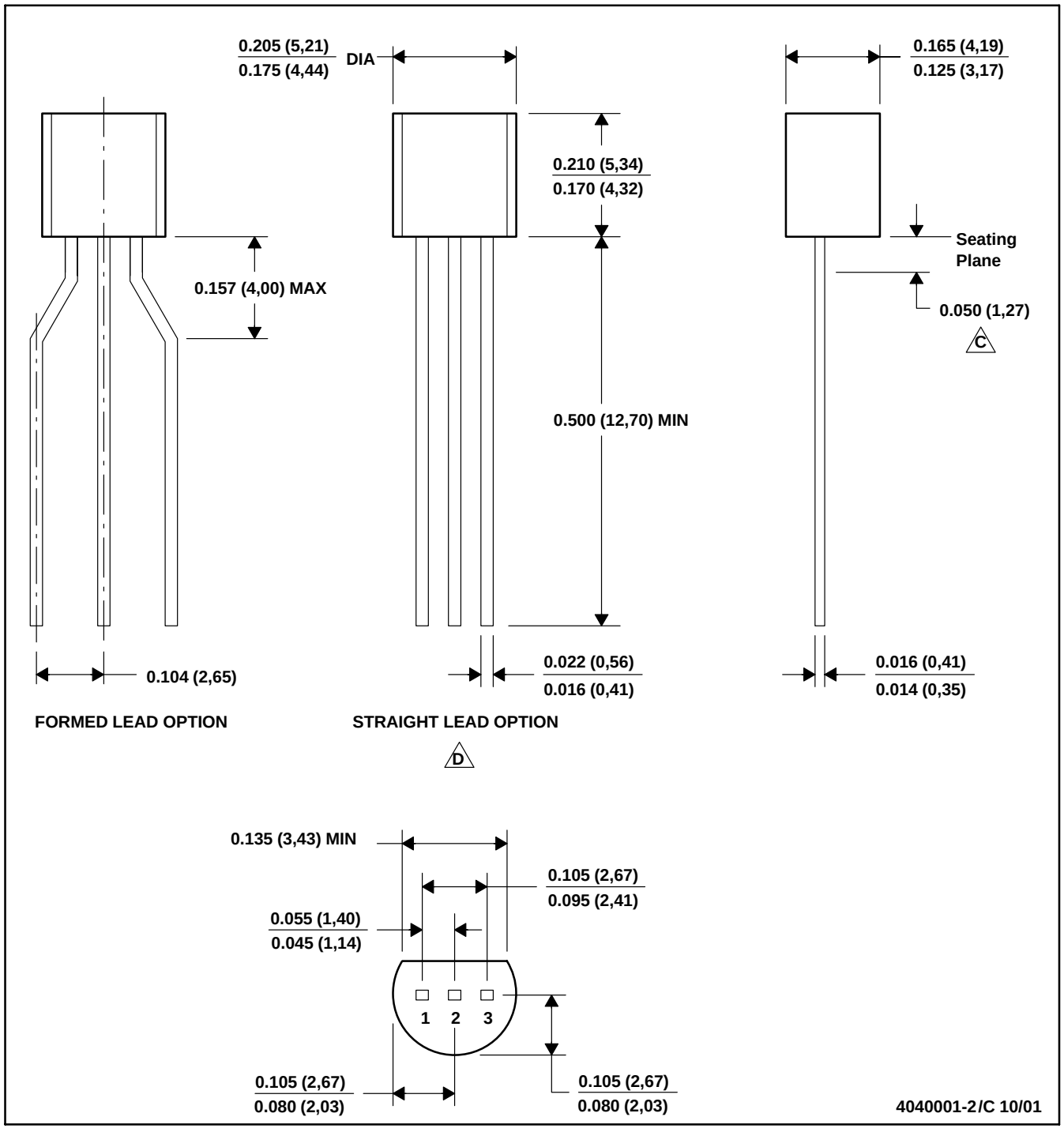


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

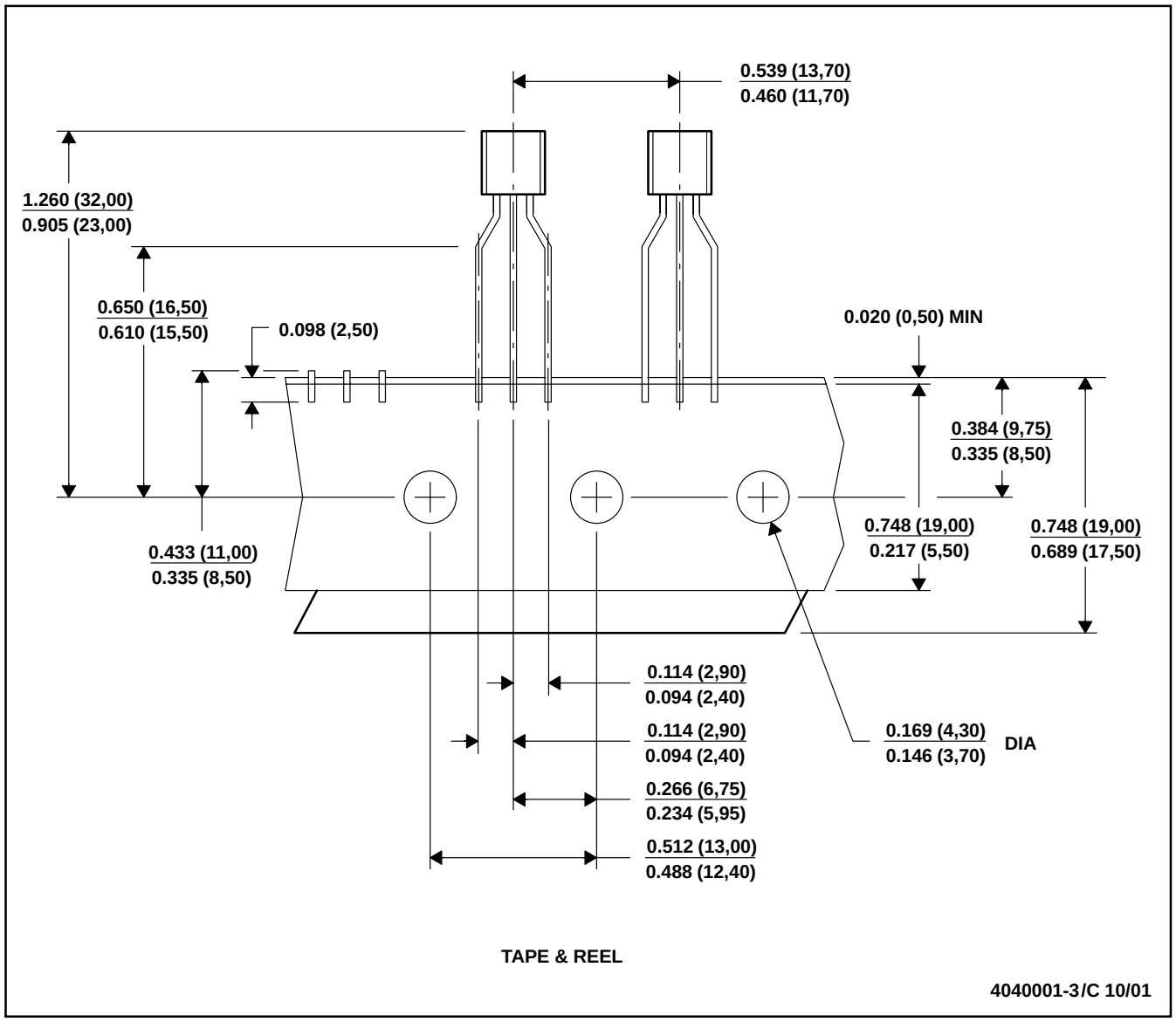
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area
D. FAlls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
E. Shipping Method:
Straight lead option available in bulk pack only.
Formed lead option available in tape & reel or ammo pack.

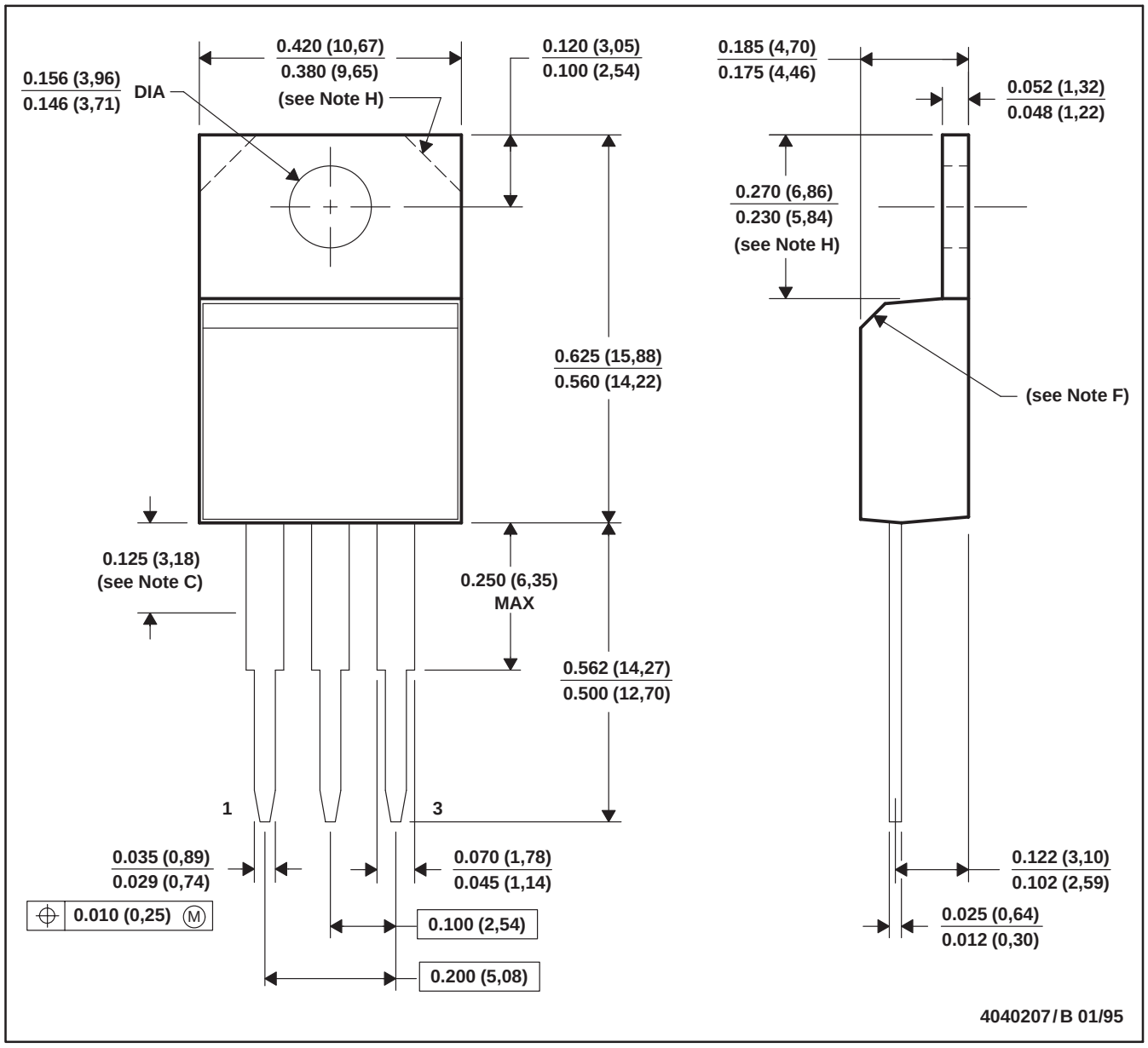
LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Format Lead Option package.

MSOT007A – JANUARY 1995 – REVISED SEPTEMBER 1995

KC (R-PSFM-T3) **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Falls within JEDEC TO-220AB
H. Tab contour optional within these dimensions

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