Features

- Supply-voltage range 2.7 V to 3.3 V
- Single sideband upconverters save filter cost
- Chosen architecture needs only one synthesizer
- 100 dB control range of IF & RF -VGAs
- 105 mA current consumption
- Programmable output power: PCS band: 8 dBm @ 54 dBc APCR, cellular band: 9 dBm @ -54 dBc ACPR
- Power-down functions support low current standby mode
- On-chip IF PLL
- 3 -wire bus programming

Benefits

- Extended battery-operating time
- Few external components
- VCO control without voltage doubler
- One device for dual band cellular/PCS and dual mode CDMA/AMPS operation
- Only single IF-filter for all 3 modes
- Very small MLF32 package
- Simple 4-bit programming
- Excellent linearity
- Low current consumption
- Very high output power

Electrostatic sensitive device.
Observe precautions for handling.

WIRELESS & µC

Dual Band CDMA / AMPS Transmitter

T0345

Description

T0345 is a monolithic integrated circuit, realised using Atmel Wireless & Microcontrollers advanced silicon germanium bipolar SiGe1 technology. It incorporates the complete transmitter chain for dual-band triple-mode cellular phones supporting CDMA (IS95) in cellular and PCS bands as well as AMPS. The device integrates an I/Q modulator, variable gain amplifier (VGA), two single side-band up-conversion mixer with fully integrated LO phase shifters, a voltage-controlled oscillator (VCO). Furthermore it includes a complete PLL with dividers, phase-frequency detector (PFD) and a charge pump. T0345 provides programmable output power in cellular and PCS band. The IC is available in a small leadless micro lead frame outline 32-pin (MLF32) package.

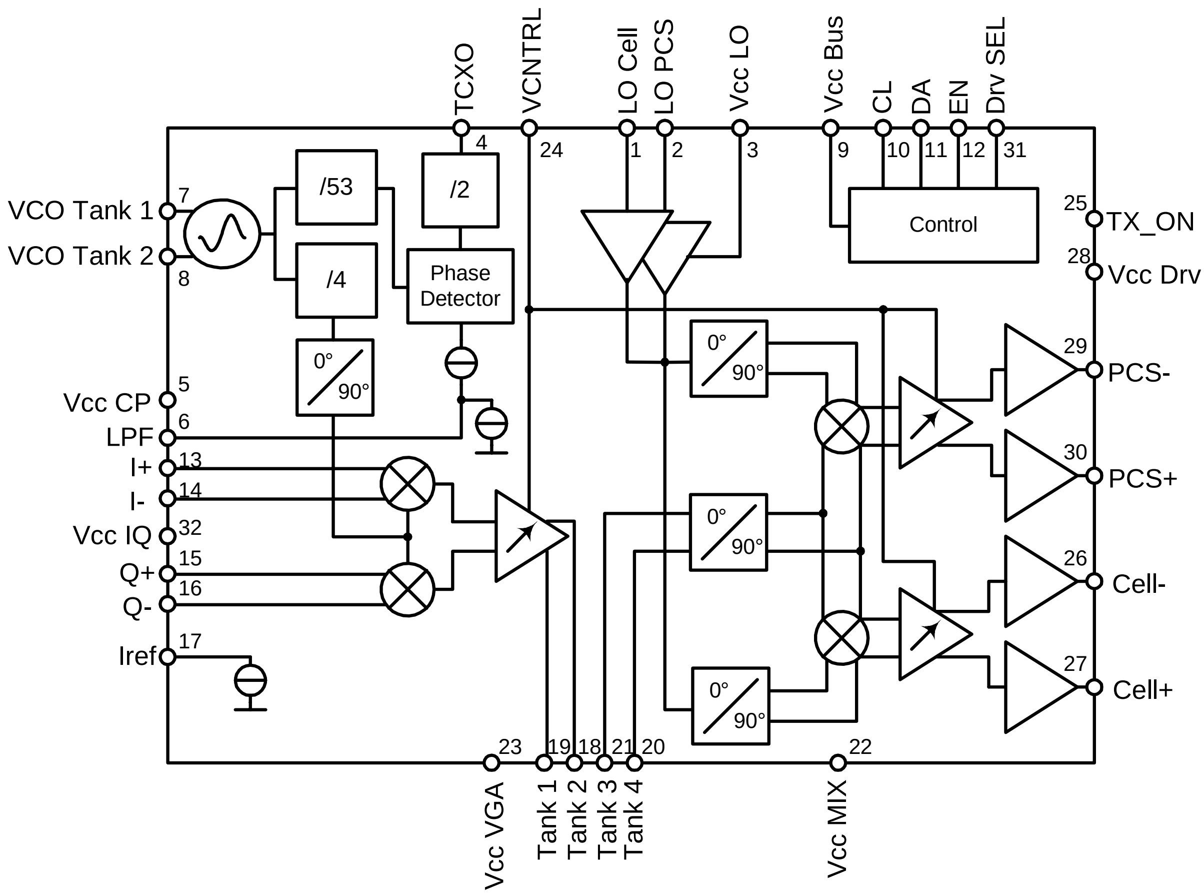
Ordering Information

Extended Type Number	Package	Remarks
T0345	MLF32	

Rev. A1, 22-Oct-01

Block Diagram

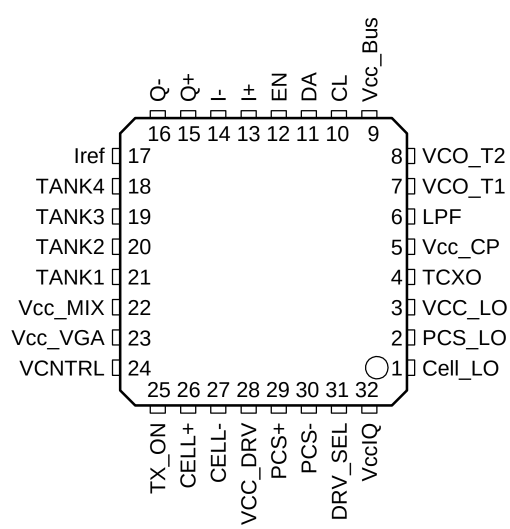
Figure 1.



Pin Description

Pin	Symbol	Function
1	Cell_LO	LO input Cellular 900 MHz
2	PCS_LO	LO input PCS 1800 MHz
3	VCC_LO	Supply LO drivers
4	TCXO	TCXO input
5	VCC_CP	Supply charge pump
6	LPF	Loop filter
7	VCO_T1	VCO tank1 (diff)
8	VCO_T2	VCO tank2 (diff)
9	VCC_bus	Supply voltage for bus from BB
10	CL	Clock 3-wire bus
11	DA	Data 3-wire bus
12	EN	Enable 3-wire bus
13	I+	Base band input
14	I-	Base band input
15	Q+	Base band input
16	Q-	Base band input
17	Iref	Reference Current Input
18	TANK4	Output to IF filter
19	TANK3	Output to IF filter
20	TANK2	Input from IF filter
21	TANK1	Input from IF filter
22	VCC_MIX	Supply RF mixer
23	VCC_VGA	Supply RF VGA
24	VCNTRL	Gain control input
25	TX ON	Transmitter ON (= high)
26	CELL+	Cellular output
27	CELL-	Cell. complementary output
28	VCC_DRV	Supply driver amplifier
29	PCS+	PCS output
30	PCS-	PCS complementary output
31	DRV_SEL	Driver select (Cellular, PCS)
32	VccIQ	Supply IQ-Modulator

Figure 2. Pinning



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltages Vcc_xxx	V_{VCC}	4.0	V
Maximum voltage difference between supply-pins	ΔV_{VCC}	200	mV
Voltage at any input	V_{Vi}	$-0.5 \le V_{Vi} \le V_{VCC} +0.5$	V
Current at any input/output pin except PCS_X, Cellular_X	$\lvert I_{I\#} \rvert, \lvert I_{O\#} \rvert$	40mA	mA
PCS_X, Cellular_X output current	$\lvert {}_{IPC} \rvert$	20mA	mA
Ambient temperature	T_{amb}	-20 to + 85	°C
Storage temperature	T_{stg}	-40 to +125	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction-ambient MLF32	R_{thJA}	tbd	K/W

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	V_{Vcc}	2.7 to 3.3	V
Ambient temperature	T_{amb}	-20 to +85	°C

Electrical Characteristics

V_S = 3 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	DC supply								
	Supply voltages		3, 5, 9, 22, 23, 28, 32	V_{Vcc}	2.7	3.0	3.3	V	
	Supply current	Active (V_{PU} = VS), No RF applied	3	I_{LOA}		7.2		mA	
		Standby (V_{PU} = 0), No RF applied	3	I_{LOP}			<1	µA	
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics

V_S = 3 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Supply current	Active (V_{PU} = VS), No RF applied	5	I_{CPA}		2.7		mA	
		Standby (V_{PU} = 0), No RF applied	5	I_{CPP}		2.7		mA	
		Bit 3 = 0, No RF applied	5	I_{CP}			<1	µA	
	Supply current	Active (V_{PUMIX} = VS), No RF applied	9	I_{BUSA}		0.7		mA	
		standby (V_{PUMIX} = 0), No RF applied	9	I_{BUSP}		0.7		mA	
	Supply current	Active (V_{PU} = Vs), No RF applied	32	I_{IQA}		371.9		mA	
		Standby (V_{PU} = 0), No RF applied	32	I_{IQP}		8.7		mA	
		Bit 3 = 0, No RF applied	32	I_{IQ}		120		µA	
	Supply current	Active (V_{PU} = Vs), No RF applied	22	I_{mixA}		19.1		mA	
		Standby (V_{PU} = 0), No RF applied	22	I_{mixP}		<1	20	µA	
	Supply current	For cellular band, No RF applied	23	I_{VGAA}		14		mA	
		For PCS band, No RF applied	23	I_{VGAA}		16.6		mA	
		No RF applied	23	I_{VGAP}			20	µA	
	Supply current	For cellular band, No RF applied	28	I_{DRVA}		15.7		mA	
		Bit 2 = 1, No RF applied	28	I_{DRVAB}		31		mA	
	Supply current	For PCS band, No RF applied	28	I_{DRVA}		15.6		mA	
		Bit 2 = 1, No RF applied	28	I_{DRVAB}		31		mA	
		No RF applied	28	I_{DRVP}		<1		µA	
	Current consumption	Cell high output	26, 27	Ic		105		mA	
		Cell low output	26, 27	Ic		92		mA	
	Current consumption	PCS high output	29, 30	Ic		105		mA	
		PCS low output	29, 30	Ic		92		mA	
	TCXO input								
	Frequency range	Sine wave 250 mVp	4	f_{TCXO}	15	20	25	MHz	
	Input-voltage range	Sine wave	4	V_{TCXO}	100	250	600	mVp	

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics

V_S = 3 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Cell_LO input								
	Frequency range.	50Ω source	1	f_{cell}	800		1100	MHz	
	Input power range	50Ω source	1	V_{cell}	-3	0		dBm	
	Input impedance	Active & standby	1	Z_{cell}		43		W	
	Input inductance	Active & standby	1	L_{cell}		1.4		nH	
	PCS_LO input								
	Frequency range.	50Ω source	2	f_{PCS}	1500		2100	MHz	
	Input power range	50Ω source	2	V_{PCS}	-3	0		dBm	
	Input impedance	Active & standby	2	Z_{PCS}		43		W	
	Input inductance	Active & standby	2	L_{PCS}		1.4		nH	
	IF_VGA input (Tank3, Tank4)								
	Frequency range.	400Ω source	20, 21	f_{VGA}	120		140	MHz	
	Input voltage range	400Ω source	20, 21	V_{VGA}	-7	-5		dBm	
	Input impedance	Active & standby	20, 21	Z_{VGA}		400		Ω	
	Input capacitance	Active & standby	20, 21	C_{VGA}				pF	
	Vcntrl input, gain								
	Input voltage range	500Ω source	24	V_{VGA}	0		2.2	Vp	
	Input impedance	Active & standby	24	Z_{VGA}		3000		W	
	Input capacitance	Active & standby	24	C_{VGA}				pF	
	I/Q modulator base band inputs I+, I-, Q+ and Q-								
	DC voltage	Referred to GND	13,14 15,16	V_I, V_{NI}, V_Q, V_{NQ}	1.35	VS1/2	VS1/2 + 0.1	V	
	MD_IQ	Frequency range	13,14 15,16	FR_{IQ}	DC		1	MHz	
	AC voltage	Referred to GND	13,14 15,16	$AC_{I,I+,Q,Q+}$		130		mVpp	
	AC voltage	Differential (preferred)	13,14 15,16	$AC_{DI,DQ}$		260		mVpp	
	VCO Tank1 and Tank2								
	Resonator	Frequency range	7, 8	FR_{MDLO}	100		600	MHz	
	Q factor	Unloaded	7, 8	Q_{LO}	40				
	Characteristic impedance	Unloaded	7, 8			tbd		Ω	
	I/Q modulator outputs; Tank1 and Tank2								
	DC current	$V_{Tank4,}$ V_{Tank3}= Vcc	18,19	I_{Tank1}.I_{Tank2}		1		mA	
	Voltage compliance		18,19	$V_{Tank1,}$ V_{Tank2}	Vcc-0.7		Vcc	V	
	IQ output voltage (differential)	Tank circuit	18,19	V_{IQ}	40		60	mVeff	
	Carrier suppression[1)]		18,19	CS_{IQ}	-30	-35		dBc	

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics

V_S = 3 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Sideband suppression[1)]		18,19	SS_{MDO}	-45	-50		dBc	
	IF spurious[1)]	f_{LO} +/- 3*f_mod	18,19	SP_{IQ}	-55	-60		dBc	
	Frequency range		18,19	f_{IQ}		150		MHz	
	Cellular upconverter (800 MHz)								
	Output frequency		26, 27	f_{cell}	824	836	849	MHz	
	RF input level	0.5 - 2GHz	26, 27	$P8_{RF}$	-13	-11		dBm	
	LO-spurious at RF/NRF port	@ $P8_{MIXLO}$ = -3 dBm @ $P8_{RF}$ = -11 dBm	26, 27	$SP8_{RF}$	-28	-30		dBm	
	MIXLO input level	0.05 - 2 GHz	26, 27	$P8_{MIXLO}$	-3	0		dBm	
	Carrier suppression	@ $P8_{MIXLO}$ = -11 dBm	26, 27	$CS8_{MIXO}$	-27			dBc	
	PCS upconverter (1900 MHz)								
	Output frequency		29, 30	f_{PCS}	1560	1750	1950	MHz	
	RF input level	0.5 - 2GHz	29, 30	$P19_{RF}$	-13	-11		dBm	
	LO-spurious at RF/NRF port	@ $P19_{MIXLO}$ = -10 dBm @ $P19_{RF}$ = -17 dBm	29, 30	$SP19_{RF}$				dBm	
	MIXLO input level	0.05 - 2 GHz	29, 30	$P19_{MIXLO}$	-3	0		dBm	
	Noise	@ 1MHz off carrier	18,19	N_{IQ}	-142			dBm/ √Hz	
	Carrier suppression	@ $P19_{MIXLO}$ = -17 dBm	29, 30	$CS19_{MIXO}$	-20			dBc	
	Cell output high power								
	Frequency range	CELL_A/B	26, 27	f_{cell}	730		970	MHz	
	Output power	CELL_A/B	26, 27	Pout		7.7		dBm	
	Adjacent channel power	CELL_A/B	26, 27	ACP		-54		dBc	
	Receive band noise	CELL_A/B	26, 27	RX noise		-130		dBm/ √Hz	
	Cell output low power								
	Frequency range	CELL_A/B	26, 27	f_{cell}	730		970	MHz	
	Output power	CELL_A/B	26, 27	Pout		-90		dBm	
	PCS output high power								
	Frequency range	PCS_A/B	29, 30	f_{PCS}	1830		2130	MHz	
	Output power	PCS_A/B	29, 30	Pout		8.2		dBm	
	Adjacent channel power	PCS_A/B	29, 30	ACP		-54		dBc	

1) I/Q base band input: differential sin( ), and cos( ) signals with 200 mVamplitude (400 mV_{PP}) and 100 kHz frequency from a low ohmic source (< 1kΩ).

2) -1 dB compression point, external load C=1.5pF to GND

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics

V_S = 3 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Receive band noise	PCS_A/B	29, 30	RX noise		-132		dBm/ √Hz	
	Current consumption		29, 30	Ic		105		mA	
	PCS output low power								
	Frequency range	PCS_A/B	29, 30	f_{PCS}	1830		2130	MHz	
	Output power	PCS_A/B	29, 30	Pout		-90		dBm	
	Current consumption		29, 30	Ic		92		mA	
	Logic inputs								
	Voltage level	Logical High	10, 11, 12, 25, 31		Vcc-0.3	3	Vcc	V	
	Voltage level	Logical low			0	0	0.3	V	
	Current					0.7		mA	
	3-wire bus								
	Clock period		10, 11, 12	TPER		100		ns	
	Rise time			TR		10		ns	
	Fall time			TF		10		ns	
	Set time data to clock			TS		35		ns	
	Hold time data to clock			TH		35		ns	
	Clock pulse width			TC		50		ns	
	Set time enable to clock			TL		40		ns	
	Set time Data to neg. going clock edge			TSC		10		ns	
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

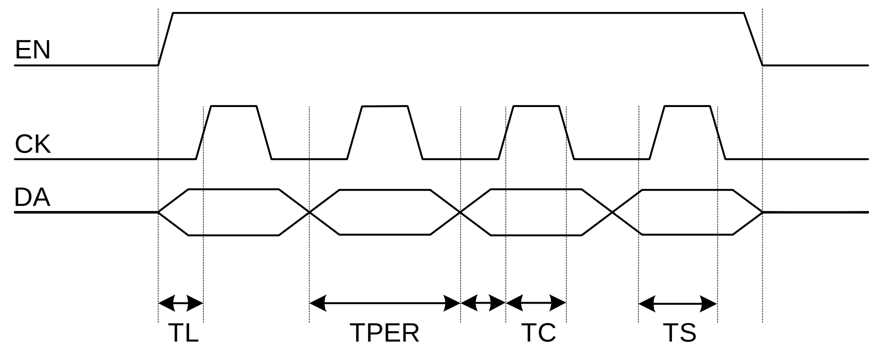
Function Select Table

Signal	Level	Description
Vctrl	High	High output power (Cellular +7dBm, PCS +8dBm)
	Low	Low output power (Cellular –90dBm, PCS –90dBm)
TX ON	High	Transmittpath on
	Low	Transmittpath off (PLL with Bit 3 active)
DRV SEL	High	Driver B active (Bit 2 low), no effect with Bit2 high
	Low	Driver A active (Bit 2 low), no effect with Bit2 high

3-Wire Bus Timing Diagram

Enable 'high' selects the T0345. Data are clocked into the shift register with the falling edge of the CK signal.

Figure 3.



Mode Selection

Function	TXON	DRV SEL	Bit 1	Bit 2	Bit 3
Turn on cellular mode	1	1	1	1	0
Turn on PCS mode	1	1	1	1	1
Turn on cellular driver A	1	0	1	0	0
Turn on cellular driver B	1	1	1	0	0
Turn on PCS driver A	1	0	1	0	1
Turn on PCS driver B	1	1	1	0	1
Idle mode	0	x	0	x	x
Turn on bandgap / PLL	0	x	1	x	x
Not allowed	1	1	0	1	1
Note: x -> don't care					

Equivalent Circuits

Figure 4. II/Q modulator

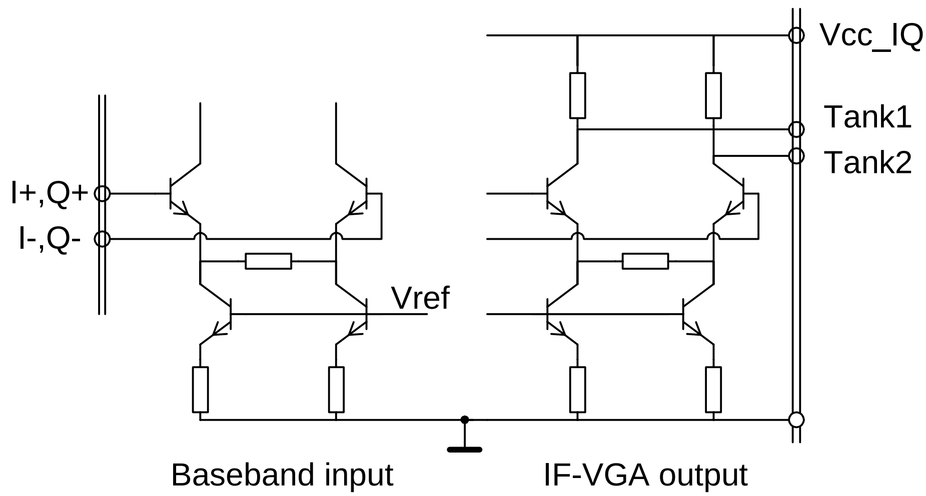


Figure 5. IF input mixer

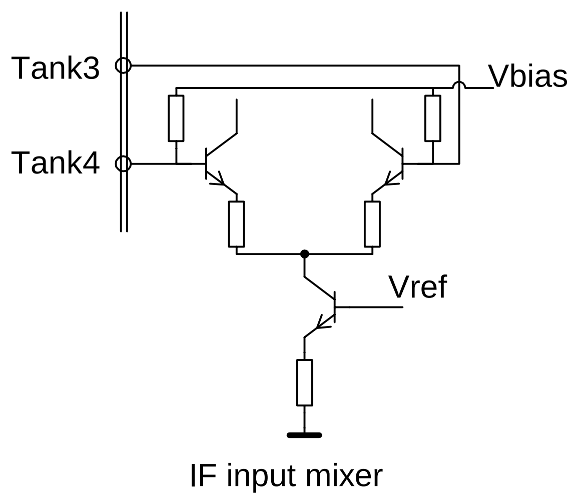


Figure 6. RF LO input

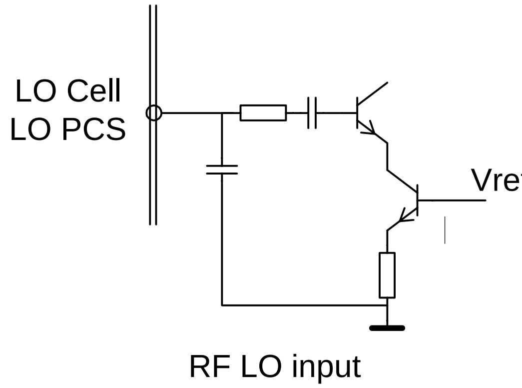


Figure 7. PA output

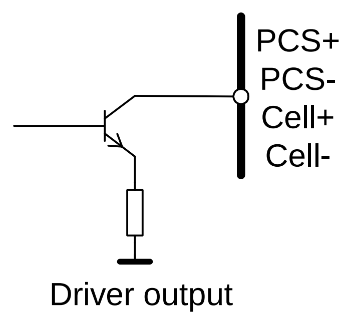


Figure 8. Charge pump

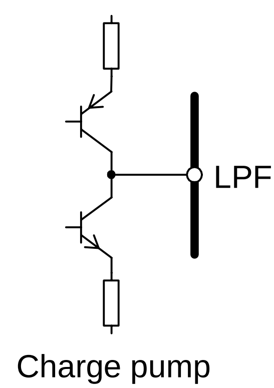


Figure 9. TX ON

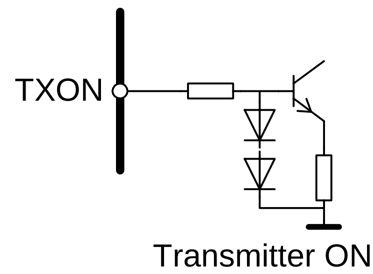


Figure 10. DRV sel

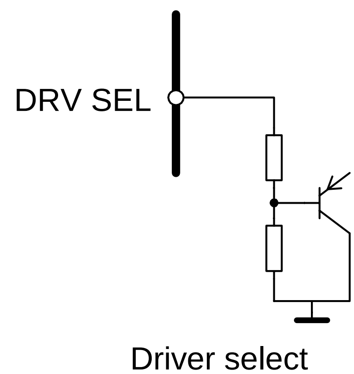


Figure 11. Gain input

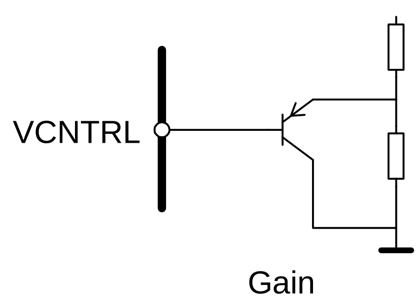
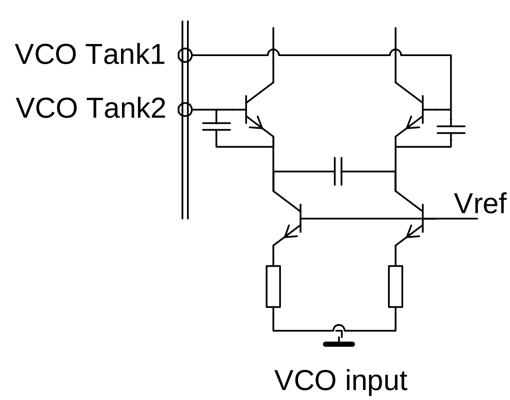


Figure 12. VCO input



Measurement Results

IF VCO

Figure 13. Control voltage vs. time

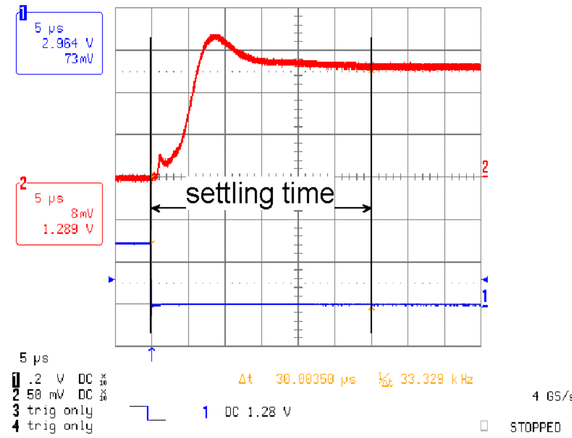


Figure 14. Output power, ACPR, I_{CC} vs. VCNTRL (CELL+)

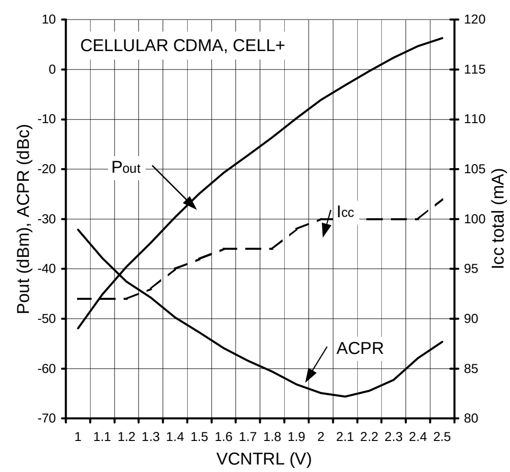


Figure 15. Output power, ACPR, I_{CC} vs. VCNTRL (PCS+)

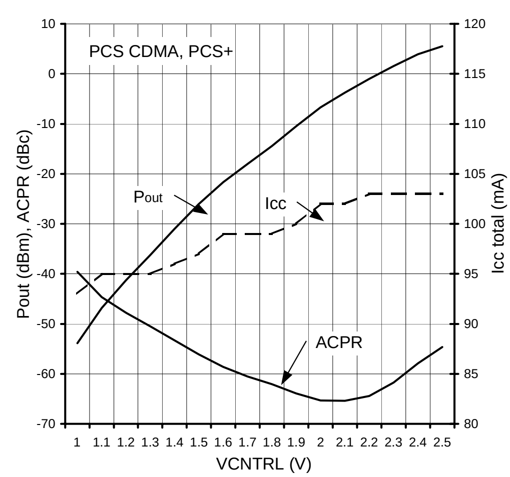


Figure 16. Output power vs. VCNTRL (CELL+)

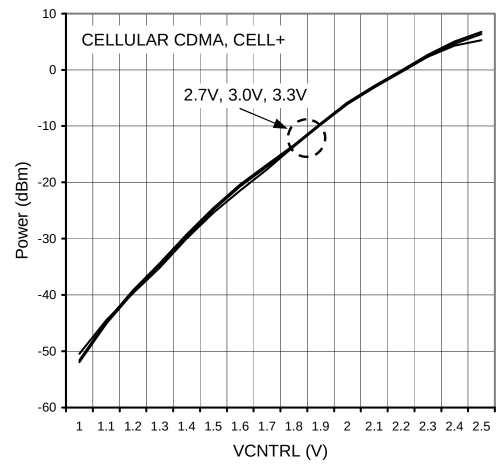


Figure 17. Output power vs. VCNTRL (CELL+) at -25°C, 27°C and 95°C

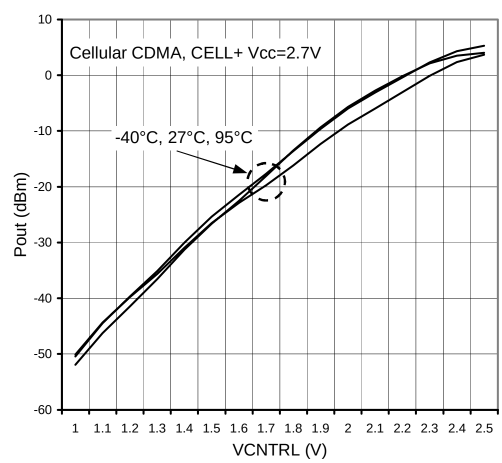


Figure 18. Output power vs. VCNTRL (PCS+)

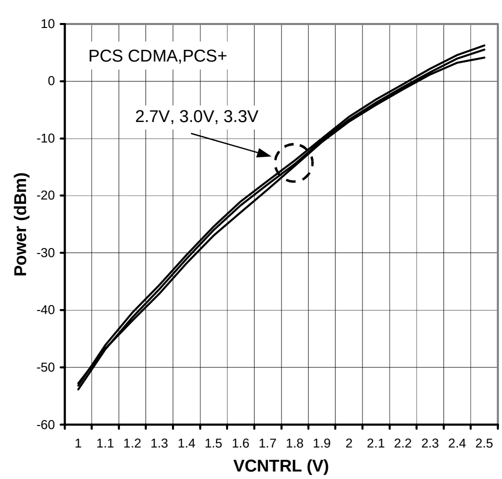


Figure 19. Output power vs. VCNTRL (PCS+) at -25°C, 27°C and 95°C

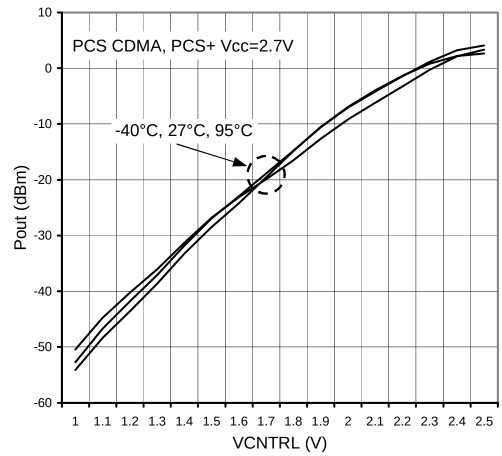


Figure 20. Output power, ACPR vs. LO power

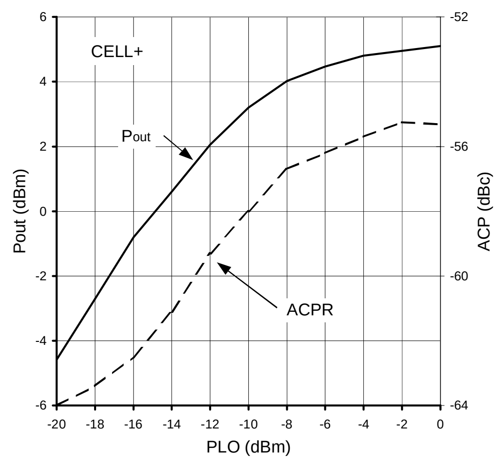


Figure 21. Output power vs. frequency cellular band (700 MHz to 1000 MHz)

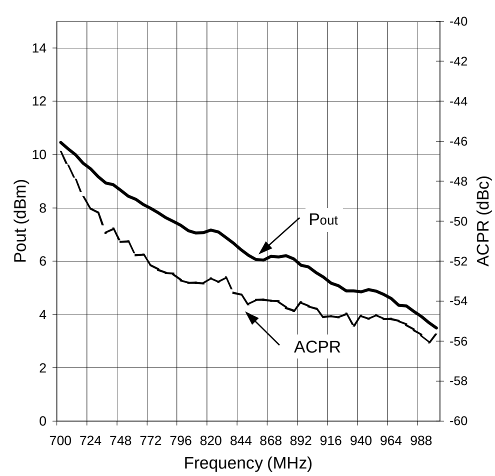
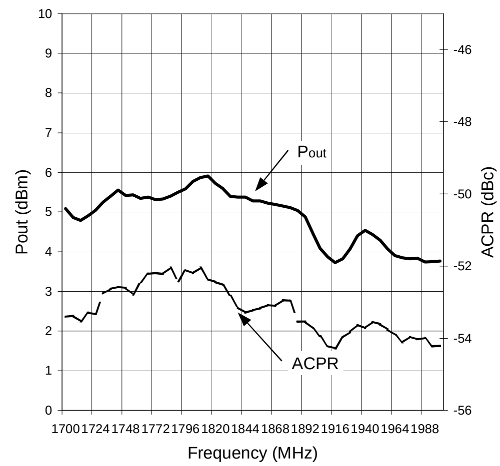


Figure 22. Output power vs. frequency cellular band (1700 MHz to 2000 MHz



Sideband suppression and LO feed through Ce(Tank 1 and Tank 2)

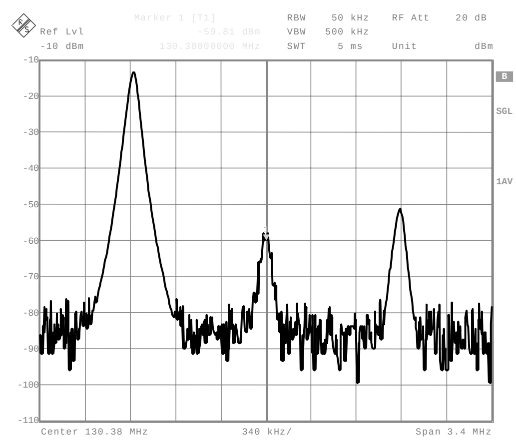


Figure 23. I/Q baseband frequency response (Tank1 and Tank2)

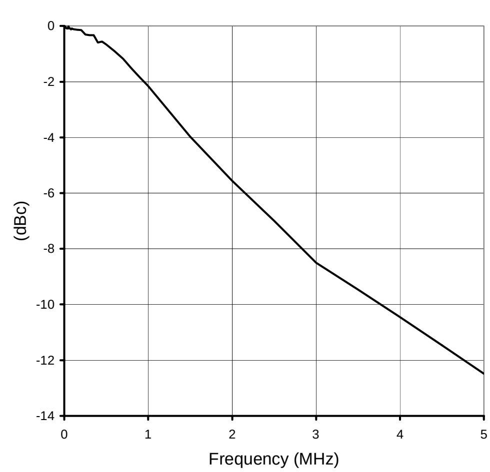


Figure 24. Cell+ output spectrum

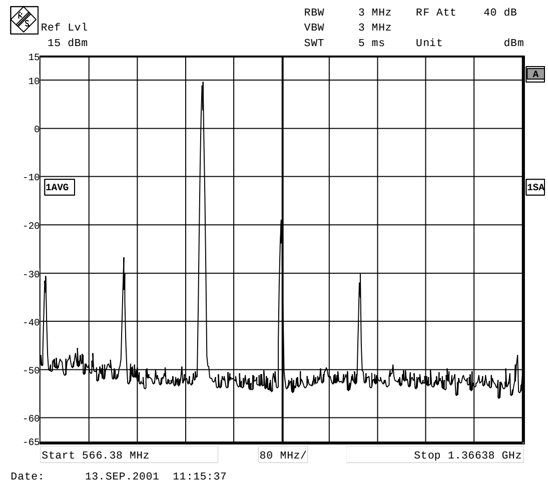


Figure 25. PCS+ output spectrum

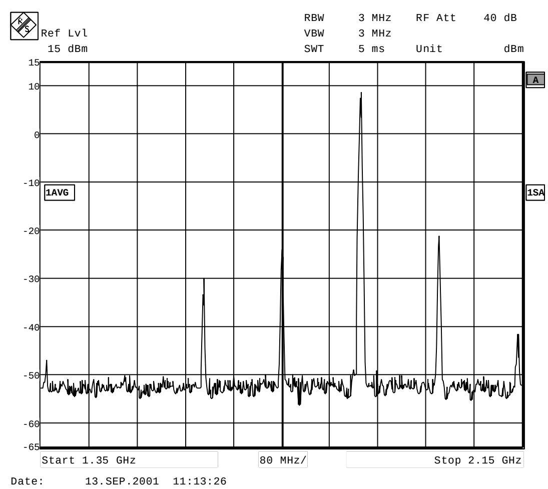


Figure 26. CELL+ cascade ACPR vs. P_{out} and V_{cc}

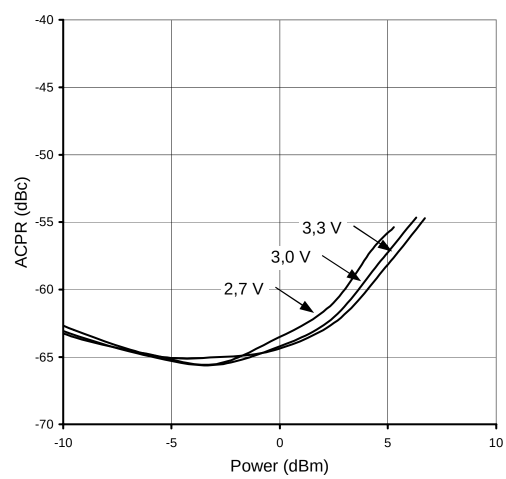


Figure 27. PCS+ cascade ACPR vs. P_{out} and V_{cc}

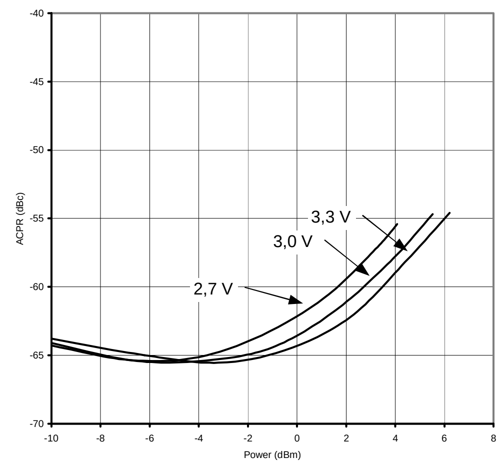


Figure 28. Icc vs. CELL+ output power (836 MHz)

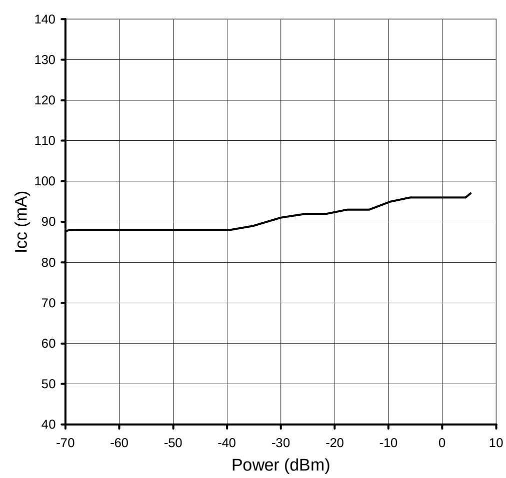


Figure 29. Icc vs. PCS+ output power (1880 MHz)

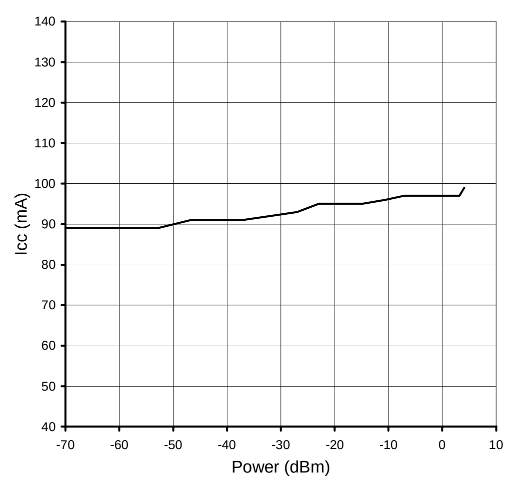


Figure 30. LO cell port S11

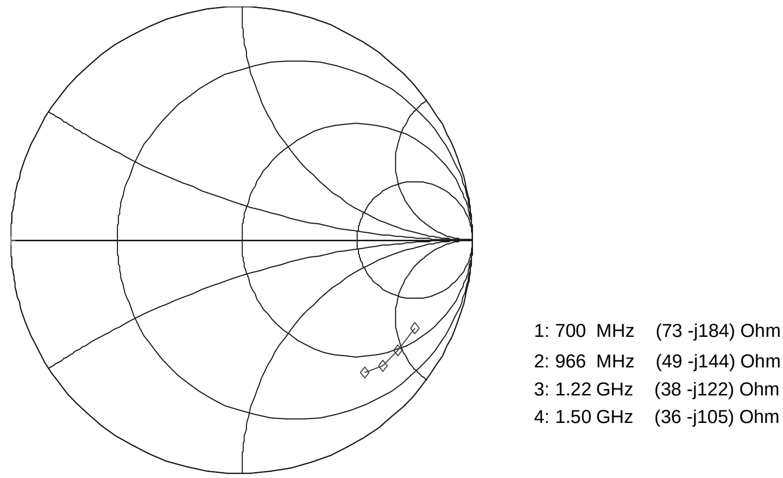
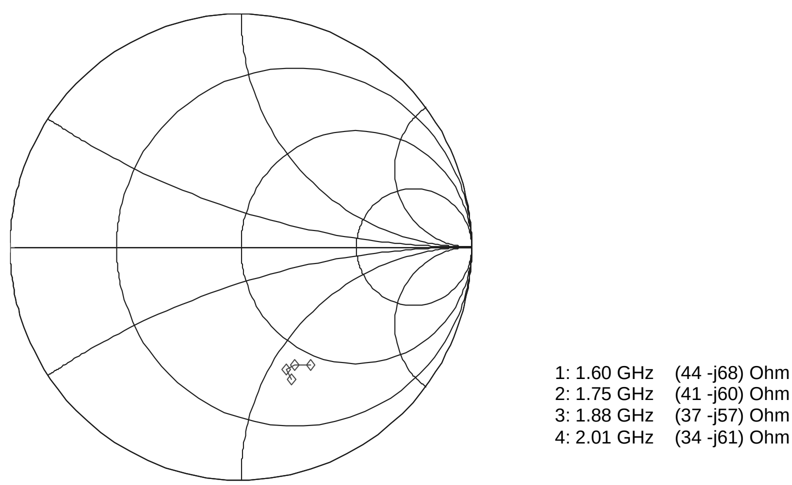
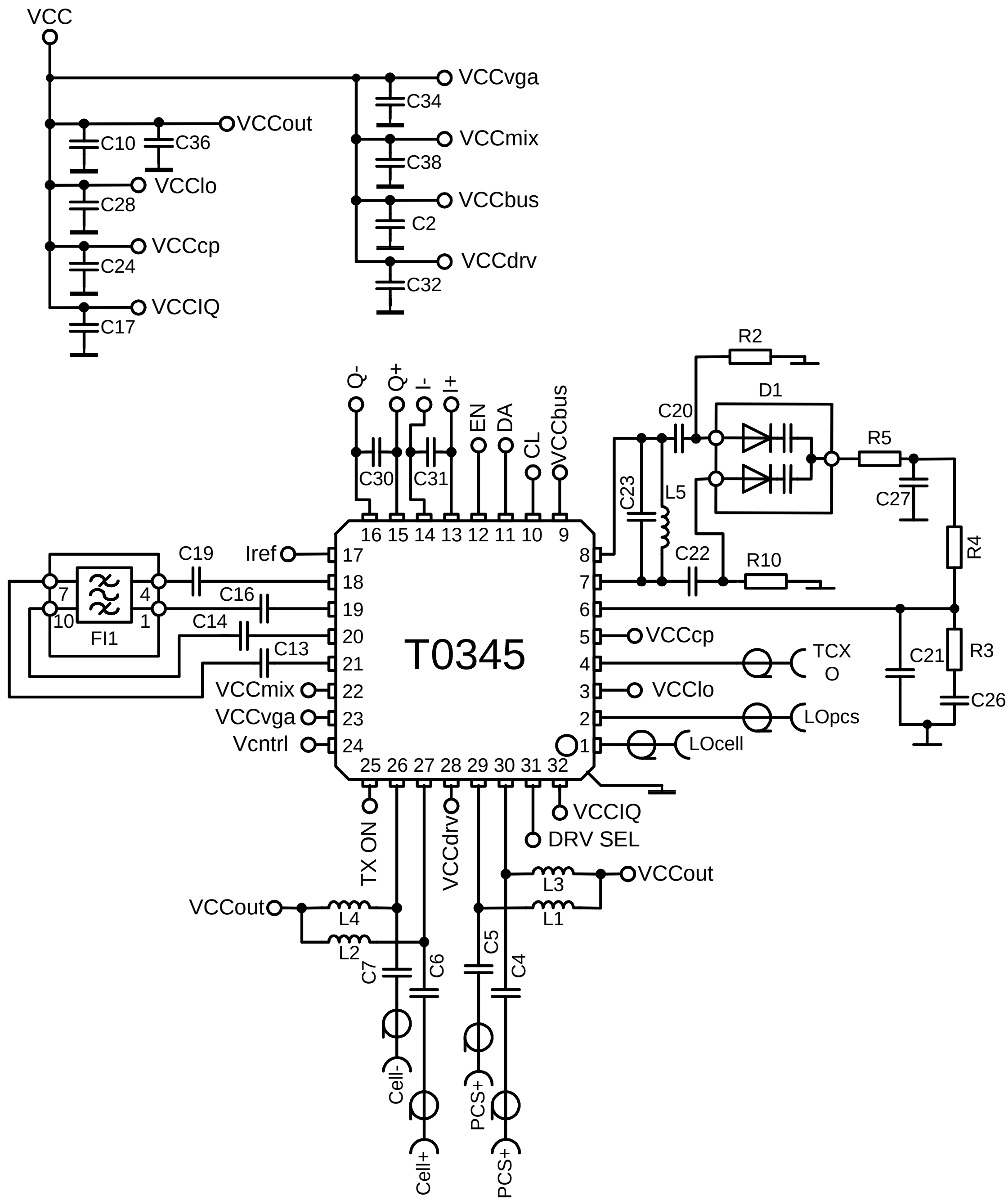


Figure 31. LO PCS port S11



Demo Board Schematics

Figure 32. Application circuit



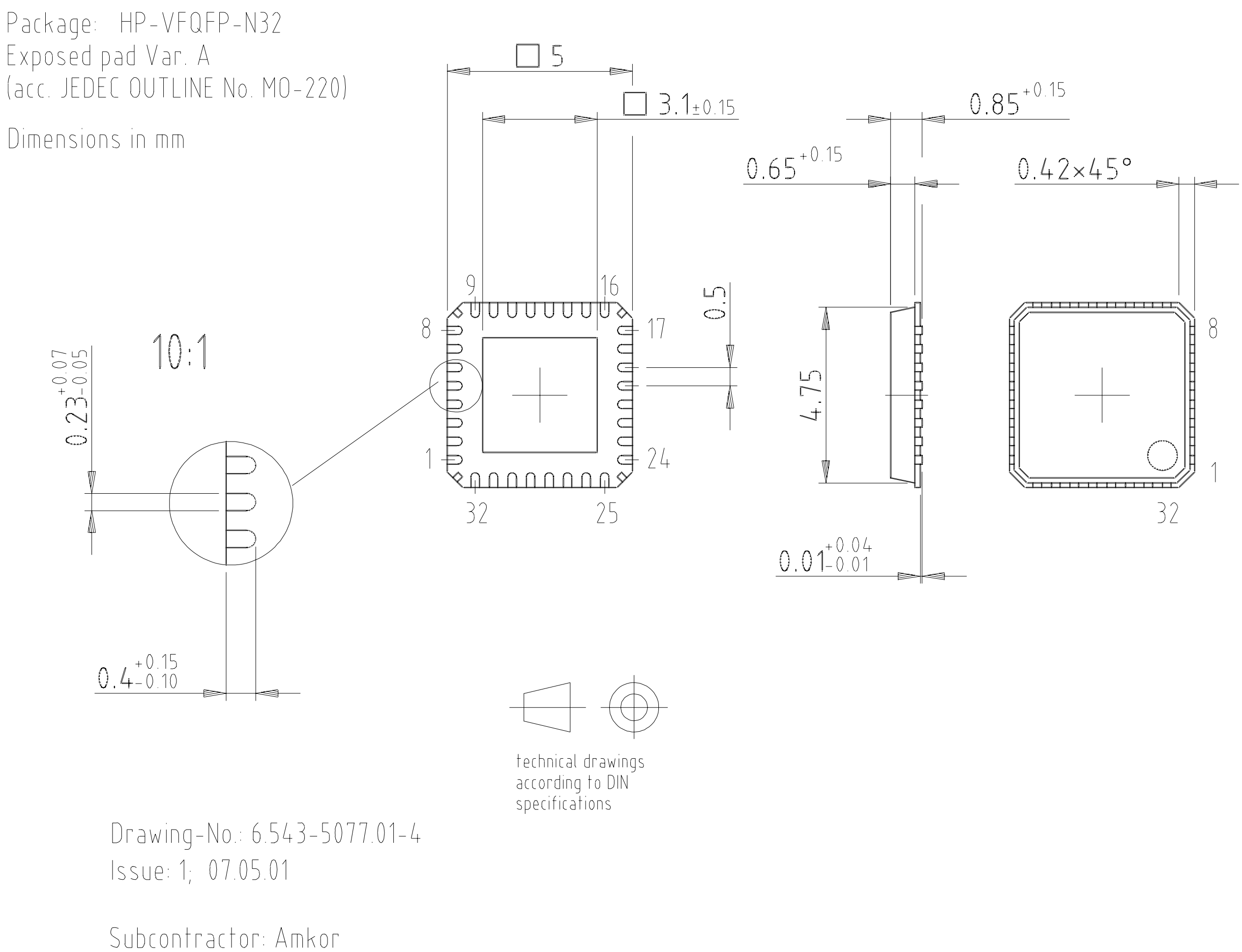
<u>Remark:</u> The lines which connects both LOs, the TCXO and the output lines need to be designed with 50 Ohm impedance !

Bill of Materials of Demo Board

Component	Reference	Part Number	Value	Size / Package
Transmitter IC	IC3	T0345 (ATMEL)		MLF32-55
ZF-Filter	FI1	LFSH30N/nc (Murata)	130.38MHz	LFSH30
Varactor-Diode	D1	BBY53-05/06 (Infineon)		SOT-23
Inductor	L5	0805CS-220_X_B (Coilcraft)	18n	0805
Inductor	L1, L3		4n7	0402(1)
Inductor	L2, L4		15n	0402(1)
Capacitor	C4, C5		22p	0402(1)
Capacitor	C10, C17, C28, C38		100n	0402(1)
Capacitor	C30, C31		68p	0402(1)
Capacitor	C13, C14, C16, C19		10n	0402(1)
Capacitor	C20, C22		8p2	0402(1)
Capacitor	C21		82p	0402(1)
Capacitor	C27		3p9	0402(1)
Capacitor	C2, C6, C7, C24, C32, C34		100p	0402(1)
Capacitor	C26		1n8	0402(1)
Resistor	R5		1k	0402(1)
Resistor	R3		6k8	0402(1)
Resistor	R2, R10		2k7	0402(1)
Resistor	R4		12k	0402(1)

Package Information

Figure 33.



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved fron the Internet: http://www.atmel-wm.com

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