SLVS387B – APRIL 2001 – REVISED DECEMBER 2002

BACKUP-BATTERY SUPERVISORS FOR RAM RETENTION

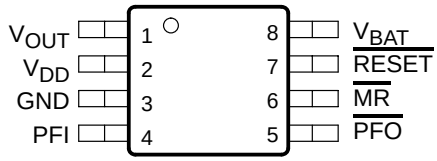
FEATURES

- **Supply Current of 40 μA (Max)**
- **Battery-Supply Current of 100 nA (Max)**
- **Precision Supply Voltage Monitor 3.3 V, 5 V, Other Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Voltage Monitor For Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal**
- **Pin-For-Pin Compatible With MAX819, MAX703, and MAX704**
- **8-Pin MSOP Package**
- **Temperature Range –40°C to 85°C**

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery-Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point of Sale Equipment**

DGK PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS3619 family of supervisory circuits monitor and control processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above V_{IT}. When the supply voltage drops below V_{IT}, the output becomes active (low) again.

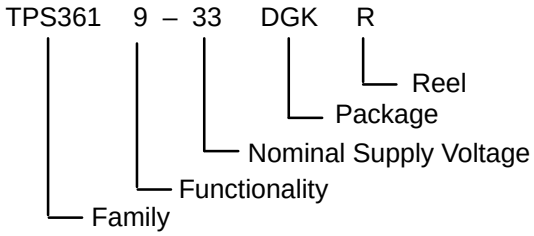
The product spectrum is designed for supply voltages of 3.3 V and 5 V. The circuits are available in an 8-pin MSOP package. The TPS3619 devices are characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME	MARKING
–40°C to 85°C	TPS3619–33DGKR†	AFL
	TPS3619–50DGKR†	AFM

† The DGKR passive indicates tape and reel of 2,500 parts.

standard and application specific versions†



DEVICE NAME	NOMINAL VOLTAGE†, V_{NOM}
TPS3619x33 DGK	3.3 V
TPS3619x50 DGK	5.0 V

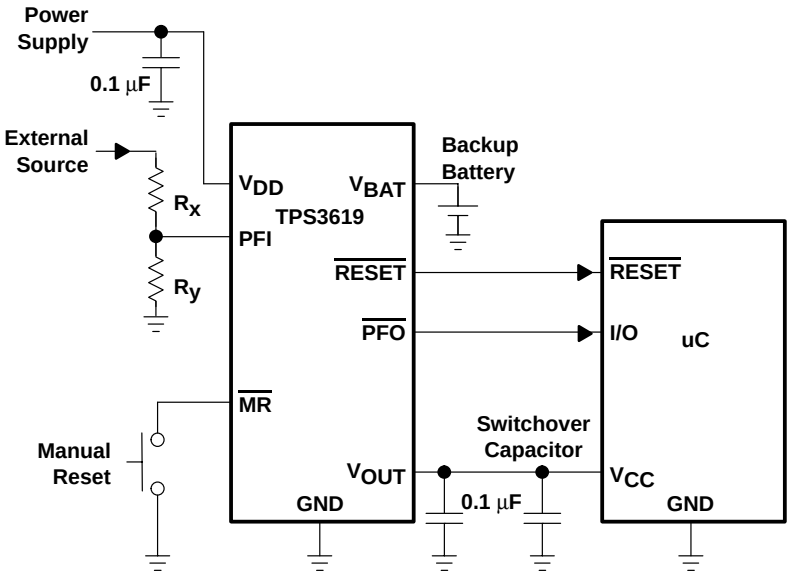
† For other threshold voltage versions, contact the local TI sales office for availability and lead-time.

FUNCTION TABLE (TPS3619)

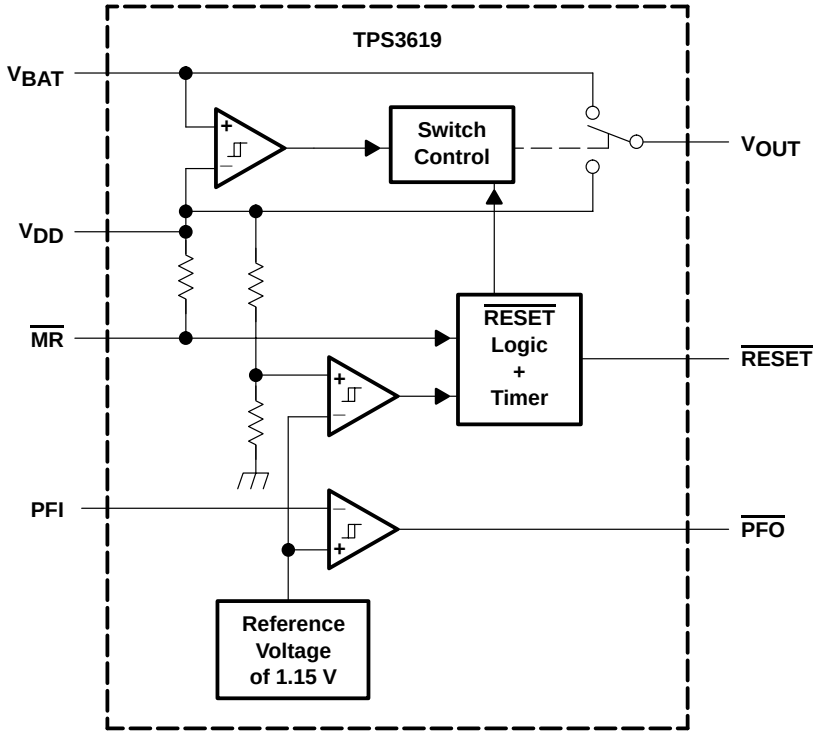
$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	$\overline{MR}$	V_{OUT}	$\overline{RESET}$
0	0	0	V_{BAT}	0
0	0	1	V_{BAT}	0
0	1	0	V_{DD}	0
0	1	1	V_{DD}	0
1	0	0	V_{DD}	0
1	0	1	V_{DD}	1
1	1	0	V_{DD}	0
1	1	1	V_{DD}	1

$PFI > V_{PFI}$	$\overline{PFO}$
0	0
1	1
COND.: VDD > VDD_MIN	

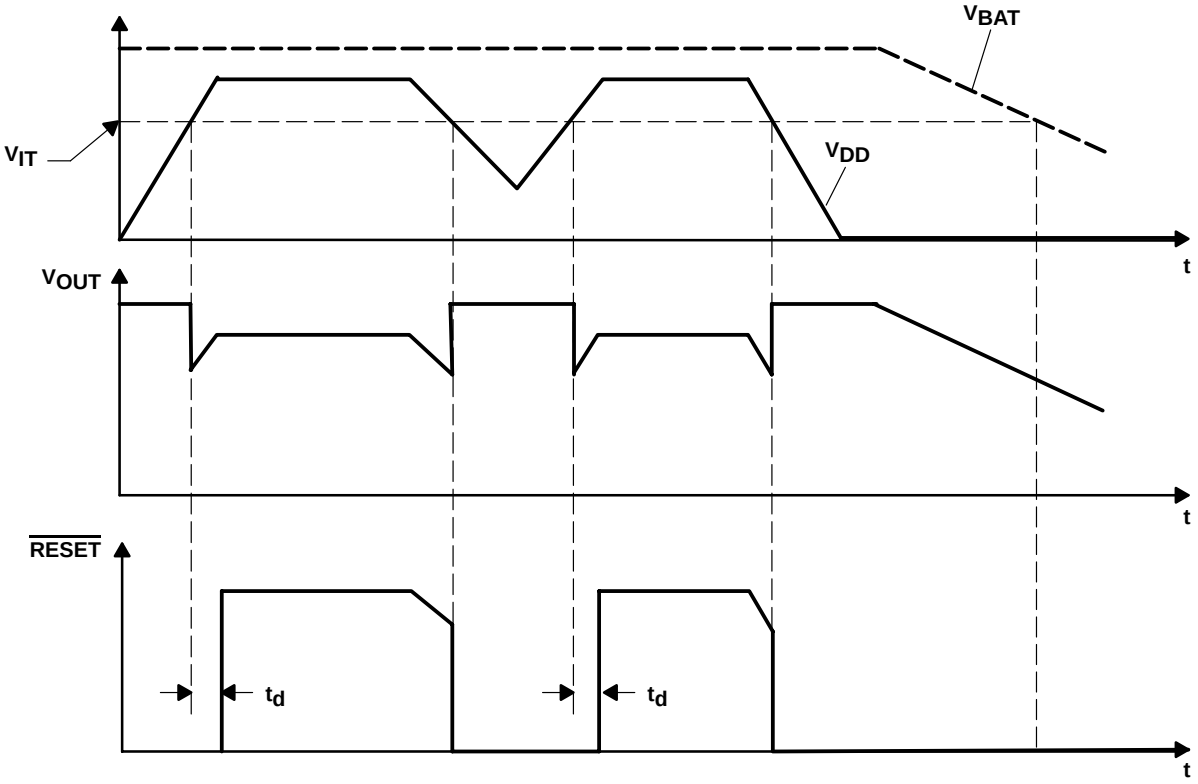
typical operating circuit



functional block diagram



timing diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	3	I	Ground
$\overline{MR}$	6	I	Manual reset input
PFI	4	I	Power-fail comparator input
$\overline{PFO}$	5	O	Power-fail comparator output
$\overline{RESET}$	7	O	Active-low reset output
V_{BAT}	8	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output

detailed description

battery freshness seal

The battery freshness seal of the TPS3619 family disconnects the backup-battery from internal circuitry until it is needed. This function ensures that the backup-battery connected to V_{BAT} is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode.

1. Connect V_{BAT} ($V_{BAT} > V_{BAT}$min)
2. Ground $\overline{PFO}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and keep connected for 5 ms < t < 35 ms

The battery freshness seal mode is disabled by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

detailed description (continued)

power-fail comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold $V_{IT(PFI)}$ of typical 1.15 V, the power-fail output ($\overline{PFO}$) goes low. If $V_{IT(PFI)}$ goes above $V_{(PFI)}$, plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to assure that the current in the PFI pin can be ignored compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, PFI should be connected to ground and $\overline{PFO}$ left unconnected.

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup-battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup-battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

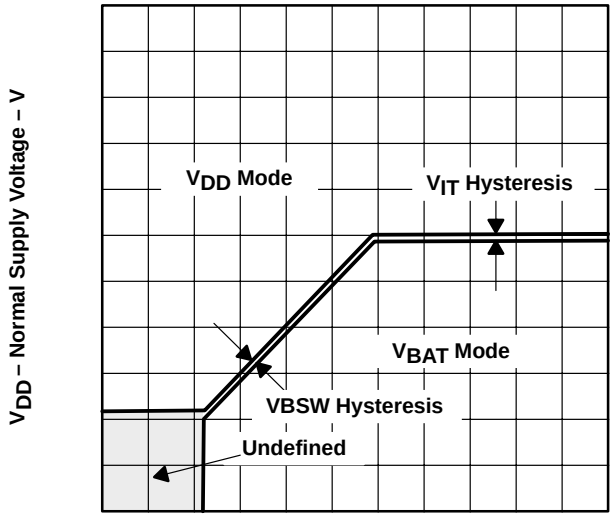


Figure 1. Normal Supply Voltage vs Backup-Battery Supply Voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{DD} (see Note1) . . . . . 7 V
$\overline{MR}$ and PFI pins (see Note 1) . . . . . –0.3 V to (V_{DD} + 0.3 V)
Continuous output current: V_{OUT}, I_O . . . . . 400 mA
All other pins, I_O (see Note 1) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD}+0.3	V
High-level input voltage, V_{IH}	0.7xV_{DD}		V
Low-level input voltage, V_{IL}		0.3xV_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at $\overline{MR}$		100	ns/V
Slew rate at V_{DD} or V_{BAT}, $\Delta t/\Delta V$		1	V/µs
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V,	I_{OH} = –400 µA	V_{DD} – 0.2 V			V
			V_{DD} = 3.3 V,	I_{OH} = –2 mA	V_{DD} – 0.4 V			
			V_{DD} = 5 V,	I_{OH} = –3 mA	V_{DD} – 0.4 V			
		$\overline{PFO}$	V_{DD} = 1.8 V,	I_{OH} = –20 µA	V_{DD} – 0.3 V			V
			V_{DD} = 3.3 V,	I_{OH} = –80 µA	V_{DD} – 0.4 V			
			V_{DD} = 5 V,	I_{OH} = –120 µA	V_{DD} – 0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{DD} = 1.8 V,	I_{OL} = –400 µA			0.2	V
			V_{DD} = 3.3 V,	I_{OL} = 2 mA			0.4	
			V_{DD} = 5 V,	I_{OL} = 3 mA			0.4	
V_{res}	Powerup reset voltage (see Note 2)		I_{OL} = 20 µA, V_{BAT} > 1.1 V or V_{DD} > 1.1 V				0.4	V
V_{OUT}	Normal mode		I_{OUT} = 8.5 mA, V_{BAT} = 0 V	V_{DD} = 1.8 V,	V_{DD} – 50 V			V
			I_{OUT} = 125 mA, V_{BAT} = 0 V	V_{DD} = 3.3 V,	V_{DD} – 150 V			
			I_{OUT} = 200 mA, V_{BAT} = 0 V	V_{DD} = 5 V,	V_{DD} – 200 V			
	Battery-backup mode		I_{OUT} = 0.5 mA, V_{BAT} = 1.5 V	V_{DD} = 0 V,	V_{BAT} – 20 mV			V
			I_{OUT} = 7.5 mA, V_{BAT} = 3.3 V		V_{BAT} – 113 mV			
$r_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V			0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{DD} = 3.3 V			8	15	
$V_{IT–}$	Negative-going input threshold voltage (see Note 3)	TPS3619-33	T_A = –40°C to 85°C		2.88	2.93	3	V
		TPS3619-50			4.46	4.55	4.64	
V_{PFI}		PFI			1.13	1.15	1.17	
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V			20		mV
			2.5 V < V_{IT} < 3.5 V			40		
			3.5 V < V_{IT} < 5.5 V			60		
		PFI				12		
		VBSW (see Note 4)	V_{DD} = 1.8 V			55		
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 x V_{DD}	V_{DD} = 5 V	–33		–76	µA
I_{IL}	Low-level input current		$\overline{MR}$ = 0 V		–110		–255	
I_I	Input current	PFI			–25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V	V_{DD} = 1.8 V			–0.3	mA
				V_{DD} = 3.3 V			–1.1	
				V_{DD} = 5 V			–2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}				40	µA
			V_{OUT} = V_{BAT}				40	
$I_{(BAT)}$	V_{BAT} supply current		V_{OUT} = V_{DD}		–0.1		0.1	µA
			V_{OUT} = V_{BAT}				0.5	
C_i	Input capacitance		V_I = 0 V to 5 V			5		pF

NOTES: 2. The lowest supply voltage at which RESET becomes active. $t_{r,VDD} \geq 15$ µs/V
3. To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
4. For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} – 0.2$ V	6			µs
		at $\overline{MR}$	$V_{DD} = V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram	60	100	140	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT} – 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V		2	5	µs
		PFI to $\overline{PFO}$ delay	$V_{IL} = V_{PFI} – 0.2$ V, $V_{IH} = V_{PFI} + 0.2$ V		3	5	
		$\overline{MR}$ to $\overline{RESET}$	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		0.1	1	

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

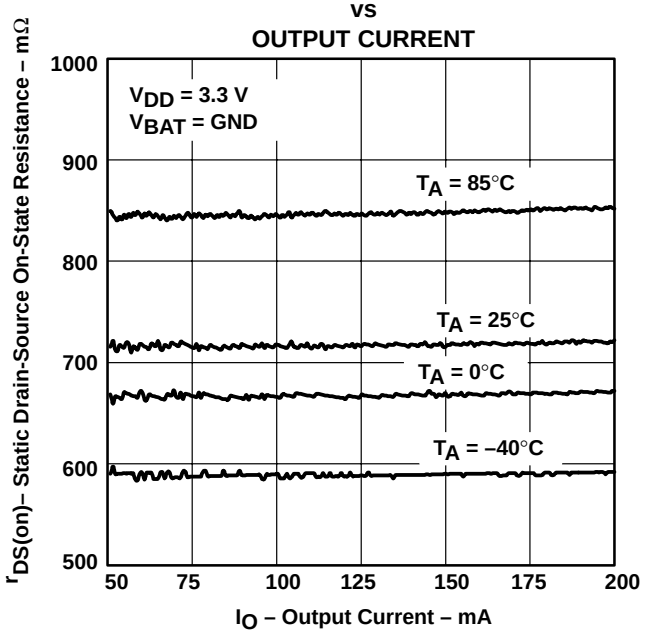


Figure 2

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

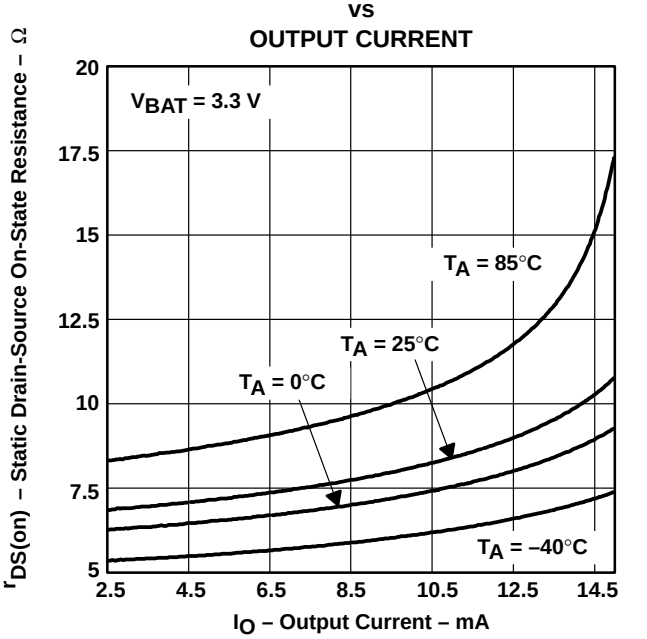


Figure 3

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

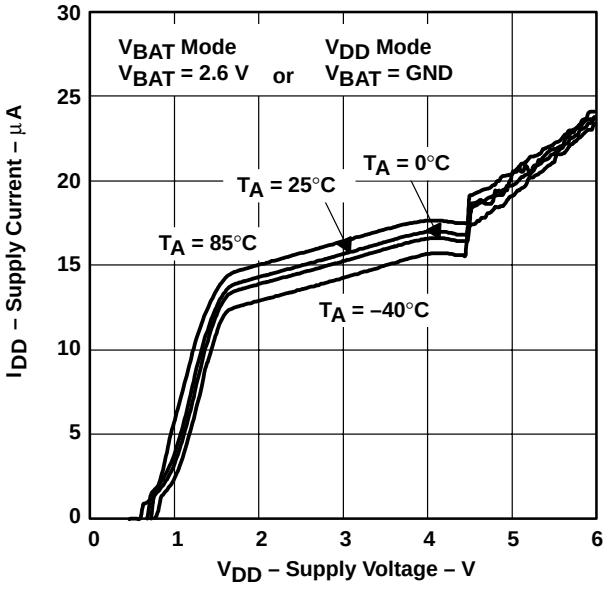


Figure 4

NORMALIZED THRESHOLD AT $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

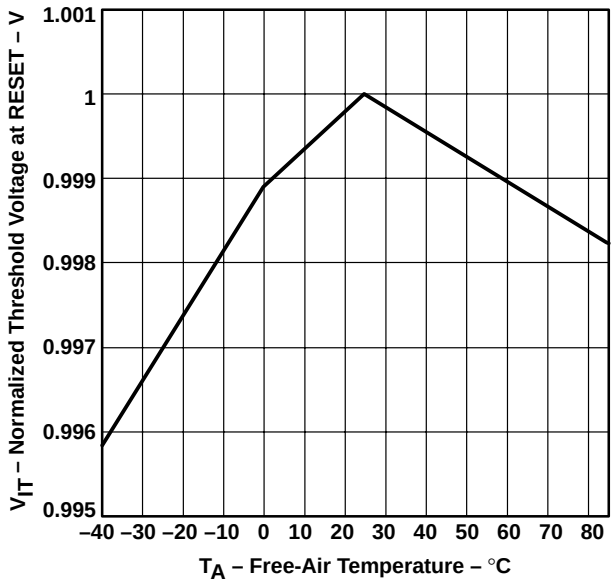


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs HIGH-LEVEL OUTPUT CURRENT

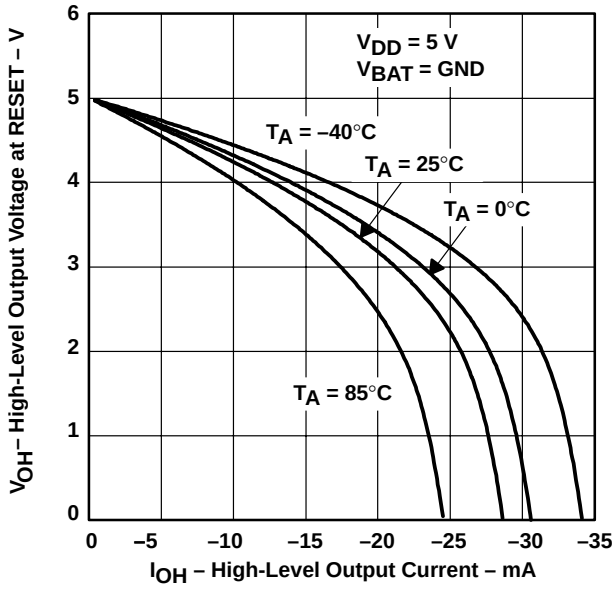


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs HIGH-LEVEL OUTPUT CURRENT

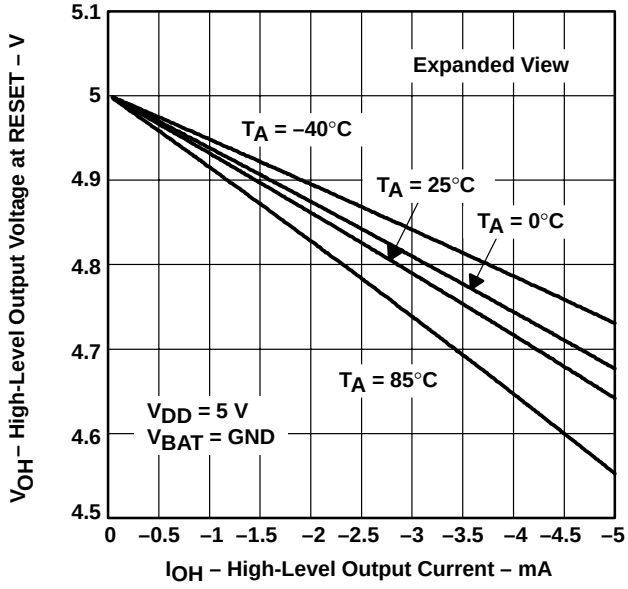


Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{PFO}$ vs HIGH-LEVEL OUTPUT CURRENT

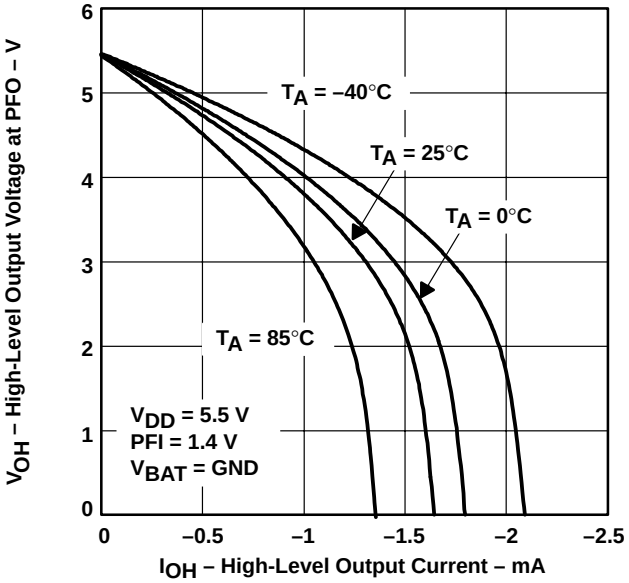


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{PFO}$ vs HIGH-LEVEL OUTPUT CURRENT

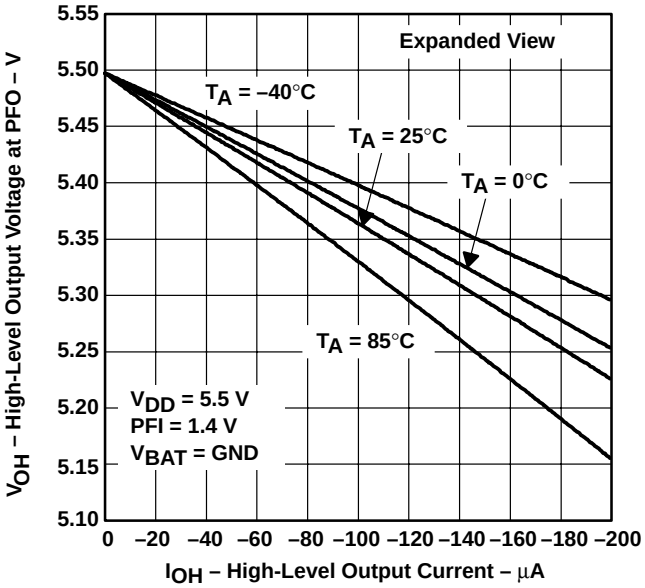


Figure 9

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{RESET}$ vs LOW-LEVEL OUTPUT CURRENT

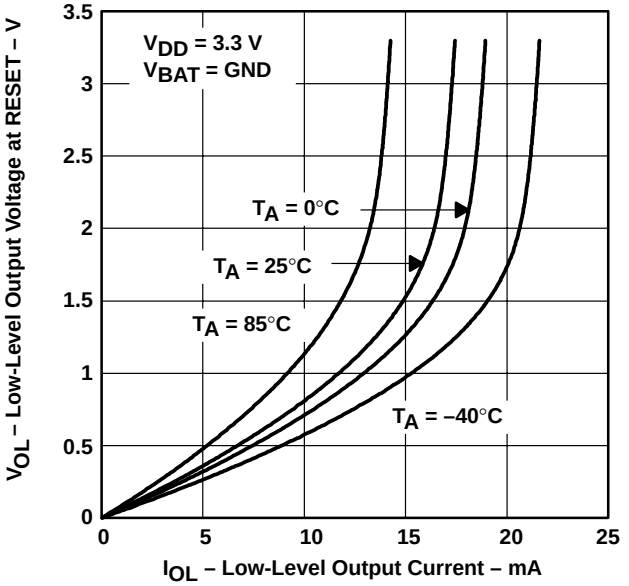


Figure 10

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{RESET}$ vs LOW-LEVEL OUTPUT CURRENT

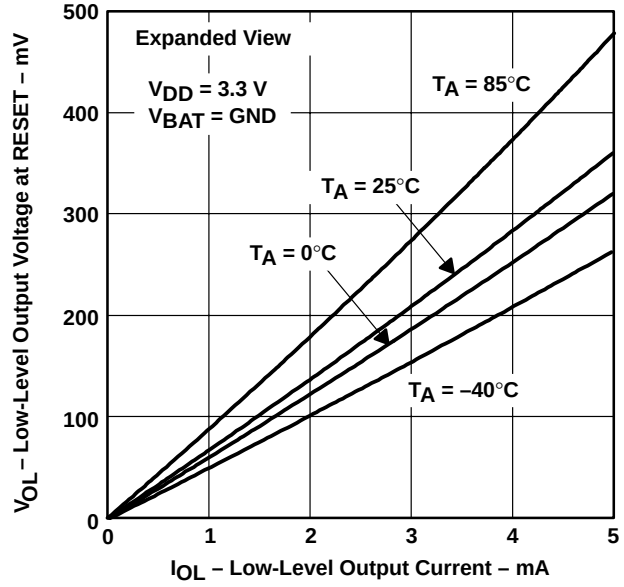


Figure 11

TYPICAL CHARACTERISTICS

MINIMUM PULSE DURATION AT V_{DD} vs THRESHOLD OVERDRIVE AT V_{DD}

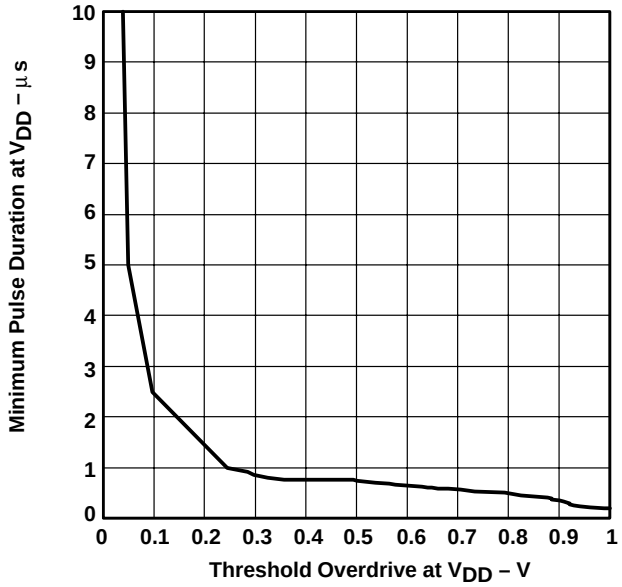


Figure 12

MINIMUM PULSE DURATION AT PFI vs THRESHOLD OVERDRIVE AT PFI

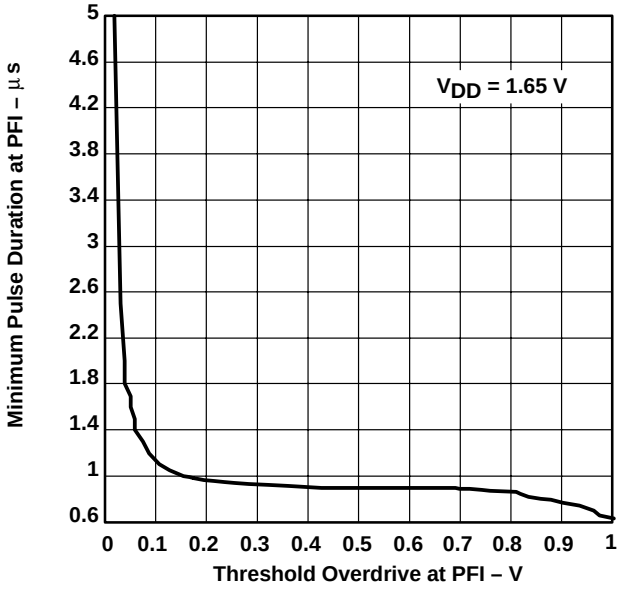
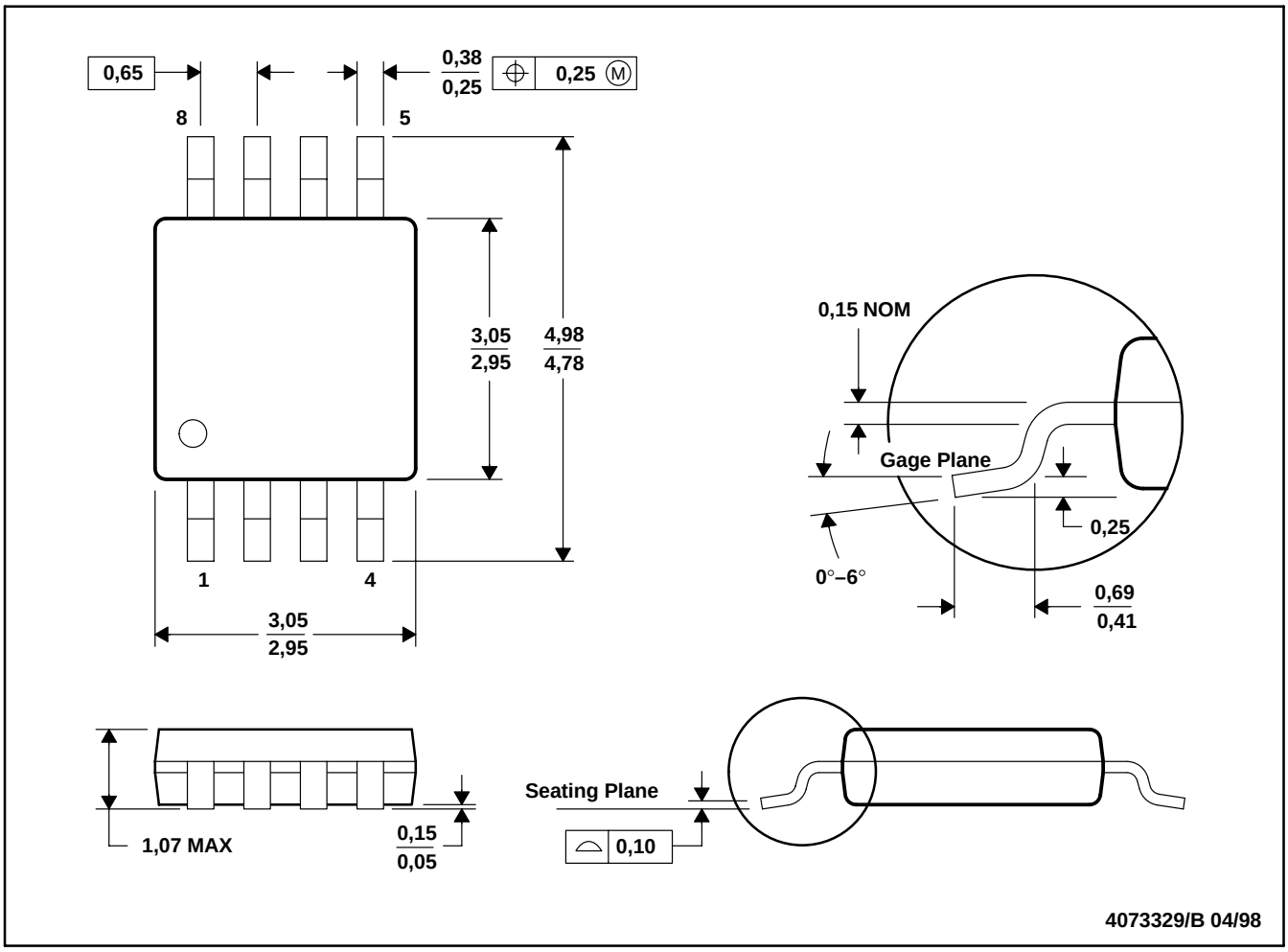


Figure 13

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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