features

- Minimum Supply Voltage of 0.75 V
- Supply Voltage Supervision Range:
  - 1.2 V, 1.5 V, 1.8 V (TPS312x)
  - 3 V (TPS3125 Devices Only)
  - Other Versions on Request
- Power-On Reset Generator With Fixed Delay Time of 180 ms
- Manual Reset Input (TPS3123/5/6/8)
- Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at $V_{DD} \geq V_{IT}$
- Supply Current of 14 μA (Typ)
- SOT23–5 Package
- Temperature Range . . . –40°C to 85°C
- Reset Output Available in Active-Low (TSP3123/4/5), Active-High (TSP3124/5), and Open-Drain Active-Low (TPS3126/8)

typical applications

- Applications Using Low Voltage DSPs, Microcontrollers, or Microprocessors
- Wireless Communication Systems
- Portable/Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook/Desktop Computers
- Automotive Systems

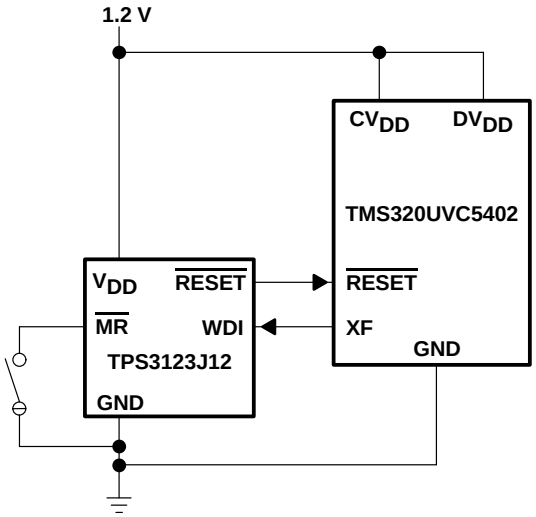
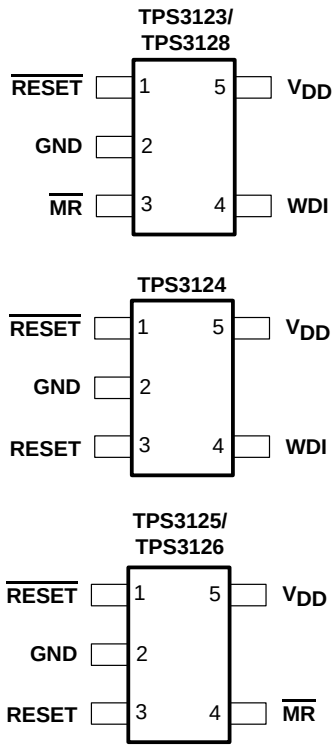


Figure 1. Typical Low-Voltage DSP Application

DBV PACKAGE
(TOP VIEW)



description

The TPS312x family of ultralow voltage processor supervisory circuits provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) becomes higher than 0.75 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_{dtyp} = 180 ms starts after V_{DD} has risen above the threshold voltage (V_{IT}).

description (continued)

When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

The TPS3123/5/6/8 devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active. The TPS3124 devices do not have the input $\overline{MR}$, but include a high-level output RESET same as the TPS3125 and TPS3126 devices. In addition, the TPS3123/4/8 have a watchdog timer that needs to be triggered periodically by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval t_{tout} = 0.8 s, $\overline{RESET}$ output becomes active for the time period (t_d). This event also reinitializes the watchdog timer.

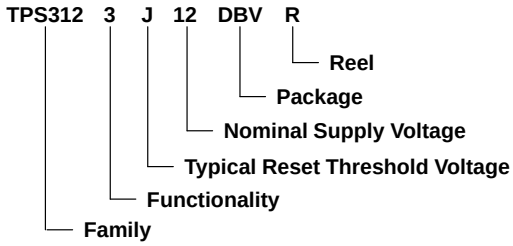
The circuits are available in a 5-pin SOT23-5 package. The TPS312x devices are characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION STANDARD VERSIONS

T_A	DEVICE NAME		THRESHOLD VOLTAGE	MARKING
–40°C to 85°C	TPS3123J12DBVR†	TPS3123J12DBVT‡	1.08 V	PBNI
	TPS3123G15DBVR†	TPS3123G15DBVT‡	1.40 V	PBOI
	TPS3123J18DBVR†	TPS3123J18DBVT‡	1.62 V	PBPI
	TPS3124J12DBVR†	TPS3124J12DBVT‡	1.08 V	PBQI
	TPS3124G15DBVR†	TPS3124G15DBVT‡	1.40 V	PBRI
	TPS3124J18DBVR†	TPS3124J18DBVT‡	1.62 V	PBSI
	TPS3125J12DBVR†	TPS3125J12DBVT‡	1.08 V	PBTI
	TPS3125G15DBVR†	TPS3125G15DBVT‡	1.40 V	PBUI
	TPS3125J18DBVR†	TPS3125J18DBVT‡	1.62 V	PBVI
	TPS3125L30DBVR†	TPS3125L30DBVT‡	2.64 V	PBXI
	TPS3126E12DBVR†	TPS3126E12DBVT‡	1.14 V	PFOI
	TPS3126E15DBVR†	TPS3126E15DBVT‡	1.43 V	PFPI
	TPS3126E18DBVR†	TPS3126E18DBVT‡	1.71 V	PFQI
	TPS3128E12DBVR†	TPS3128E12DBVT‡	1.14 V	PFRI
	TPS3128E15DBVR†	TPS3128E15DBVT‡	1.43 V	PFSI
	TPS3128E18DBVR†	TPS3128E18DBVT‡	1.71 V	PFTI

† The DBVR passive indicates tape and reel of 3000 parts.
‡ The DBVT passive indicates tape and reel of 250 parts.

ordering information application specific versions (see Note)



DEVICE NAME	NOMINAL SUPPLY VOLTAGE, V_{NOM}
TPS312xx12DBV	1.2 V
TPS312xx15DBV	1.5 V
TPS312xx18DBV	1.8 V
TPS312xx30DBV	3.0 V

DEVICE NAME	TYPICAL RESET THRESHOLD VOLTAGE–V_{IT-}
TPS312xAxxDBV	V_{NOM}–1%
TPS312xBxxDBV	V_{NOM}–2%
TPS312xCxxDBV	V_{NOM}–3%
TPS312xDxxDBV	V_{NOM}–4%
TPS312xExxDBV	V_{NOM}–5%
TPS312xFxxDBV	V_{NOM}–6%
TPS312xGxxDBV	V_{NOM}–7%
TPS312xHxxDBV	V_{NOM}–8%
TPS312xIxxDBV	V_{NOM}–9%
TPS312xJxxDBV	V_{NOM}–10%
TPS312xKxxDBV	V_{NOM}–11%
TPS312xLxxDBV	V_{NOM}–12%
TPS312xMxxDBV	V_{NOM}–13%
TPS312xNxxDBV	V_{NOM}–14%
TPS312xOxxDBV	V_{NOM}–15%

NOTE: For the application specific versions contact the local TI sales office for availability and lead time.

Function Tables

TPS3123/8

$\overline{MR}$	VDD > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

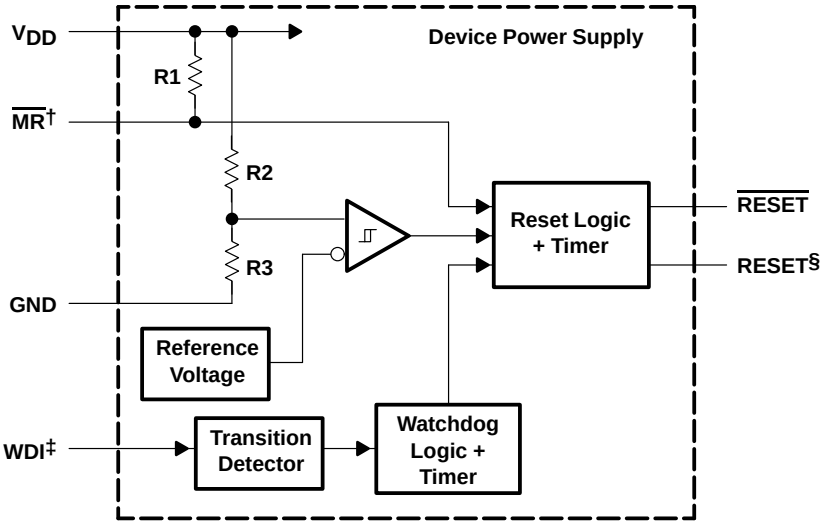
TPS3124

VDD > V_{IT}	$\overline{RESET}$	RESET
0	L	H
1	H	L

TPS3125/6

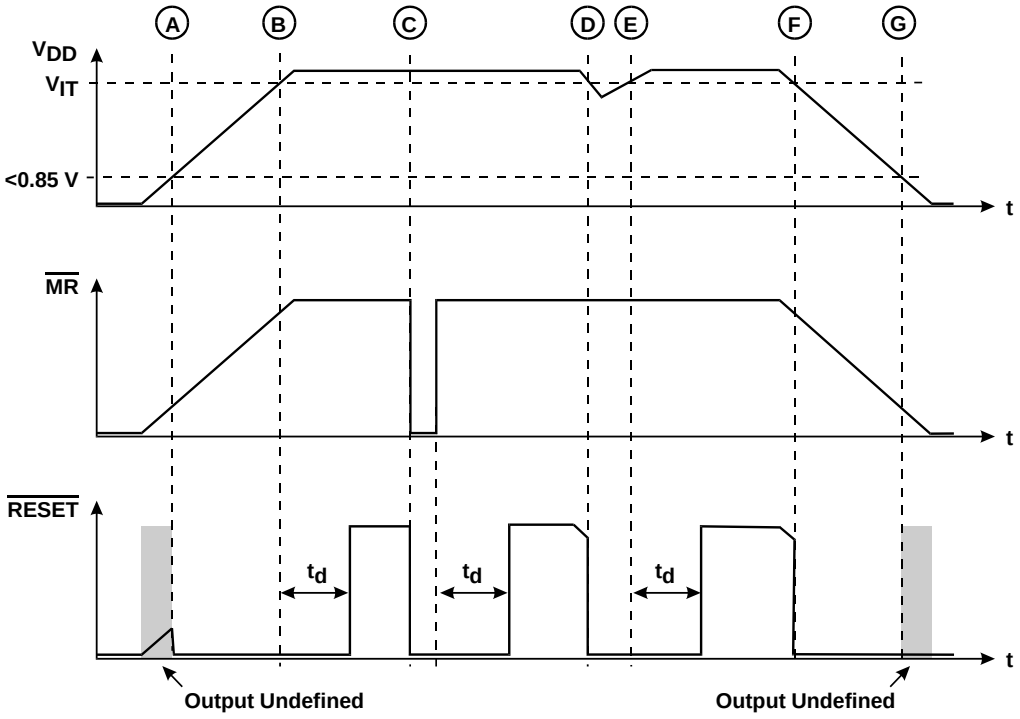
$\overline{MR}$	VDD > V_{IT}	$\overline{RESET}$	RESET
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

functional block diagram

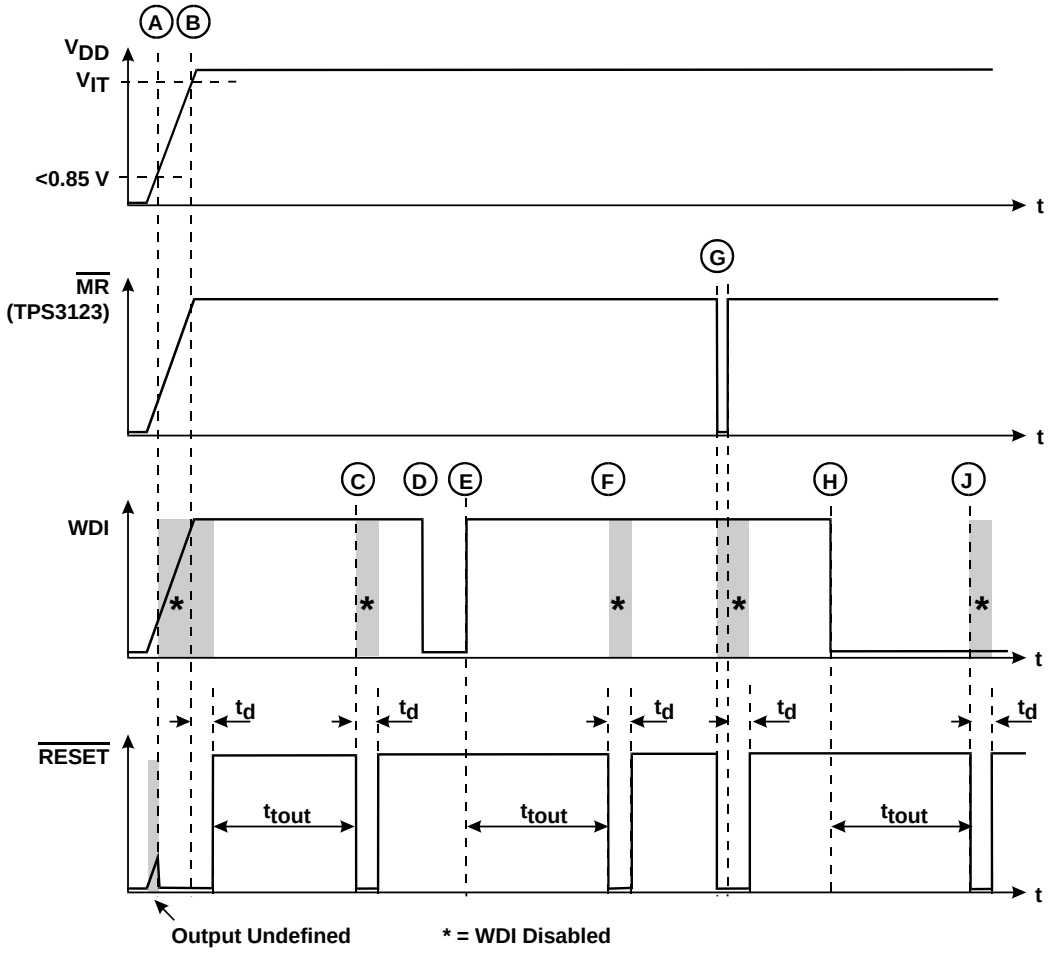


† TPS3123/5/6/8
‡ TPS3123/4/8
§ TPS3124/5/6

timing diagram TPS3123/5/6/8



timing diagram TPS3123/4/8



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.6 V
All other pins (see Note 1) . . . . . –0.3 V to 3.6 V
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . –5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}	T_A = 0°C to 85°C	0.75	3.3	V
	T_A = –40°C to 85°C	0.85	3.3	
Input voltage, V_I		0	V_{DD}+0.3	V
High-level input voltage, V_{IH}		0.7×V_{DD}		V
Low-level input voltage, V_{IL}			0.3×V_{DD}	V
Input transition rise and fall rate at WDI, $\Delta t/\Delta V$			1	µs/V
Operating free-air temperature range, T_A		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	$\overline{MR}$ pullup resistor (internal)					27		kΩ
I_{IH}	High-level input current	WDI	WDI = V_{DD} = 3.3 V		–1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD},	V_{DD} = 3.3 V	–20		–55	
I_{IL}	Low-level input current	WDI	WDI = 0 V,	V_{DD} = 3.3 V	–1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0 V,	V_{DD} = 3.3 V	–80		–170	
I_{OH}	High-level output current	TPS3126–xx, TPS3128–xx	V_{DD} = V_{OH} = 3.3 V				200	nA
V_{OH}	High-level output voltage (TPS3123/4/5 only)	RESET	V_{DD} = 1.5 V,	I_{OH} = –1 mA	0.8×V_{DD}			V
			V_{DD} = 3.3 V,	I_{OH} = –4.5 mA				
		RESET	V_{DD} = 0.75 V,	I_{OH} = –8 µA				
			V_{DD} = 1.5 V,	I_{OH} = –1 mA				
V_{OL}	Low-level output voltage	$\overline{RESET}$	V_{DD} = 0.75 V,	I_{OL} = 15 µA			0.2 × V_{DD}	V
			V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
		RESET	V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
			V_{DD} = 3.3 V,	I_{OL} = 3 mA			0.4	
$V_{IT–}$	Negative-going input threshold voltage (see Note 2)	TPS312xJ12	T_A = –40°C to 85°C		1.04	1.08	1.12	V
		TPS312xG15			1.35	1.40	1.45	
		TPS312xJ18			1.56	1.62	1.68	
		TPS312xL30			2.57	2.64	2.71	
		TPS312xE12			1.10	1.14	1.18	
		TPS312xE15			1.38	1.43	1.48	
		TPS312xE18			1.65	1.71	1.77	
V_{hys}	Hysteresis at V_{DD} input		1 V < $V_{IT–}$ < 1.4 V			15		mV
			1.4 V < $V_{IT–}$ <2 V			20		
			2 V < $V_{IT–}$ < 3 V			30		
I_{DD}	Supply current	TPS3123-xx TPS3124-xx TPS3128-xx	$\overline{WDI}$ = V_{DD}, $\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		µA
				V_{DD} = 3.3 V		22	30	
		TPS3125-xx TPS3126-xx (see Note 3)	$\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		
				V_{DD} = 3.3 V		18	25	
C_i	Input capacitance at $\overline{MR}$, WDI		V_I = 0 V to 3.3 V			5		pF

NOTES: 2. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
3. The supply current during delay time t_d is typical 5 µA higher.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	At V_{DD}	$V_{IH} = V_{IT-} + 0.2$ V, $V_{IL} = V_{IT-} - 0.2$ V	6			µs
		At $\overline{MR}$	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
		At WDI		0.1			

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{tout}	Watchdog time out		$V_{DD} \geq V_{IT-} + 0.2$ V, See timing diagram	0.8	1.4	2.1	s
t_d	Delay time		$V_{DD} > V_{IT-} + 0.2$ V, See timing diagram	100	180	260	ms
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3123/5/6/8)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.8 \times V_{DD}$			0.1	µs
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3125/6)				0.1	
t_{PHL}	Propagation delay time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			10	µs
t_{PLH}	Propagation delay time, low-to-high-level output	V_{DD} to RESET delay (TPS3124/5/6)				10	

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

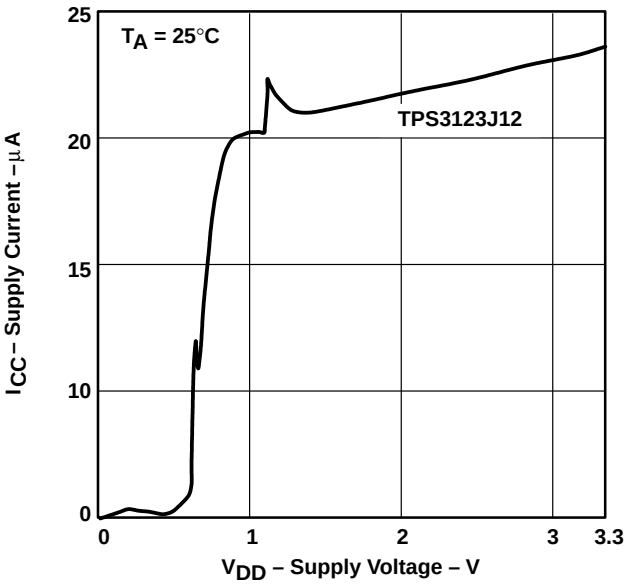


Figure 2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

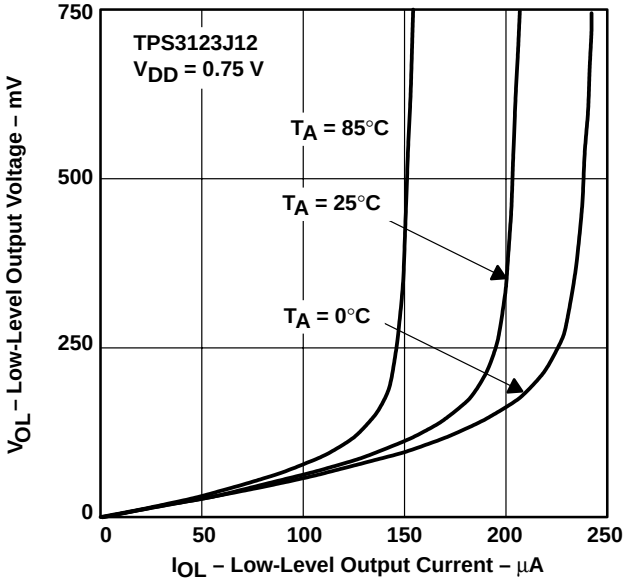


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

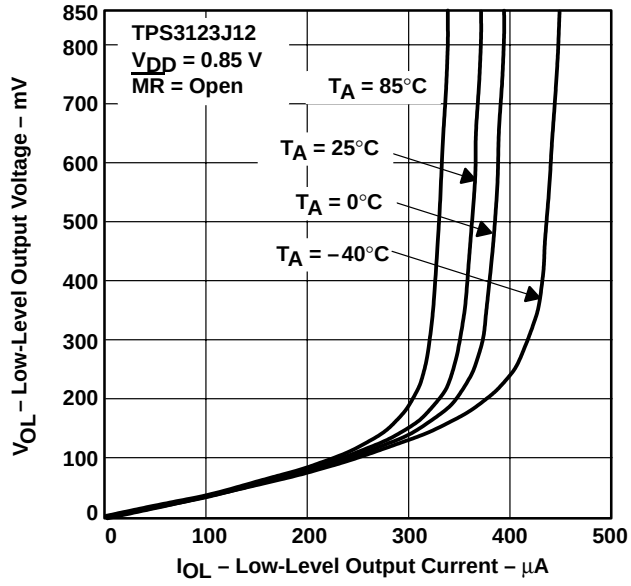


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

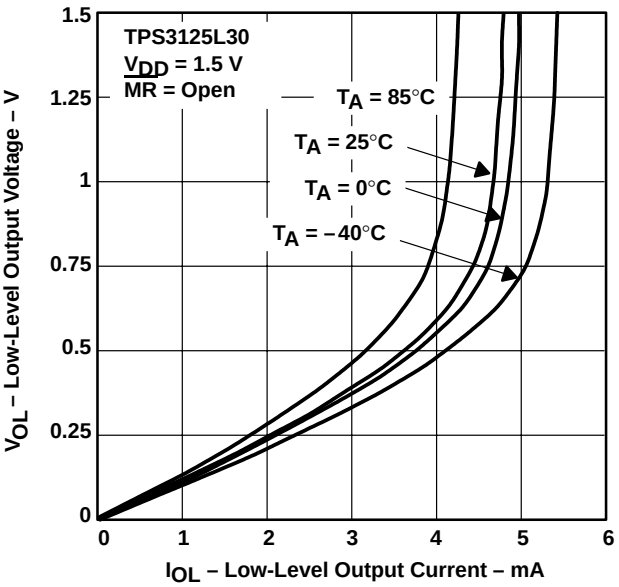


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

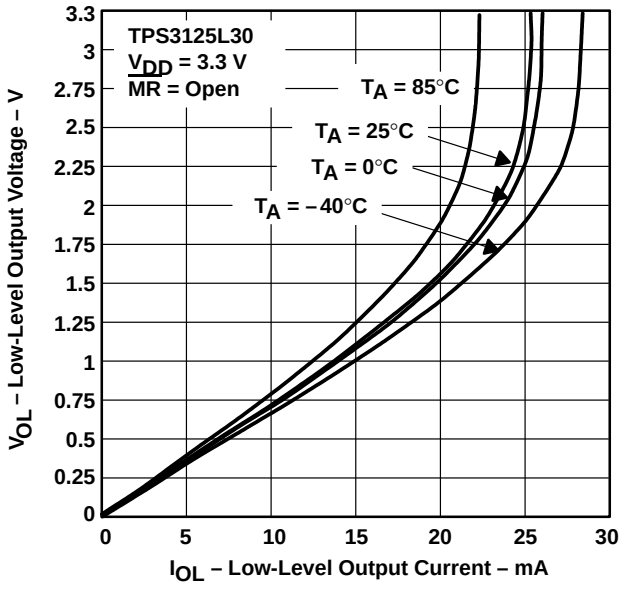


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

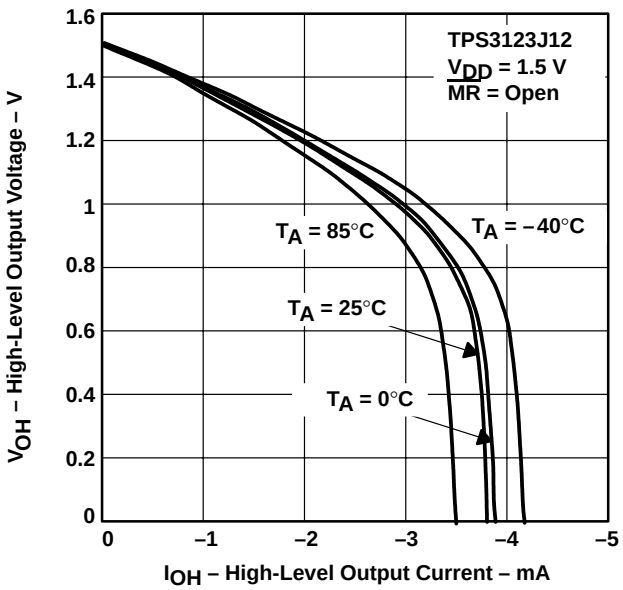


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

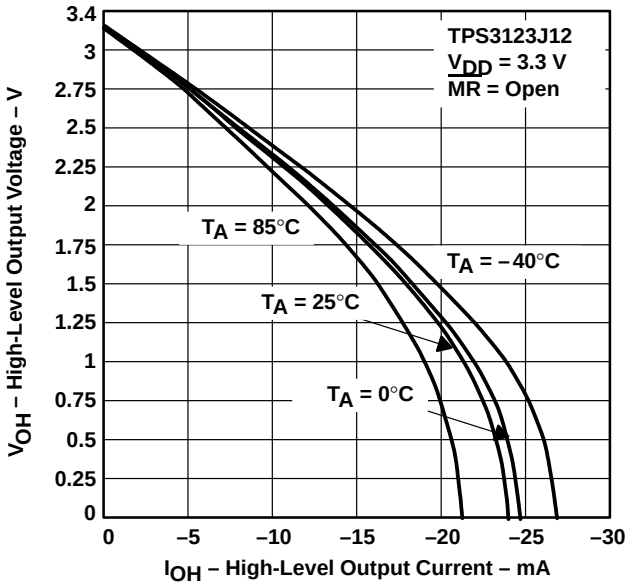


Figure 8

NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

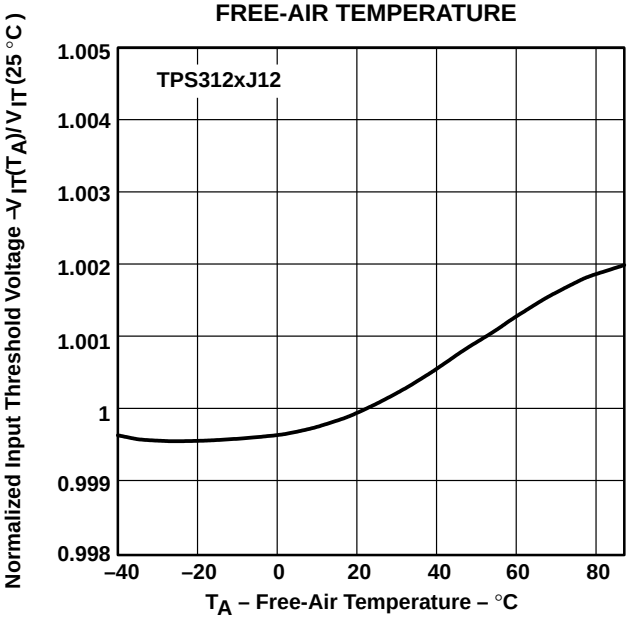


Figure 9

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

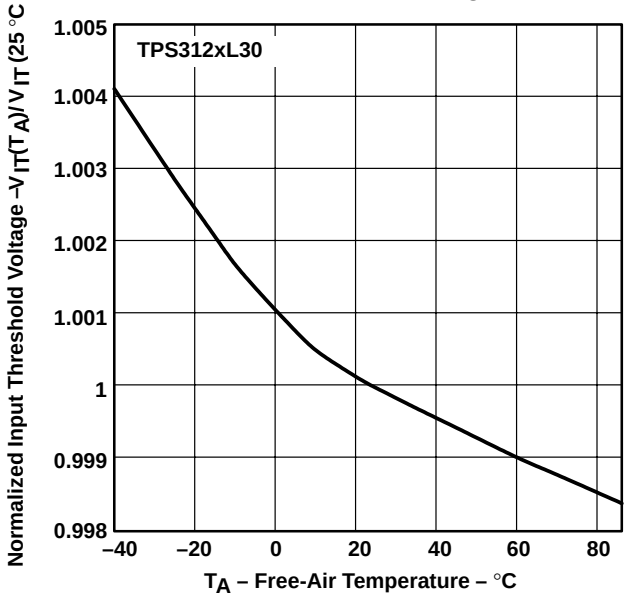


Figure 10

MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

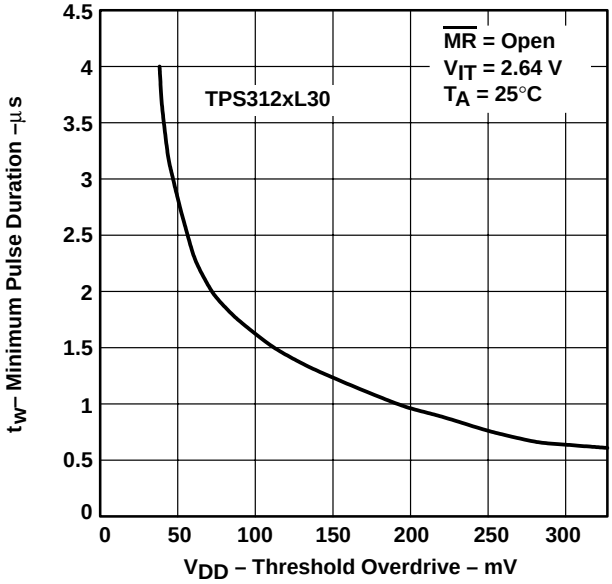


Figure 11

MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

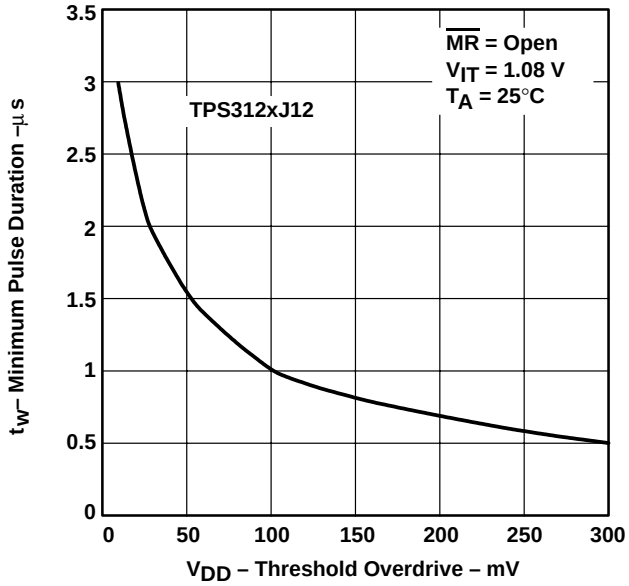
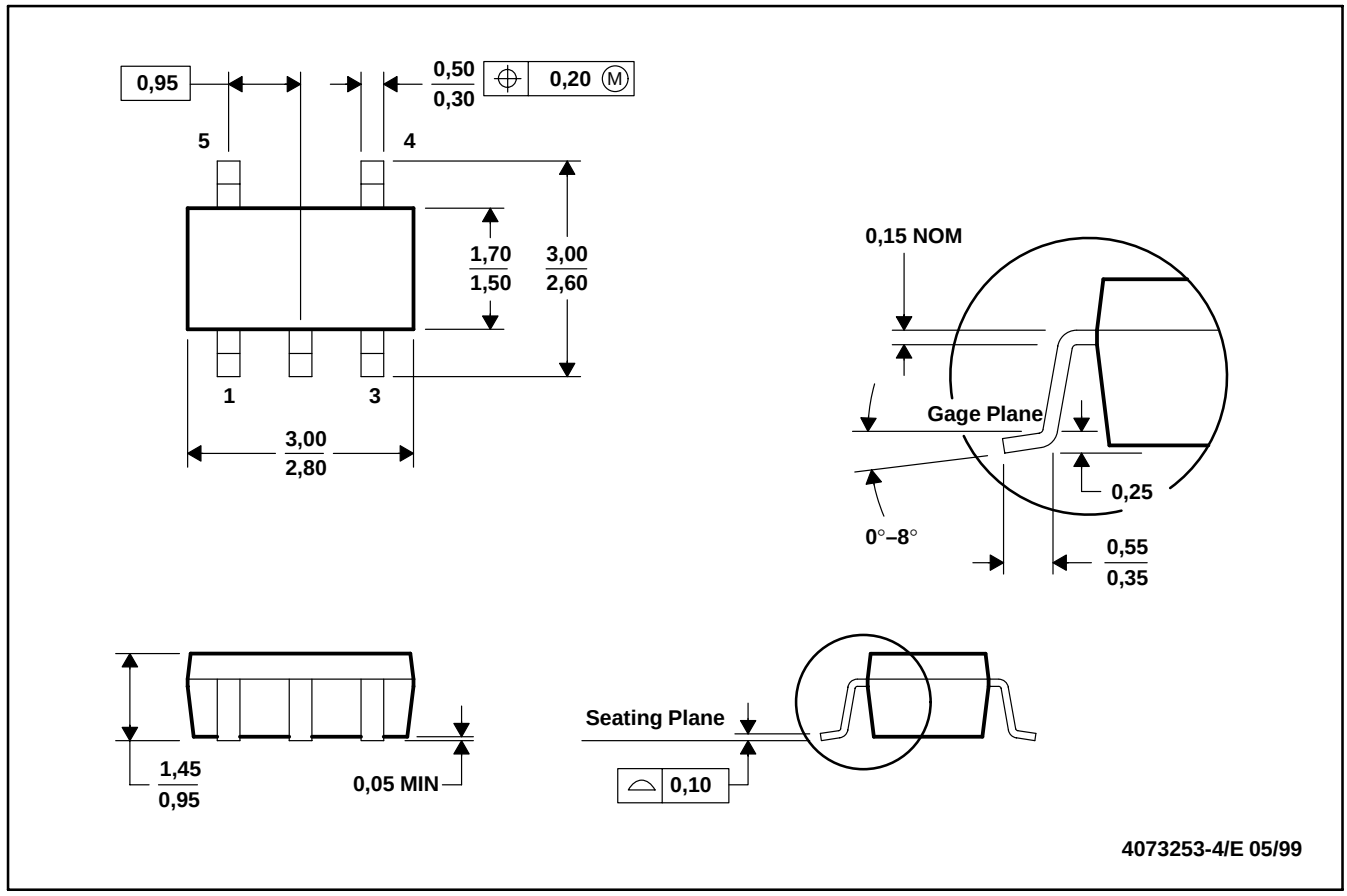


Figure 12

MECHANICAL DATA

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

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