

TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SLVS087L – DECEMBER 1994 – REVISED FEBRUARY 2003

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Programmable Delay Time by External Capacitor
- Supply Voltage Range . . . 2 V to 6 V
- Defined $\overline{\text{RESET}}$ Output from $V_{\text{DD}} \geq 1 \text{ V}$
- Power-Down Control Support for Static RAM With Battery Backup
- Maximum Supply Current of 16 μA
- Power Saving Totem-Pole Outputs
- Temperature Range . . . Up to -55°C to 125°C

description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum $V_{\text{DD}} (\geq 2 \text{ V})$ is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{\text{I}(\text{SENSE})}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_{d} , is determined by an external capacitor:

$$t_{\text{d}} = 2.1 \times 10^4 \times C_{\text{T}}$$

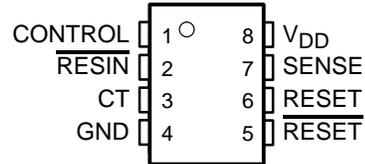
Where

C_{T} is in farads

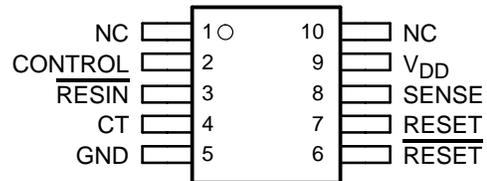
t_{d} is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_{d} , has expired.

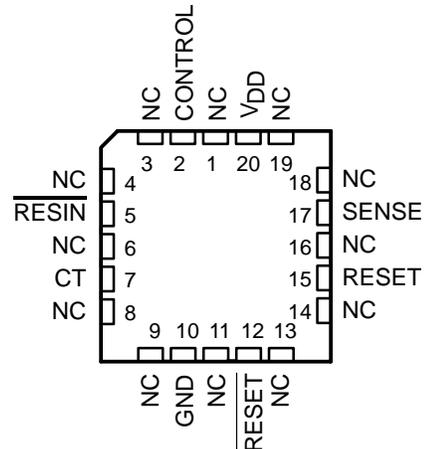
D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description (continued)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select (\overline{CS}) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($CSH1$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxI is characterized for operation over a temperature range of -40°C to 85°C ; the TLC77xxQ is characterized for operation over a temperature range of -40°C to 125°C ; and the TLC77xxM is characterized for operation over the full Military temperature range of -55°C to 125°C .

AVAILABLE OPTIONS

T _A	THRESHOLD VOLTAGE (V)	PACKAGED DEVICES					
		SMALL OUTLINE (D) [†]	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC DUAL FLATPACK (U)	PLASTIC DIP (P)	THIN SHRINK SMALL OUTLINE (PW) [‡]
-40°C to 85°C	1.1	TLC7701ID	—	—	—	TLC7701IP	TLC7701IPW
	2.25	TLC7725ID	—	—	—	TLC7725IP	TLC7725IPW
	2.63	TLC7703ID	—	—	—	TLC7703IP	TLC7703IPW
	2.93	TLC7733ID	—	—	—	TLC7733IP	TLC7733IPW
	4.55	TLC7705ID	—	—	—	TLC7705IP	TLC7705IPW
-40°C to 125°C	1.1	TLC7701QD	—	—	—	TLC7701QP	TLC7701QPW
	2.25	TLC7725QD	—	—	—	TLC7725QP	TLC7725QPW
	2.63	TLC7703QD	—	—	—	TLC7703QP	TLC7703QPW
	2.93	TLC7733QD	—	—	—	TLC7733QP	TLC7733QPW
	4.55	TLC7705QD	—	—	—	TLC7705QP	TLC7705QPW
-55°C to 125°C	2.93	—	TLC7733MFK	TLC7733MJG	—	—	—
	4.55	—	TLC7705MFK	TLC7705MJG	TLC7705MU	—	—

[†] The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).

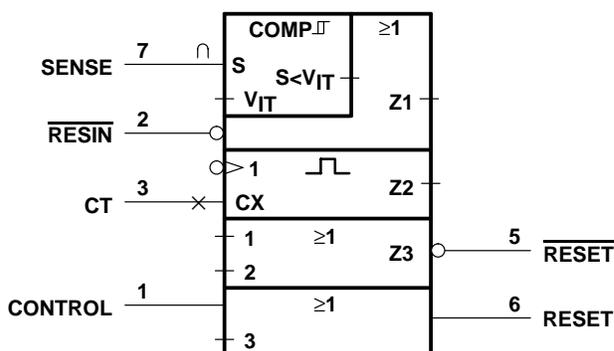
[‡] The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TLC7705QPWLE).

FUNCTION TABLE

CONTROL	\overline{RESIN}	$V_I(\text{SENSE}) > V_{IT+}$	RESET	\overline{RESET}
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L [§]	H [§]
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H [§]

[§] RESET and \overline{RESET} states shown are valid for $t > t_d$.

logic symbol[¶]

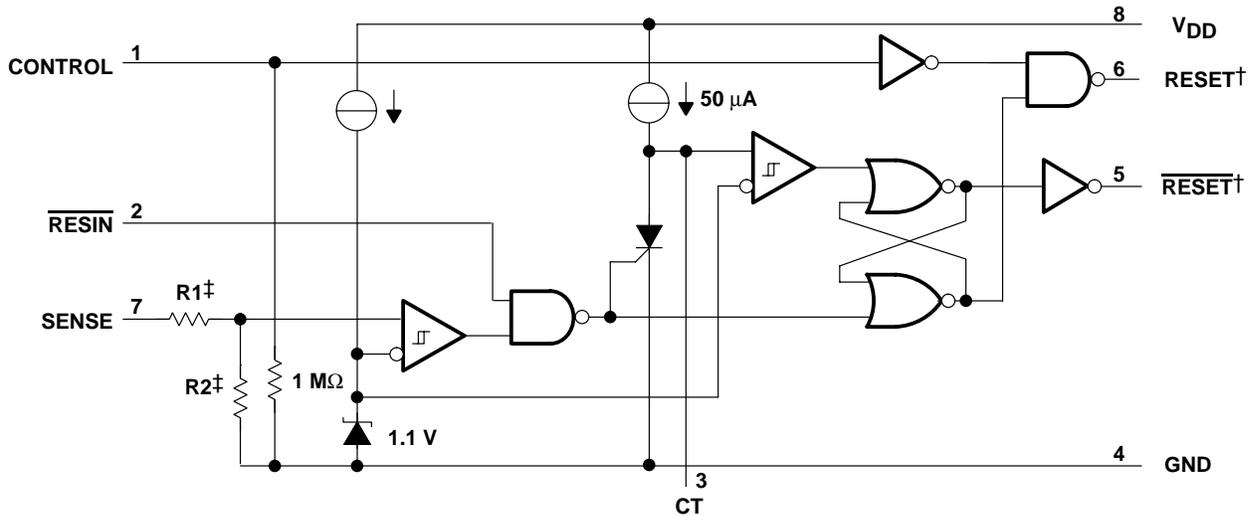


[¶] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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functional block diagram

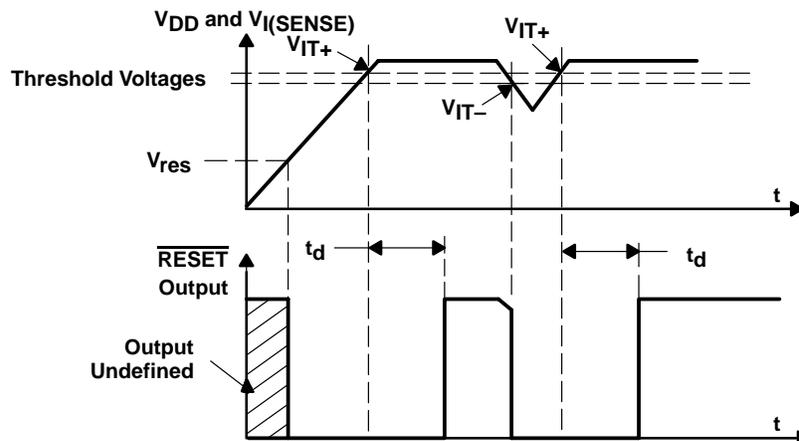


† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.

‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7725	600 k Ω	600 k Ω
TLC7703	698 k Ω	502 k Ω
TLC7733	750 k Ω	450 k Ω
TLC7705	910 k Ω	290 k Ω

timing diagram



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electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC77xx			UNIT	
			MIN	TYP†	MAX		
V _{OH}	High-level output voltage	I _{OH} = -20 μA	V _{DD} = 2 V	1.8		V	
			V _{DD} = 2.7 V	2.5			
			V _{DD} = 4.5 V	4.3			
		I _{OH} = -2 mA	V _{DD} = 4.5 V	3.7			
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	V _{DD} = 2 V	0.2		V	
			V _{DD} = 2.7 V	0.2			
			V _{DD} = 4.5 V	0.2			
		I _{OL} = 2 mA	V _{DD} = 4.5 V	0.5			
V _{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)	TLC7701	V _{DD} = 2 V to 6 V	1.04	1.1	1.16	V
		TLC7725		2.18	2.25	2.32	
		TLC7703		2.56	2.63	2.70	
		TLC7733		2.86	2.93	3	
		TLC7705		4.47	4.55	4.63	
V _{hys}	Hysteresis voltage, SENSE	TLC7701	V _{DD} = 2 V to 6 V	30		mV	
		TLC7725	V _{DD} = 2 V to 6 V	70		mV	
		TLC7703,					
		TLC7733,					
		TLC7705					
V _{res}	Power-up reset voltage‡	I _{OL} = 20 μA	1		V		
I _I	Input current	RESIN	V _I = 0 V to V _{DD}	2		μA	
		CONTROL	V _I = V _{DD}	7	15		
		SENSE	V _I = 5 V	5	10		
		SENSE, TLC7701 only	V _I = 5 V	2			
I _{DD}	Supply current	RESIN = V _{DD} , SENSE = V _{DD} ≥ V _{ITmax} + 0.2 V CONTROL = 0 V, Outputs open	9		16	μA	
I _{DD(d)}	Supply current during t _d	V _{DD} = 5 V, V _{CT} = 0, RESIN = V _{DD} , SENSE = V _{DD} , CONTROL = 0 V, Outputs open	120	150		μA	
C _I	Input capacitance, SENSE	V _I = 0 V to V _{DD}	50		pF		

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be connected near the supply terminals.



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electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC77xxM			UNIT	
				MIN	TYP†	MAX		
V _{OH}	High-level output voltage	I _{OH} = -20 μA	V _{DD} = 2 V	T _A = 25°C	1.8		V	
				T _A = -55°C to 125°C	1.7			
			V _{DD} = 2.7 V	T _A = 25°C	2.5			
				T _A = -55°C to 125°C	2.3			
			V _{DD} = 4.5 V	T _A = 25°C	4.3			
				T _A = -55°C to 125°C	4.2			
I _{OH} = -2 mA	V _{DD} = 4.5 V	T _A = 25°C	3.7					
		T _A = -55°C to 125°C	3.6					
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	V _{DD} = 2 V	T _A = 25°C		0.2	V	
				T _A = -55°C to 125°C		0.2		
			V _{DD} = 2.7 V	T _A = 25°C		0.2		
				T _A = -55°C to 125°C		0.2		
			V _{DD} = 4.5 V	T _A = 25°C		0.2		
				T _A = -55°C to 125°C		0.2		
			I _{OL} = 2 mA	V _{DD} = 4.5 V	T _A = 25°C			0.5
					T _A = -55°C to 125°C			0.5
V _{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)	TLC7733	V _{DD} = 2 V to 6 V	2.86	2.93	3.1	V	
		TLC7705		4.3	4.5	4.8		
V _{hys}	Hysteresis voltage, SENSE	V _{DD} = 2 V to 6 V	V _{DD} = 2 V to 6 V		70		mV	
V _{res}	Power-up reset voltage‡	I _{OL} = 20 μA				1	V	
I _I	Input current	RESIN	V _I = 0 V to V _{DD}			2	μA	
		CONTROL	V _I = V _{DD}		7	15		
		SENSE	V _I = 5 V		5	10		
		SENSE, TLC7701 only	V _I = 5 V			2		
I _{DD}	Supply current	RESIN = V _{DD} , SENSE = V _{DD} ≥ V _{ITmax} + 0.2 V CONTROL = 0 V, Outputs open			9	16	μA	
I _{DD(d)}	Supply current during t _d	TLC7733	V _{CT} = 0, RESIN = V _{DD} , CONTROL = 0 V, SENSE = V _{DD} , Outputs open	V _{DD} = 3.3 V		250	μA	
		TLC7705		V _{DD} = 5 V		120 150		
C _I	Input capacitance, SENSE	V _I = 0 V to V _{DD}				50	pF	

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.



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switching characteristics at $V_{DD} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	MEASURED		TEST CONDITIONS	TLC77xx			UNIT
	FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d Delay time	$V_I(\text{SENSE}) \geq V_{IT+}$	$\overline{\text{RESET}}$ and $\overline{\text{RESET}}$	$\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = 100\text{ nF}$, $T_A = \text{Full range}$, See timing diagram	1.1	2.1	4.2	ms
t_{PLH} Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = \text{NC}^\dagger$	20			μs
t_{PHL} Propagation delay time, high-to-low-level output				5			
t_{PLH} Propagation delay time, low-to-high-level output		$\overline{\text{RESET}}$		5			
t_{PHL} Propagation delay time, high-to-low-level output				20			
t_{PLH} Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, $\text{SENSE} = V_{IT+max} + 0.2\text{ V}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = \text{NC}^\dagger$	20			μs
t_{PHL} Propagation delay time, high-to-low-level output				40			
t_{PLH} Propagation delay time, low-to-high-level output		$\overline{\text{RESET}}$		45			ns
t_{PHL} Propagation delay time, high-to-low-level output				20			
t_{PLH} Propagation delay time, low-to-high-level output	CONTROL	RESET	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, $\text{SENSE} = V_{IT+max} + 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $C_T = \text{NC}^\dagger$	38			ns
t_{PHL} Propagation delay time, high-to-low-level output					38		
Low-level minimum pulse duration to switch $\overline{\text{RESET}}$ and $\overline{\text{RESET}}$	SENSE		$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, $V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	3			μs
	$\overline{\text{RESIN}}$			1			
t_r Rise time		$\overline{\text{RESET}}$ and $\overline{\text{RESET}}$	10% to 90%	8			ns/V
t_f Fall time			90% to 10%	4			

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

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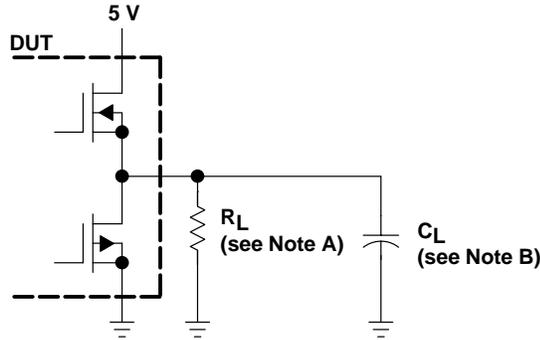
switching characteristics at $V_{DD} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$

PARAMETER	MEASURED		TEST CONDITIONS	T_A	TLC77xxM			UNIT
	FROM (INPUT)	TO (OUTPUT)			MIN	TYP	MAX	
t_d Delay time	$V_{I(\text{SENSE})} \geq V_{IT+}$	RESET and RESET	RESIN = 2.7 V, CONTROL = 0.4 V, $C_T = 100\text{ nF}$, See timing diagram	Full range	1.1	2.1	4.2	ms
t_{PLH} Propagation delay time, low-to-high-level output	SENSE	RESET	$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, RESIN = 2.7 V, CONTROL = 0.4 V, $C_T = \text{NC}^\dagger$	25°C			20	μs
		Full range				24		
		RESET		25°C			5	μs
		Full range				7		
t_{PHL} Propagation delay time, high-to-low-level output	SENSE	RESET	$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, RESIN = 2.7 V, CONTROL = 0.4 V, $C_T = \text{NC}^\dagger$	25°C			5	μs
		Full range				7		
		RESET		25°C			20	μs
		Full range				24		
t_{PLH} Propagation delay time, low-to-high-level output	RESIN	RESET	$V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, CONTROL = 0.4 V, $C_T = \text{NC}^\dagger$	25°C			20	μs
		Full range				24		
		RESET		25°C			45	ns
		Full range				65		
t_{PHL} Propagation delay time, high-to-low-level output	RESIN	RESET	$V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, CONTROL = 0.4 V, $C_T = \text{NC}^\dagger$	25°C			40	ns
		Full range				60		
		RESET		25°C			20	μs
		Full range				24		
t_{PLH} Propagation delay time, low-to-high-level output	CONTROL	RESET	$V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, RESIN = 2.7 V, $C_T = \text{NC}^\dagger$	25°C			38	ns
Full range						58		
t_{PHL} Propagation delay time, high-to-low-level output				25°C			38	ns
Full range						58		
Low-level minimum pulse duration	SENSE		$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, $V_{IL} = 0.4\text{ V}$, $V_{IH} = 2.7\text{ V}$	Full range	3			μs
	RESIN				1			
t_r Rise time		RESET and RESET	10% to 90%	Full range	8			ns/V
t_f Fall time			90% to 10%		4			

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, $R_L = 2\text{ k}\Omega$.
B. $C_L = 50\text{ pF}$ includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations

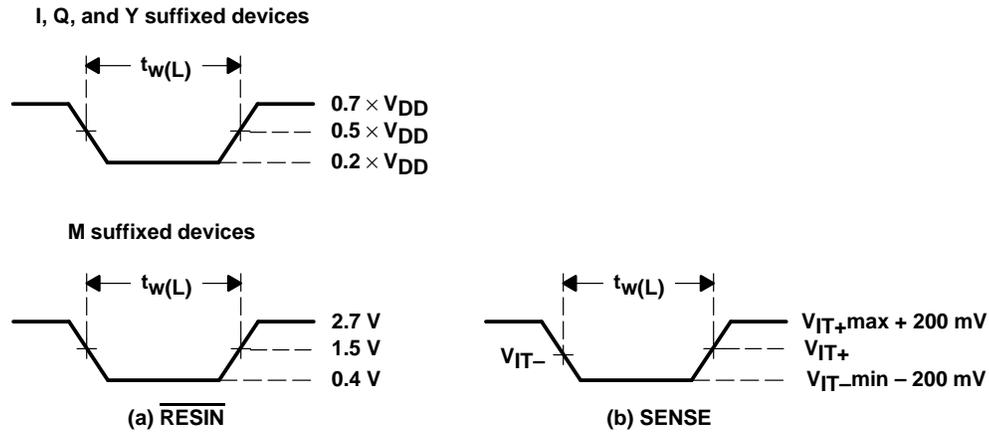


Figure 2. Input Pulse Definition Waveforms

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TYPICAL CHARACTERISTICS

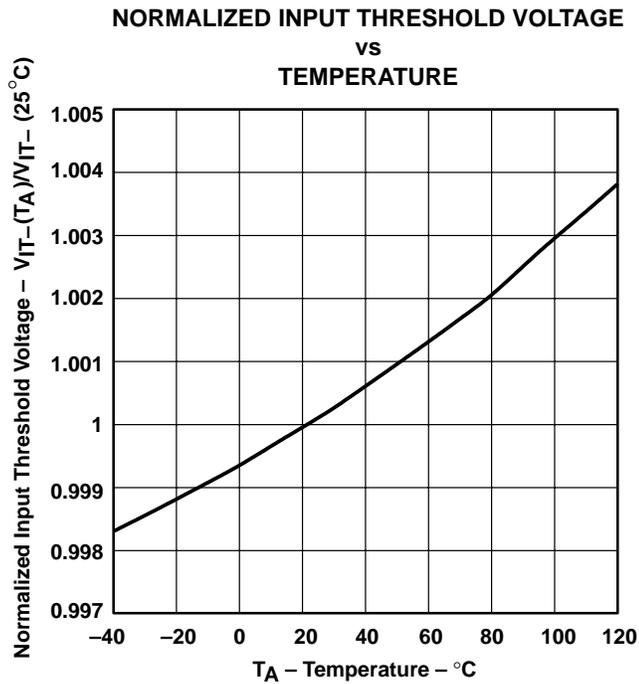


Figure 3

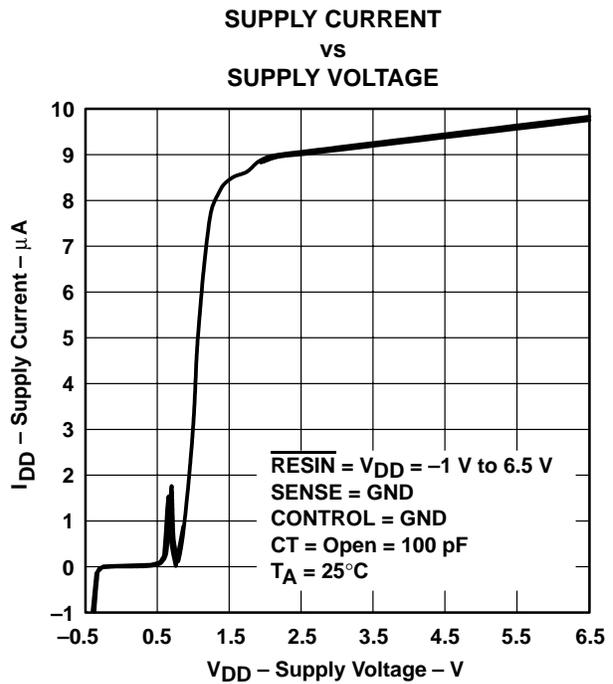


Figure 4

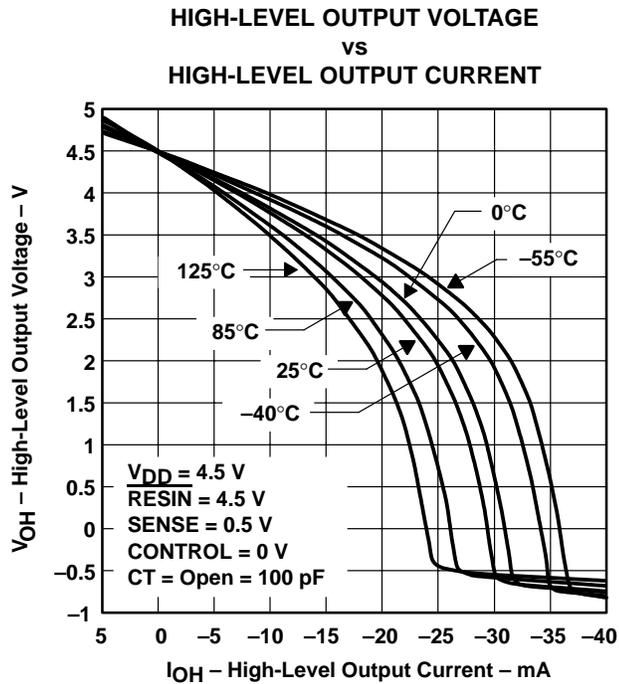


Figure 5

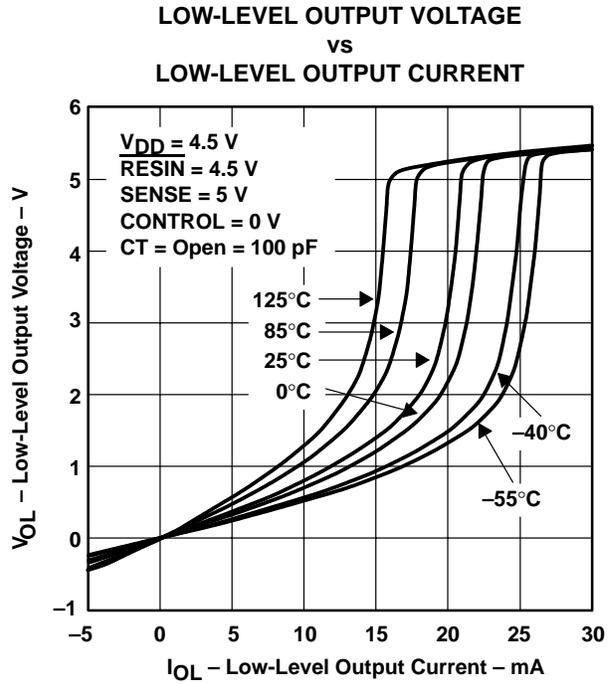
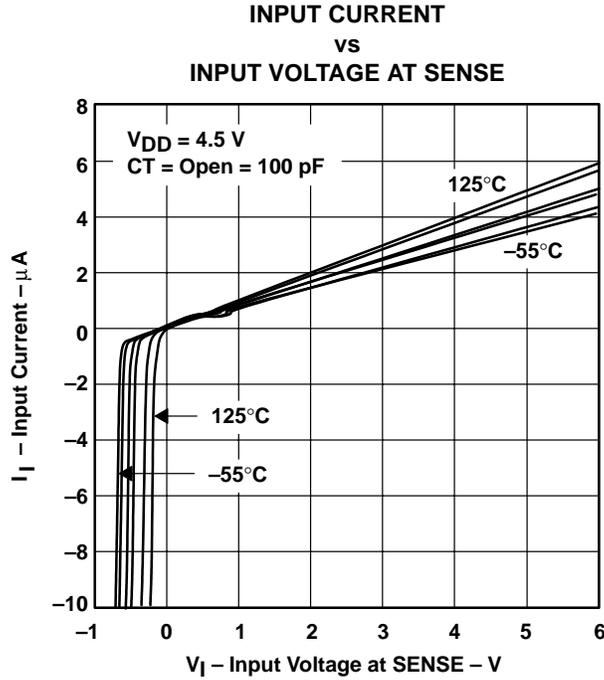


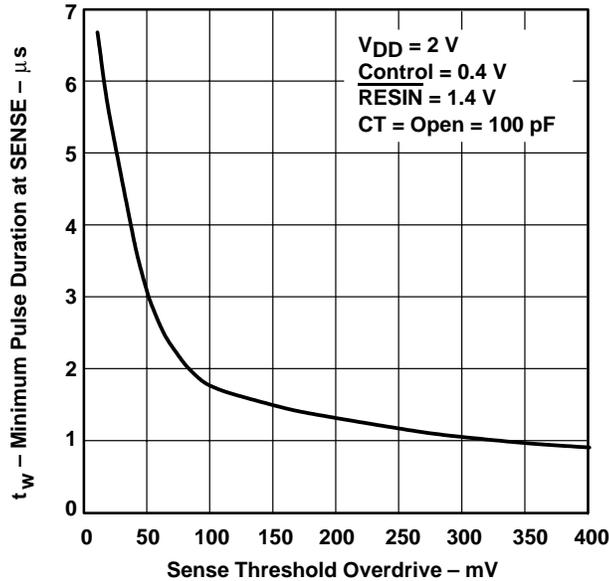
Figure 6



TYPICAL CHARACTERISTICS



**MINIMUM PULSE DURATION AT SENSE
vs
SENSE THRESHOLD OVERDRIVE**



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APPLICATION INFORMATION

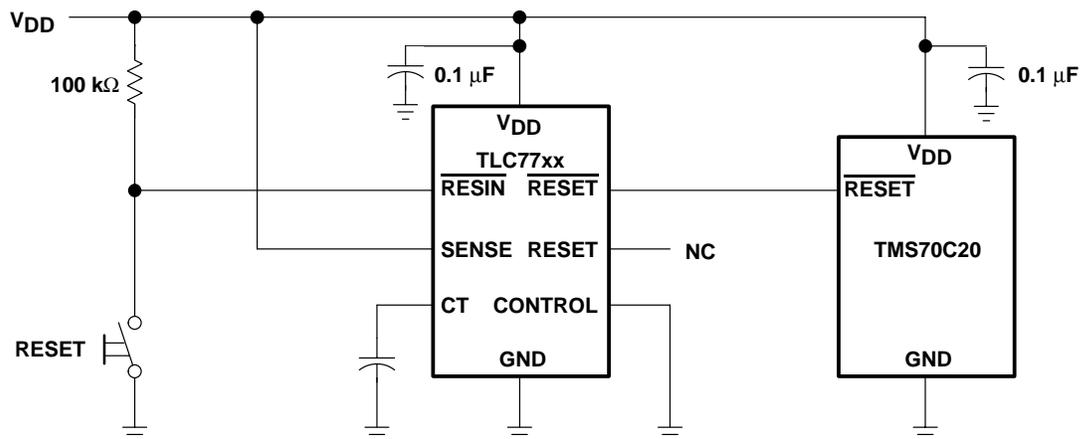


Figure 9. Reset Controller in a Microcomputer System

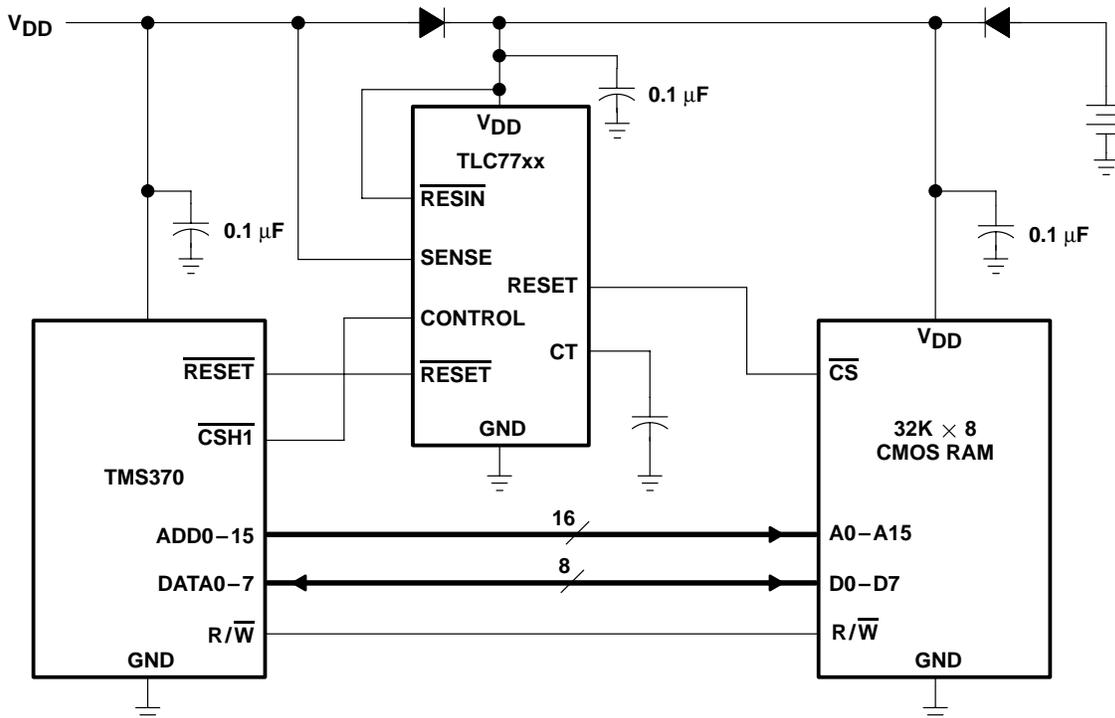


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

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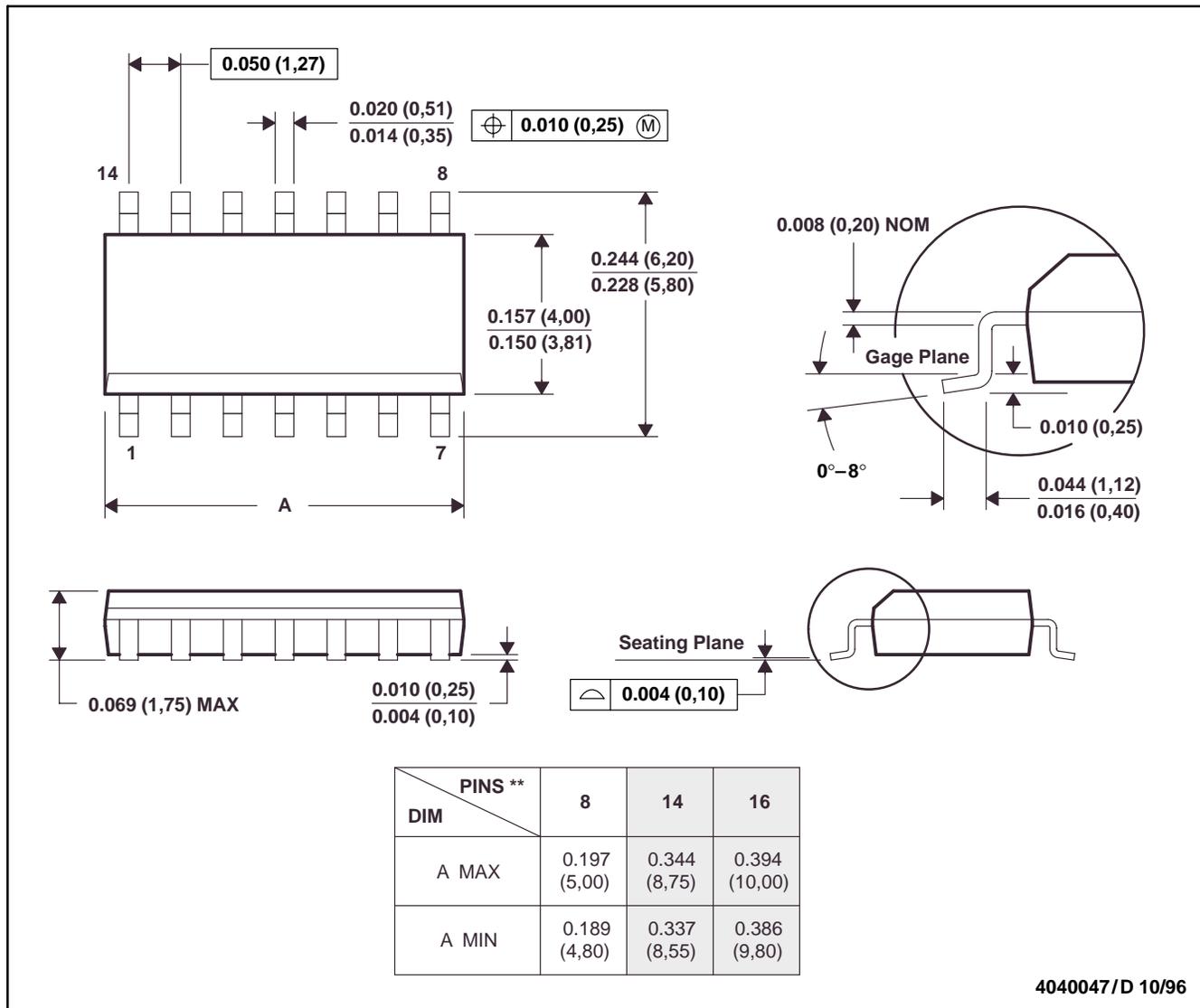
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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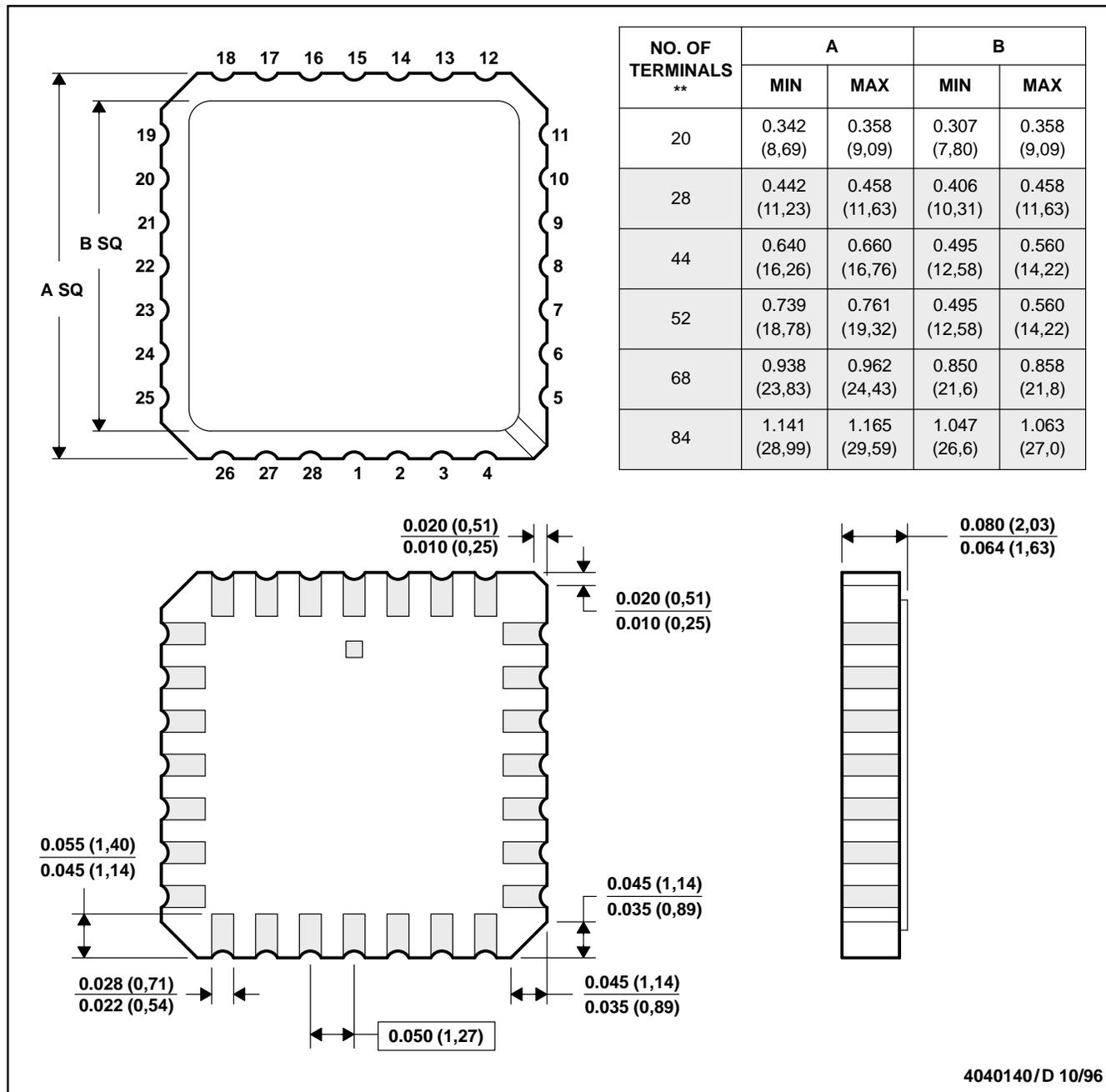
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MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004



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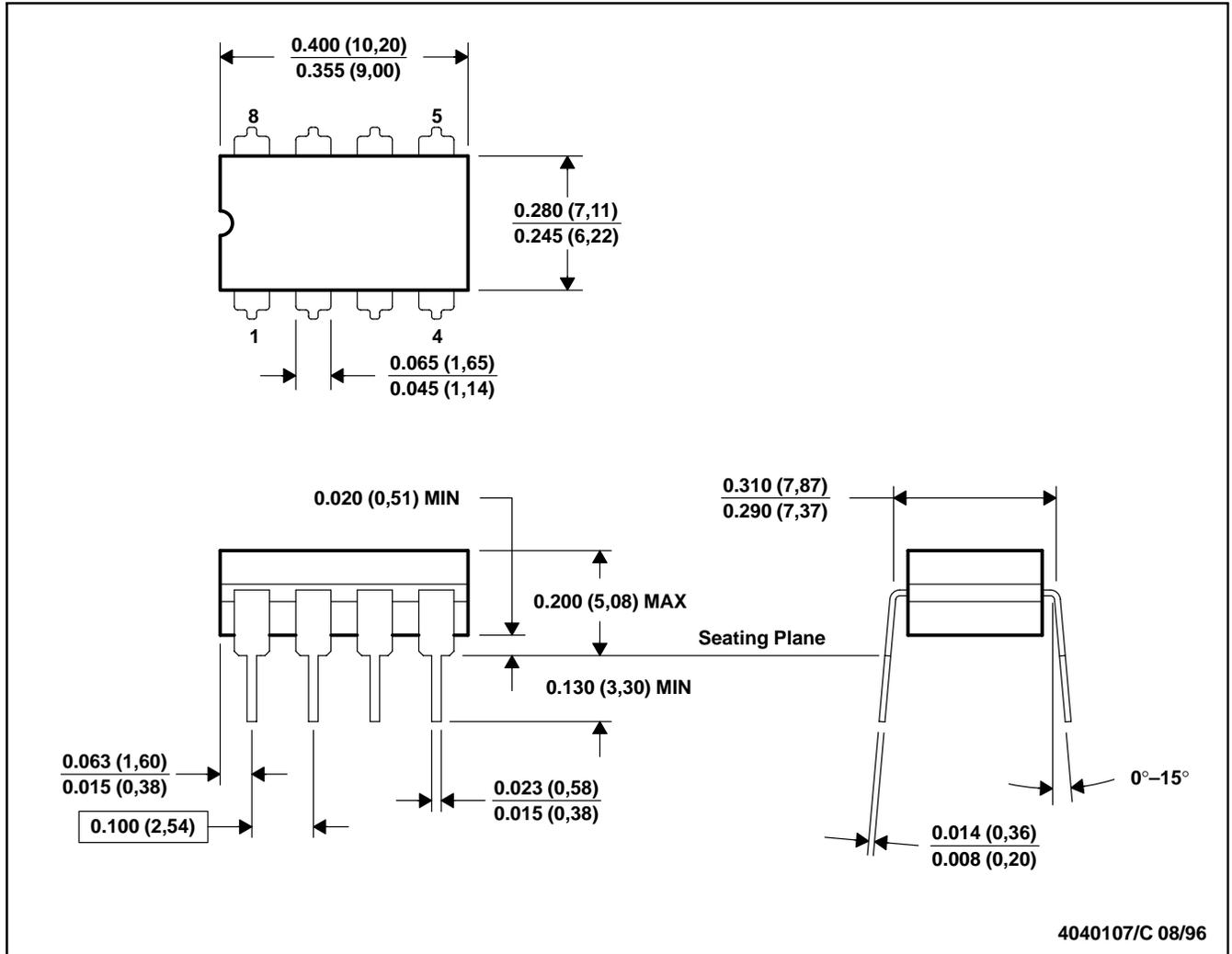
TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SLVS087L – DECEMBER 1994 – REVISED FEBRUARY 2003

MECHANICAL DATA

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T8

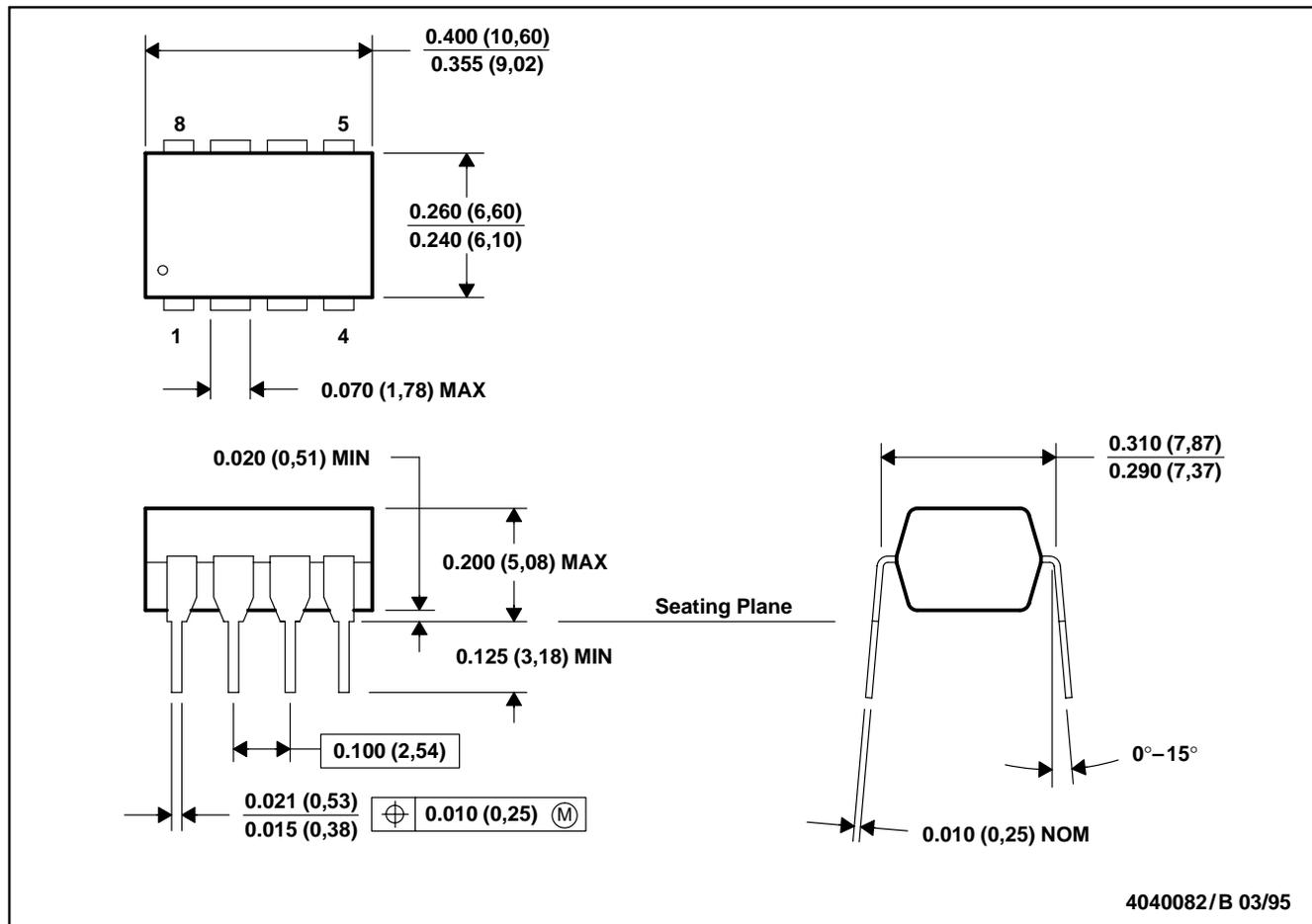
TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SLVS087L – DECEMBER 1994 – REVISED FEBRUARY 2003

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 MICROPOWER SUPPLY VOLTAGE SUPERVISORS

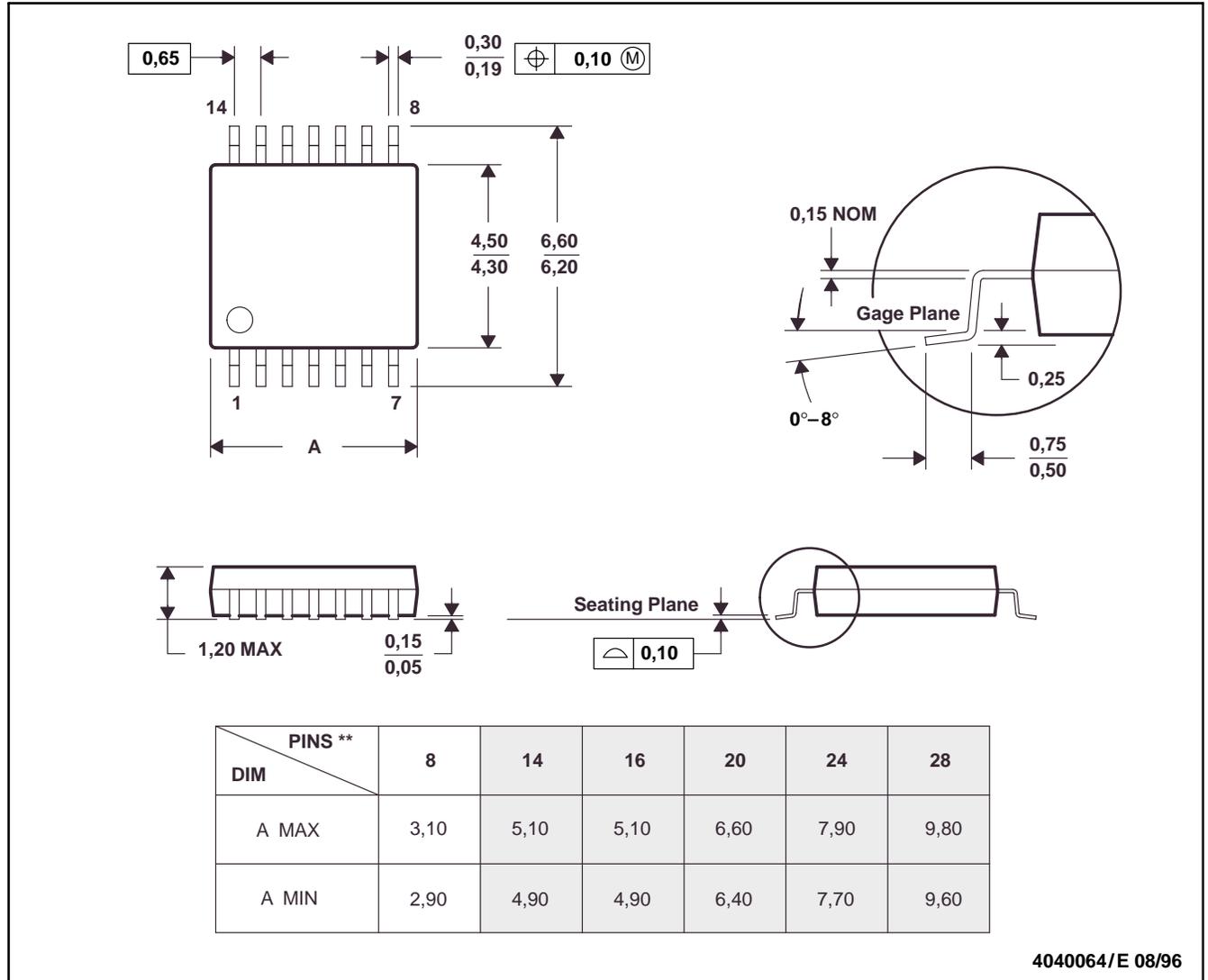
SLVS087L – DECEMBER 1994 – REVISED FEBRUARY 2003

MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

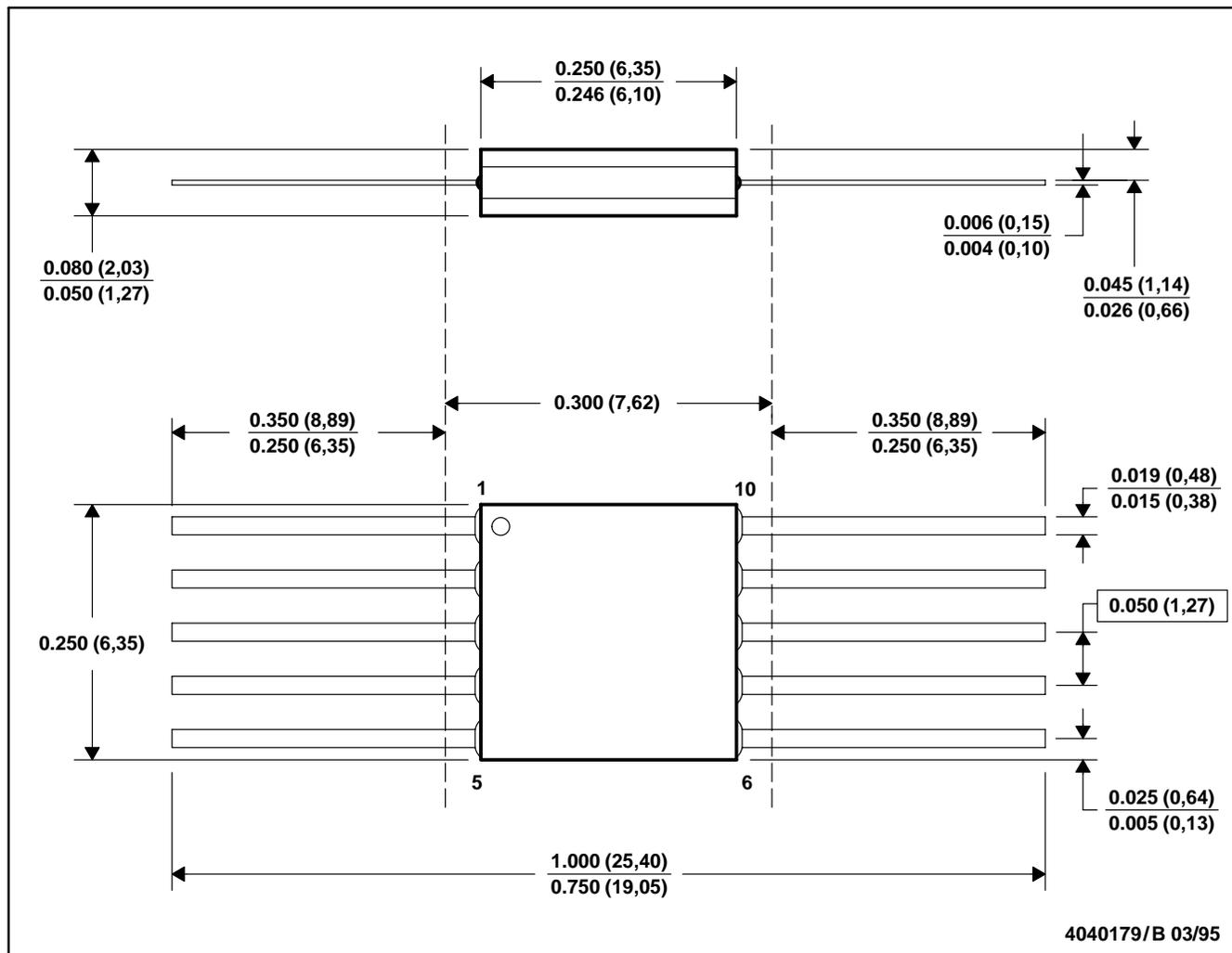
TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SLVS087L – DECEMBER 1994 – REVISED FEBRUARY 2003

MECHANICAL DATA

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

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