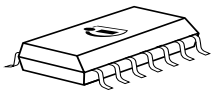
Step-Down DC/DC Controller for external N-MOSFETs TLE 6387 G

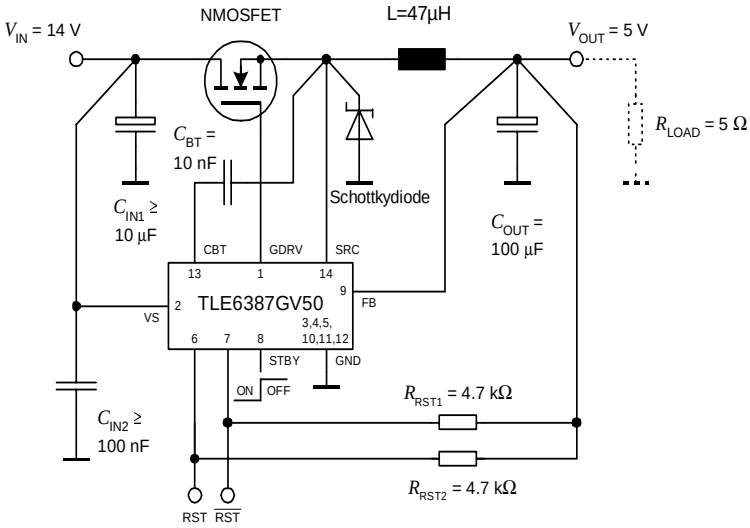
Target Datasheet

Features

- Input voltage range up to 60V
- Fixed output voltages: 5V at version GV50
  and 5.8V at version GV60
- Integrated output voltage supervision with
  over- and undervoltage reset (only at version GV50)
- Fixed reset delay time of 21ms (only at version GV50)
- Short-circuit protection
- Current mode control scheme without
  current sense resistor
- Stable operation even for ESR = 0
- Switching frequency of 400kHz
- Smart feedback wirebreak protection
- Overtemperature protection
- Wide ambient temperature range
  from -40°C to 125°C



P-DSO-14-3, -4, -9, -11



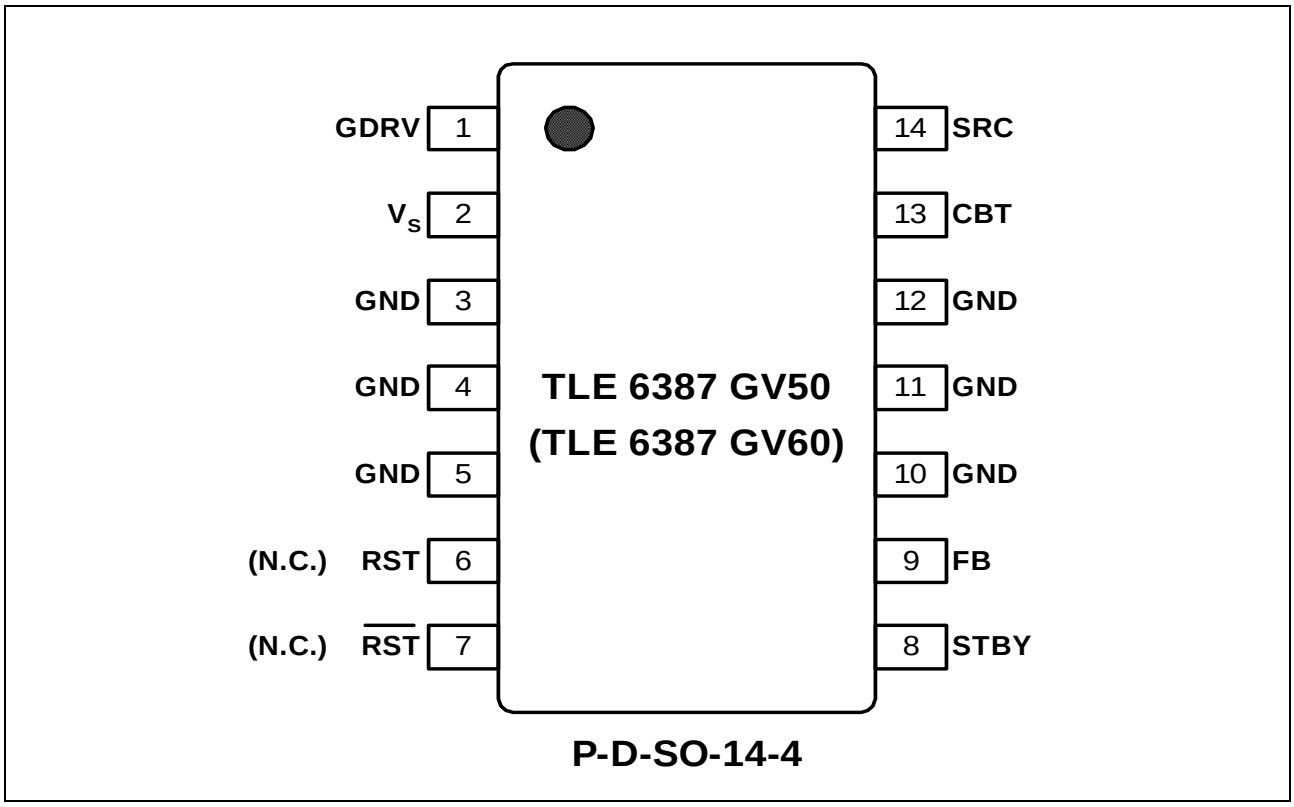
Type	Ordering Code	Package	Description
TLE 6387 GV50	on request	P-DSO-14-4	5V version
TLE 6387 GV60	on request	P-DSO-14-4	5.8V version

Functional description

The **TLE6387** DC-DC switching controllers are used to built up buck (or step down) converter circuits for loads higher 1A with efficiencies higher than 80%. The device combines the regulation loop for a buck converter topology with an output voltage supervision module that generates a reset signal in case of over- or undervoltage at the output of the step-down converter. The special observer-based adaptive current mode control scheme requires neither external compensation in terms of an RC-network nor a current sense resistor for proper operation of the buck circuit. These controllers drive an external N-channel MOSFET, allowing design flexibility for different applications by choosing the appropriate switching transistor. The high switching frequency of 400kHz

allow the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs. The output voltage is preset to 5.0V (**TLE 6387 GV50**) or 5.8V (**TLE 6387 GV60)**. Input voltages up to 60V and the wide temperature range make the device suitable for all automotive applications in the existing 12V powernet as well as in the future 42V powernet.

Pin Configuration (top view)



Pin Definitions and Functions

Pin No	Symbol	Function
1	GDRV	**Gate driver output.** Connect straight to the gate of N-channel MOS.
2	V_S	**Supply voltage input.** Battery input, connect a 100nF Capacitor to GND.
3, 4, 5, 10, 11, 12	GND	**Ground pins.** Analog signal ground .
6	RST (N.C.)	**Reset output.** Open collector output, connect via a pull up resistor of 4.7kΩ to the output of the buck converter. Only available at version GV50, at version GV60 this pin is not connected.
7	$\overline{\text{RST}}$ (N.C.)	**Inverse reset output.** Open collector output, connect via a pull up resistor of 4.7kΩ to the output of the buck converter. Only available at version GV50, at version GV60 this pin is not connected.
8	STBY	**Inhibit input.** An active high signal will disable the device, active low turns it on.
9	FB	**Feedback input.** Connect the output of the buck converter straight to this pin to get the output voltage information.
13	CBT	**Bootstrap capacitor input.** Connect a ceramic capacitor between the source of the NMOS/cathode of the freewheeling diode and this pin to obtain the gateoverdrive in switchmode operation.
14	SRC	**Source Input.** Connect this pin to the source node of the NMOS for overcurrent detection and internal current signal forming

1 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Supply Voltage Input					
1.1	Voltage	V_S	-0.5	65	V	–
1.2	Current	I_S	–	–	–	
1.3	**Bootstrap Capacitor Input**					
1.4	Voltage	V_{CBT}	-0.5	75	V	$\lvert V_{CBT} - V_{SRC} \rvert \leq$ 10V
1.5	Current	I_{CBT}	–	–	–	
1.6	**Gate Driver Output**					
1.7	Voltage	V_{GDRV}	– 1	75	V	$\lvert V_{GDRV} - V_{SRC} \rvert \leq$ 10V
1.8	Current	I_{GDRV}	–	–	–	
1.9	**Source Input**					
1.10	Voltage	V_{SRC}	– 1	65	V	
1.11	Current	I_{SRC}	–	–	–	
	Reset Output					
1.12	Voltage	V_{RST}	– 0.5	20	V	
1.13	Current	I_{RST}	–	–	–	
1.14	**Inverse Reset Output**					
1.15	Voltage	$V_{\overline{RST}}$	– 0.5	20	V	
1.16	Current	$I_{\overline{RST}}$	–	–	–	
1.17	**Inhibit Input**					
1.18	Voltage	V_{STBY}	– 0.5	8	V	
1.19	Current	I_{STBY}	–	–	–	
1.20	**Feedback Input**					
1.21	Voltage	V_{FB}	– 0.5	20	V	
1.22	Current	I_{FB}	–	–	–	

1 Absolute Maximum Ratings (cont'd)

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	ESD-Protection (Human Body Model; R=1,5kΩ; C=100pF)					
1.23	all pins to GND	V_{HBM}	–2	2	kV	
1.24	**Temperatures**					
1.25	Junction temperature	T_j	– 40	150	°C	
1.26	Storage temperature	T_{stg}	– 65	150	°C	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

2 Operating Range

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
2.1	Supply voltage range	V_S	6	60	V	Version GV50
2.2	Supply voltage range	V_S	7	60	V	Version GV60
2.3	Source voltage range	V_{SRC}	– 1	60	V	
2.4	Junction temperature	T_j	– 40	150	°C	
2.5	**Thermal Resistance**					
2.6	Junction ambient	R_{thj-a}		112	K/W	[1] PCB heat sink area 0mm^2
2.7	Junction ambient	R_{thj-a}		92	K/W	[1] PCB heat sink area 300mm^2
2.8	Junction ambient	R_{thj-a}		78	K/W	[1] PCB heat sink area 600mm^2
2.9	Junction pin	$R_{thj-pin4}$		32	K/W	

[1] Package mounted on PCB 80 x 80 x 1.5 mm^3; 35µ Cu; 5µ Sn; zero airflow

3 Electrical Characteristics

7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Voltage Supply						
3.1	Supply current into V_S	I_S	1.5	4	6.5	mA	V_{FB} = 5 V, V_S = 24 V and 55 V V_{STBY} = 0 V GDRV open

3 Electrical Characteristics (cont'd)

7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.2	Supply current into V_S	I_S		170	300	µA	V_S = 14 V, 24 V and 55 V V_{STBY} = 5 V
	Gate Driver						
3.3	Bootstrap charger, output voltage	$V_{CBT} - V_{SRC}$	5		10	V	V_{STBY} = 0 V C_{CBT} = 10 nF
3.4	Gate driver, high level output voltage	$V_{GDRV} - V_{SRC}$	5		10	V	V_{STBY} = 0 V C_{CBT} = 10 nF C_{GDRV} = 1.5 nF
3.5	Gate driver, low level output voltage	$V_{GDRV} - V_{SRC}$			0.2	V	V_{SRC} = 0 V V_{FB} = 5.5 V V_{STBY} = 0 V C_{CBT} = 10 nF C_{GDRV} = 1.5 nF
3.6	Gate driver, peak charging current	I_{GDRV}		– 0.35		A	GBD
3.7	Gate driver, peak discharging current	I_{GDRV}		1		A	GBD
3.8	Gate driver, gate charge	Q_{GDRV}	10			nC	GBD
3.9	Gate driver, rise time	$t_{r,GDRV}$		30	50	ns	GBD
3.10	Gate driver, fall time	$t_{f,GDRV}$		14	25	ns	GBD

3 Electrical Characteristics (cont'd)

7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.11	Gate driver, source current	I_{SRC}	100	275	400	µA	V_S = V_{SRC} = 55V V_{FB} = 5V V_{STBY} = 5V
3.12	Undervoltage Lockout, upper threshold voltage	V_{CBT} – V_{SRC}	2.5		4.5	V	V_{SRC} = V_{FB} = 0V V_{STBY} = 0V C_{CBT} = 10nF GDRV open
3.13	Undervoltage Lockout, lower threshold voltage	V_{CBT} – V_{SRC}	2.0		4.0	V	V_{SRC} = V_{FB} = 0 V V_{STBY} = 0 V C_{CBT} = 10 nF GDRV open
3.14	Short-circuit protection, threshold voltage	V_S – V_{SRC}	0.5	0.75	1.00	V	Version GV50
3.15	Short-circuit protection, threshold voltage	V_S – V_{SRC}	1.00	1.25	1.50	V	Version GV60
3.16	Short-circuit protection, switching delay	$t_{SC,d}$		150	250	ns	V_S = 7V V_{SRC} = 5V V_{CBT} - V_{SRC} = 7V V_{STBY} = 0V V_{FB} = 4V GDRV open
	Control Loop						
3.17	Feedback voltage	V_{FB}	4.85	5	5.15	V	Version GV50, see application circuit

3 Electrical Characteristics (cont'd)

7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.18	Feedback voltage	V_{FB}	5.70		6.00	V	Version GV60, see application circuit
3.19	Feedback voltage, line regulation	ΔV_{FB}		8	50	mV	V_S step from 6V to 24V (GV50) from 7V to 24V (GV60) and from 50V to 24V, see application circuit
3.20	Feedback voltage, load regulation	ΔV_{FB}		5	50	mV	I_L step from 0.5A to 1A, see application circuit $I_L R_L \leq 0.5$ V
3.21	Feedback current	I_{FB}	100	125	335	µA	V_{FB} =5 V V_S = 6V (GV50) V_S = 7V (GV60) V_{STBY} = 0 V
3.22	Feedback current	I_{FB}	350	470	700	µA	V_{FB} =5 V V_S =4 V or V_{STBY} = 5 V
3.23	Oscillator frequency	f_{OSC}	330	390	430	kHz	
3.24	Duty cycle, minimum	D	2		5.5	%	
3.25	Duty cycle, maximum	D	95		98	%	

3 Electrical Characteristics (cont'd)

7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.26	LC_{OUT}-filter, resonant frequency	f_{LC}	0.5	2	11	kHz	$f_{LC} = \frac{1}{2\pi\sqrt{LC}}$
3.27	Choking coil, offset voltage	$I_L \cdot R_L$			0.5	V	
	Supervision Reset Generator available at Version GV50 ONLY!						
3.28	Undervoltage, lower threshold voltage	V_{FB}	4.5	4.7	4.8	V	V_{FB} decreasing $I_{\overline{RST}}$ = 2 mA
3.29	Undervoltage, voltage hysteresis	ΔV_{FB}	40	70	100	mV	V_{FB} decreasing $I_{\overline{RST}}$ = 2 mA
3.30	Undervoltage, switching delay	$t_{UV,d}$	5	35	40	µs	V_{FB} decreasing $I_{\overline{RST}}$ = 2 mA
3.31	Overvoltage, upper threshold voltage	V_{FB}	5.2	5.4	5.5	V	V_{FB} increasing $I_{\overline{RST}}$ = 2 mA
3.32	Overvoltage, voltage hysteresis	ΔV_{FB}	50	85	120	mV	V_{FB} increasing $I_{\overline{RST}}$ = 2 mA
3.33	Overvoltage, switching delay	$t_{OV,d}$	5	35	40	µs	V_{FB} increasing $I_{\overline{RST}}$ = 2 mA
3.34	Reset, output voltage	V_{RST}			0.1	V	I_{RST} = 20 µA V_{FB} = 5 V
3.35					0.4	V	I_{RST} = 2 mA V_{FB} = 5 V
3.36		$V_{\overline{RST}}$			0.1	V	$I_{\overline{RST}}$ = 20 µA V_{FB} = 6 V
3.37					0.4	V	$I_{\overline{RST}}$ = 2 mA V_{FB} = 6 V
3.38					0.2	V	$I_{\overline{RST}}$ = 0.3 mA V_{FB} = 1 V

3 Electrical Characteristics (cont'd)

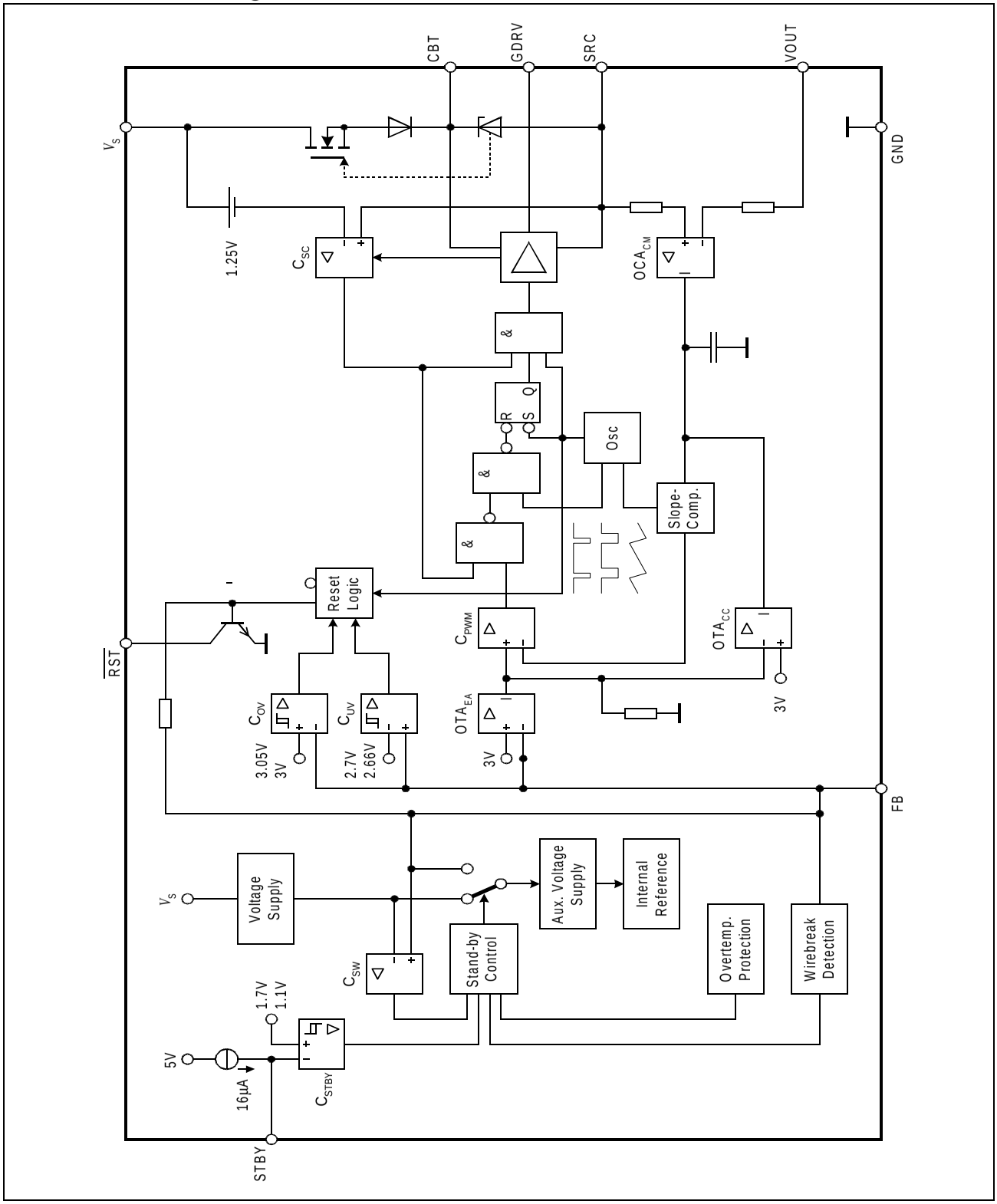
7V< V_S <36V; - 40°C< T_j <150°C;

The electrical characteristics involve the spread of values guaranteed within the supply voltage and junction temperature range given below. All voltages are given with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.39	Reset, output current	I_{RST}			2	µA	V_{RST} = 6 V V_{FB} = 6 V
3.40		$I_{\overline{RST}}$			2	µA	$V_{\overline{RST}}$ = 6 V V_{FB} = 5 V
3.41	Reset, recovery delay	t_{RST}	19	21	25	ms	V_{FB} decreasing I_{RST} = 2 mA
3.42		$t_{\overline{RST}}$	19	21	25	ms	V_{FB} decreasing $I_{\overline{RST}}$ = 2 mA
	Standby control						
3.43	Stand-by, high level threshold voltage	V_{STBY}			2	V	V_{FB} = 3 V
3.44	Stand-by, low level threshold voltage		0.8			V	V_{FB} = 3 V
3.45	Stand-by, hysteresis	ΔV_{STBY}	0.4	0.6	1.2	V	V_{FB} = 3 V
3.46	Stand-by, pull-up current	I_{STBY}	– 30	– 16	– 10	µA	V_{STBY} = 0 V
	Thermal Shutdown						
3.47	Overtemperature, upper threshold	T_{OT}		190		°C	V_{STBY} = 0 V V_{FB} = 3 V
3.48	Overtemperature, lower threshold	T_{OT}		170		°C	V_{STBY} = 0 V V_{FB} = 3 V
3.49	Overtemperature, hysteresis	ΔT_{OT}		20		°C	V_{STBY} = 0 V V_{FB} = 3 V

4 Detailed circuit description

4.1 Block diagram



4.2 Functional Description

Internal Power Supply

The TLE 6387 G internal power supply consists of an internal voltage supply, a subsequent auxiliary voltage supply and the internal voltage reference. As long as the supply voltage provided at pin 2 (V_S) is high enough, the entire controller is supplied from this voltage by means of the internal voltage supply. If the regulated voltage of the internal voltage supply, however, drops below the converter's output voltage sensed at pin 9 (FB), the auxiliary voltage supply and the internal voltage reference are immediately cut off the internal voltage supply and are supplied from the converter's output voltage, instead. In this way the output voltage supervisor, which drives the reset output, keeps on running even though the supply voltage at pin 2 (V_S) has dropped down to zero. The same switching operation is performed whenever the controller is set into stand-by, either by external request via pin 8 (STBY), by overtemperature protection or by wirebreak detection (cf. **"Stand-by Management"**).

Stand-by Management

The same switching operation as described above (cf. **"Internal Power Supply"**) is also performed, whenever the controller is set into stand-by mode, either by external request, by overtemperature protection or by wirebreak detection. While the latter are failure modes, the external stand-by request is controlled by pin 8 (STBY). As long as the voltage at pin 8 exceeds 2 V the controller is disabled. However, if the voltage at pin 8 drops below 0.8 V the controller is enabled. To avoid unintentional start-ups pin 8 is internally pulled-up. In this way the controller is disabled even if this pin is not connected.

Observer-Based Adaptive Current Mode Control

IIn order to achieve a fast and stable control with excellent line and load regulation and with a precisely controlled output voltage, TLE 6387 G uses observer-based adaptive current mode control. Like conventional current mode control it consists of two control loops. The first loop serves to control the output voltage sensed at pin 9 (FB) by means of error amplifier OTA_{EA}. The second loop is used to control the load current. Unlike conventional approaches the load current is calculated by OCA_{CM} integrating the voltage across the choking coil, i.e. between pin 14 (SRC) and pin 9 (FB). In this way the current loop can do without an additional resistor, which is usually needed to sense the load current and which reduces the overall efficiency of the DC/DC converter. To achieve a stable duty cycle at values above 50%, the current loop is furthermore equipped with an appropriate slope-compensation. In order to achieve a precise output voltage regardless of the respective load current the voltage loop and the current loop are coupled by OTA_{CC}. OTA_{CC} serves to compensate the DC voltage offset of the choking coil, which

results from its inevitable series resistance and the average load current $(I_L \cdot R_L)$. In order not to spoil the current mode signal this offset is slowly compensated using the inherent inertia of the voltage loop. Please note, since the inputs of OTA_{EA} and OCA_{CM} are internally connected, it is not possible to increase the output voltage by feeding back only a fraction of the output voltage to pin 9 (FB). In fact , whenever the generated output voltage differs from the voltage sensed at pin 9 (FB), a large DC offset is added to the internal current mode signal, which cannot be compensated by OTA_{CC} and which consequently will result in a clampled output voltage.

Protection Circuitry (only avaiable at version GV50)

To achieve a safe operation of the controller and its load connected, TLE 6387 G is equipped with different protection circuitry. To warn loads supplied of temporary undervoltages or overvoltages the output voltage is continuously supervised for undervoltages or overvoltages. To prevent the undervoltage and overvoltage comparators C_{uv} and C_{ov} from being triggered due to inevitable noise that is superimposed on the voltage sensed at pin 9 (FB), both comparators are equipped with a corresponding hysteresis as well as an input low pass filter. In case an undervoltage or overvoltage has been detected, the reset signals at pin 6 (RST) and pin 7 ($\overline{\text{RST}}$) are set according to1. If the undervoltage or overvoltage has passed both signals are reset after 21 ms. A corresponding timing diagram is given in 1 and 2.

V_{FB}	RST	$\overline{\text{RST}}$
Undervoltage	Z	L
Overvoltage	Z	L
Else	L	Z

Table 1 Reset Logic Truth Table

In order to make sure the output voltage supervisor is working properly down to an output voltage of 1 V regardless of the supply voltage at pin 2 (V_S), its supply voltage is switched between the internal voltage supply and the converters output voltage if necessary (cf. **“Internal Power Supply”**).

To protect the converter and the driven power switch from destruction due to a short-circuited output, the voltage drop across the power switch is checked cycle-by-cycle. If this voltage drop exceeds 1.25 V, the driver is immediately shut off for the remaining part of the respective cycle. As a result, the duty cycle is kept constant at a value as small as possible.

In order to prevent the output voltage from high overvoltages, which may be caused by a missing output capacitor or a broken connection between pin 9 (FB) and the output capacitor, TLE 6387 G is equipped with a smart wirebreak protection, which shortly checks the status of pin 9 (FB) whenever the controller is turned on.

To prevent the controller from overheating, the chip temperature is continuously checked. If this temperature exceeds 190 °C the controller is switched into stand-by mode until the temperature has dropped below 170 °C.

Bootstrap Driver

TLE 6387 G's bootstrap driver comprises the bootstrap capacitor charger, an undervoltage lockout and the gate driver.

By means of the bootstrap capacitor charger the bootstrap capacitor is quickly charged each duty cycle. Charging occurs as long as the gate driver is switched off and the voltage of the bootstrap capacitor does not exceed its maximum value. As soon as the capacitor is charged or the gate driver is switched on, charging is switched off.

The gate driver is equipped with a class B push-pull output stage which is actively held high or low respectively to prevent from unintentional switching of the driven transistor, which otherwise may be caused by spurious signals.

To control the gate voltage rise and fall times an external resitor can be added between GDRV and the gate of the external transistor.

4.3 Functional Block Description

Oscillator

The oscillator provides the digital clock signals required for minimum and maximum duty cycle limitation, reset delay timing and current mode slope compensation. All of these signals are derived from a saw-tooth ramp running at 400 kHz.

Error Amplifier OTA_{EA}

Being part of the voltage control loop the error amplifier OTA_{EA} serves to monitor the output voltage sensed at pin 9 (FB) with respect to an internal high precision reference voltage. Its output voltage represents the amplified difference of these input voltages.

Current Compensation Amplifier OTA_{CC}

OTA_{CC} is used to compensate the DC offset of OCA_{CM}. By means of this compensation a large effective open loop gain of the outer voltage control loop is achieved, which ensures an accurate output voltage.

Current Mode Amplifier OCA_{CM}

The current mode signal is provided by the fast current amplifier OCA_{CM}. This is done without any shunt resistor by integrating the alternating voltage drop across the choking coil.

PWM Comparator C_{PWM}

By comparison of the compensated current mode signal and the output voltage of OTA_{EA} the fast comparator C_{PWM} creates the required duty cycle.

Standby Control Comparator C_{STBY}

An external stand-by request is handled by C_{STBY}. As long as pin 8 (STBY) is not connected, the voltage at this pin is pulled-up by means of an internal current source and the controller is kept in stand-by mode (V_{STBY} > 2 V). As soon as the voltage at pin 8 (STBY) drops below 0.8 V the controller becomes active. This stand-by feature, however, does not control the operation of the reset logic's outputs at pins 6 (RST) and 7 ($\overline{RST}$). The reset logic keeps on running as long as V_{FB} > 1 V.

Overvoltage Comparator C_{OV} (Version GV50 only)

C_{OV} checks the average output voltage at pin 9 (V_{FB}) for overvoltages. In order to filter the output voltage ripple as well as transient voltage spikes the overvoltage comparator is equipped with a threshold voltage hysteresis and a low pass filter. If the upper threshold voltage is exceeded, both reset outputs are set. If afterwards the voltage at pin 9 (V_{FB}) drops below the lower threshold voltage, both reset outputs are reset as soon as the corresponding reset delay of 21 ms has past.

Undervoltage Comparator C_{UV} (Version GV50 only)

C_{UV} checks the average output voltage at pin 9 (V_{FB}) for undervoltages. In order to filter the output voltage ripple as well as transient voltage spikes the undervoltage comparator is equipped with a threshold voltage hysteresis and a low pass filter. If the voltage at pin 9 (V_{FB}) drops below the lower threshold voltage, both reset outputs are set. If afterwards the voltage at pin 9 (V_{FB}) increases above the upper threshold voltage, both reset outputs are reset as soon as the corresponding reset delay of 21 ms has past.

Short-Circuit Comparator C_{SC}

In order to allow for a broad variety of driven transistors a short-circuit condition is detected by C_{SC} as soon as the voltage drop across the respective transistor exceeds 0.75V (GV50) or 1.25V (GV60). To distinguish the large short-circuit voltage drop from the even larger voltage drop that occurs if the driven transistor is switched off, C_{SC} is enabled a fixed delay after the gate of the driven transistor is charged and disabled as soon as the driver is switched off.

4.4 Reset Over- and Undervoltage Timing Diagrams (Only at version GV50)

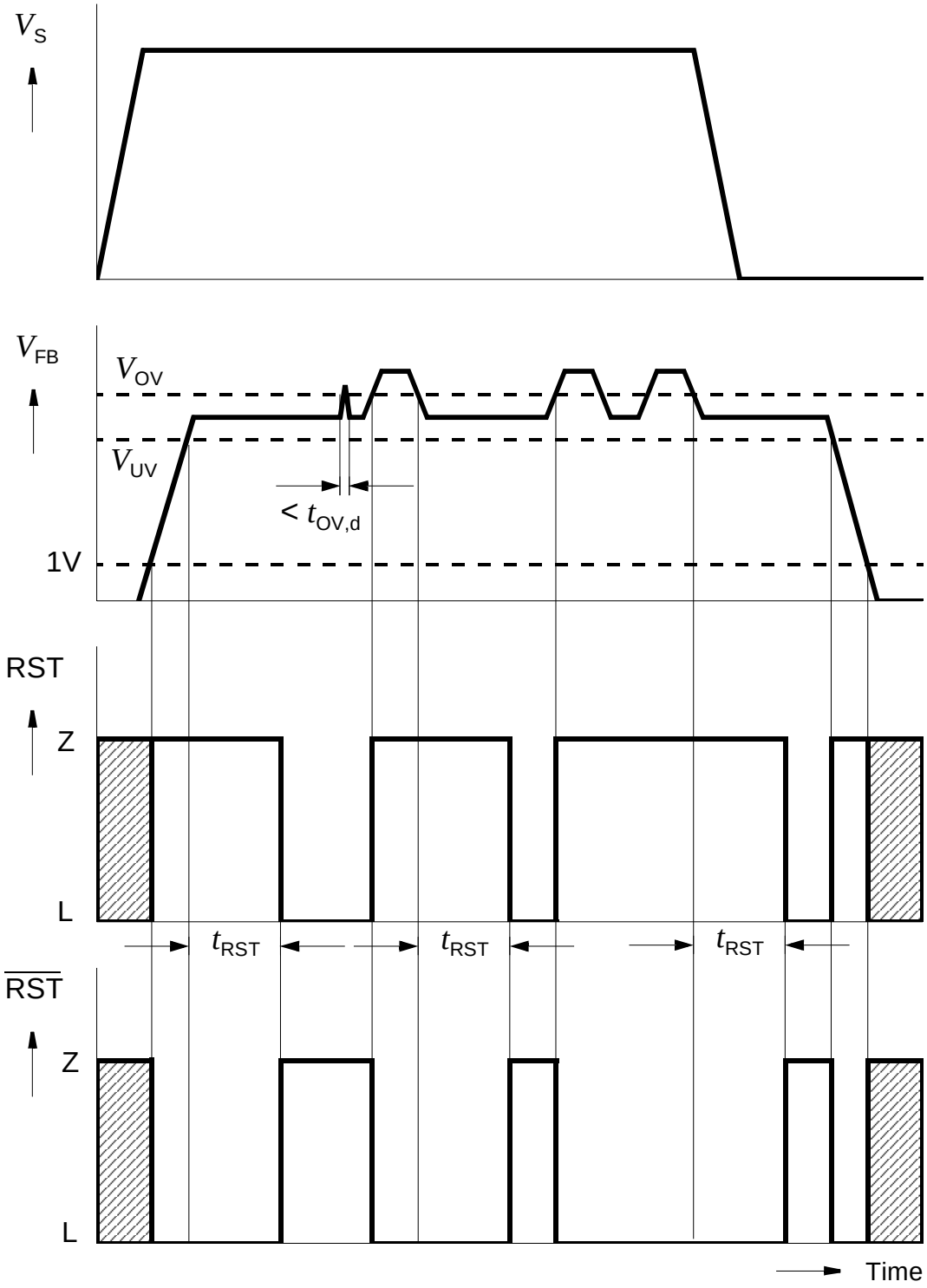


Figure 1 Voltage Supervisor Overvoltage Timing Diagram

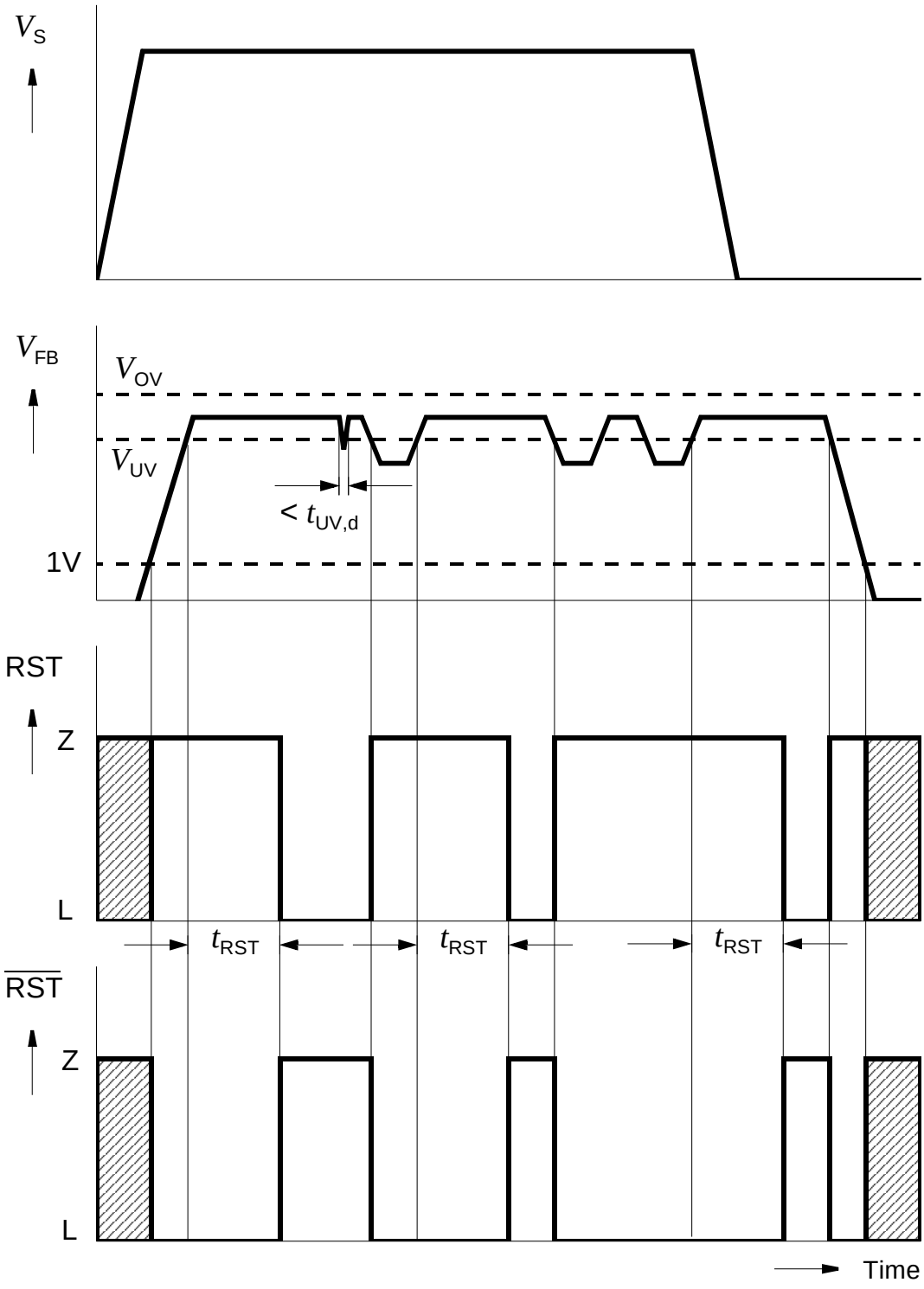


Figure 2 Voltage Supervisor Undervoltage Timing Diagram

5 Application Information

5.1 General Information

It is not possible to use the TLE 6387 to generate output voltages much higher than 5V by simply adding a voltage divider to the output and feeding back only a fraction of the output voltage to pin 9 (FB). This is due to the OTA_{EA} and OCA_{CM} being internally conected to each other. In fact, whenever the generated output voltagediffers from the voltage sensed at pin 9 (FB), a large DC-offset is added to the internal current mode signal, which cannot be compensated by OTA_{CC} and which consequently will result in a clamped output voltage.

The maximum load current which can be supplied is limited either by the power dissipation of the driven transistor, by it's gate capacitance, by the voltage drop across the ESR of the choking coil or by the resonant frequency of the output LC-filter. At short circuit condition (also start up condition) the max. current is limited by the short circuit comparator (see section 4) which turns off the NMOS according to the product RDSon times load current. So the MOSFet and the inductance (max. current rating) have to be chosen appropriate

The minimum load current which has to be supplied is basically determined by the maximum input voltage V_{IN} and the minimum duty cycle of the TLE 6387. If the load supplied is too small, the output voltage may exceed 5V. In order to cover the entire input voltage range a minimum load of 50Ω is recommended.

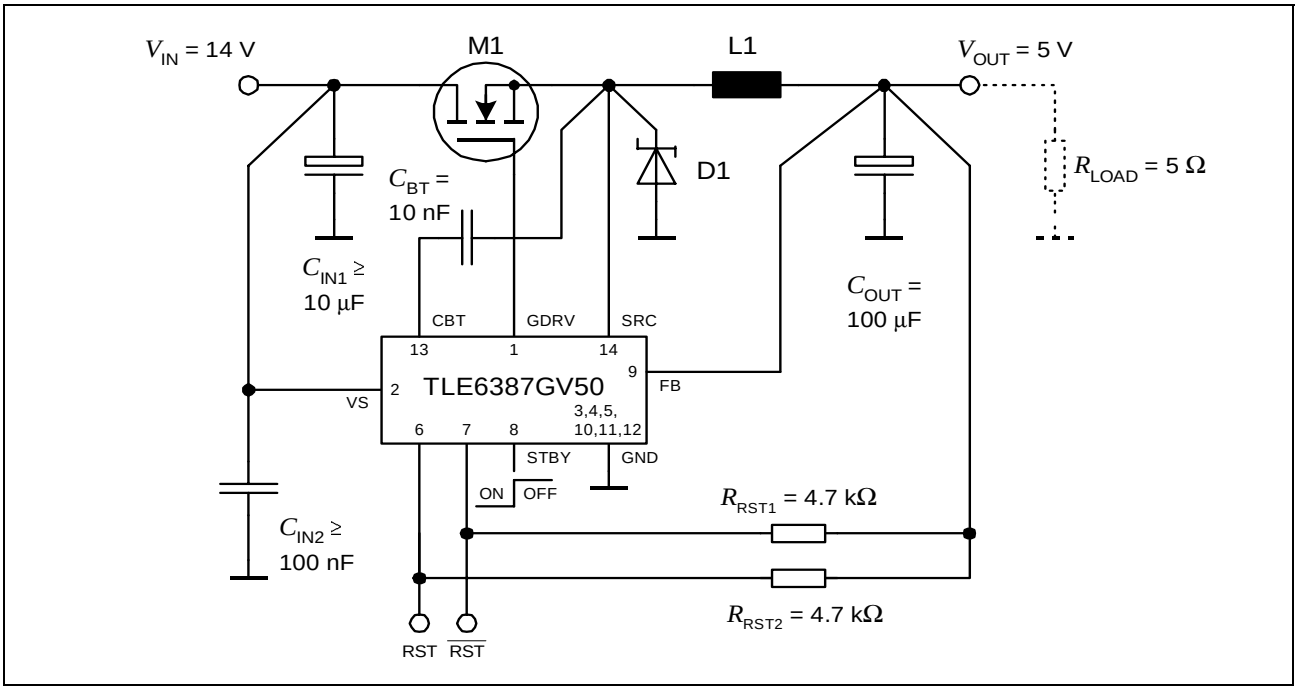


Figure 3 Typical application circuit TLE6387GV50

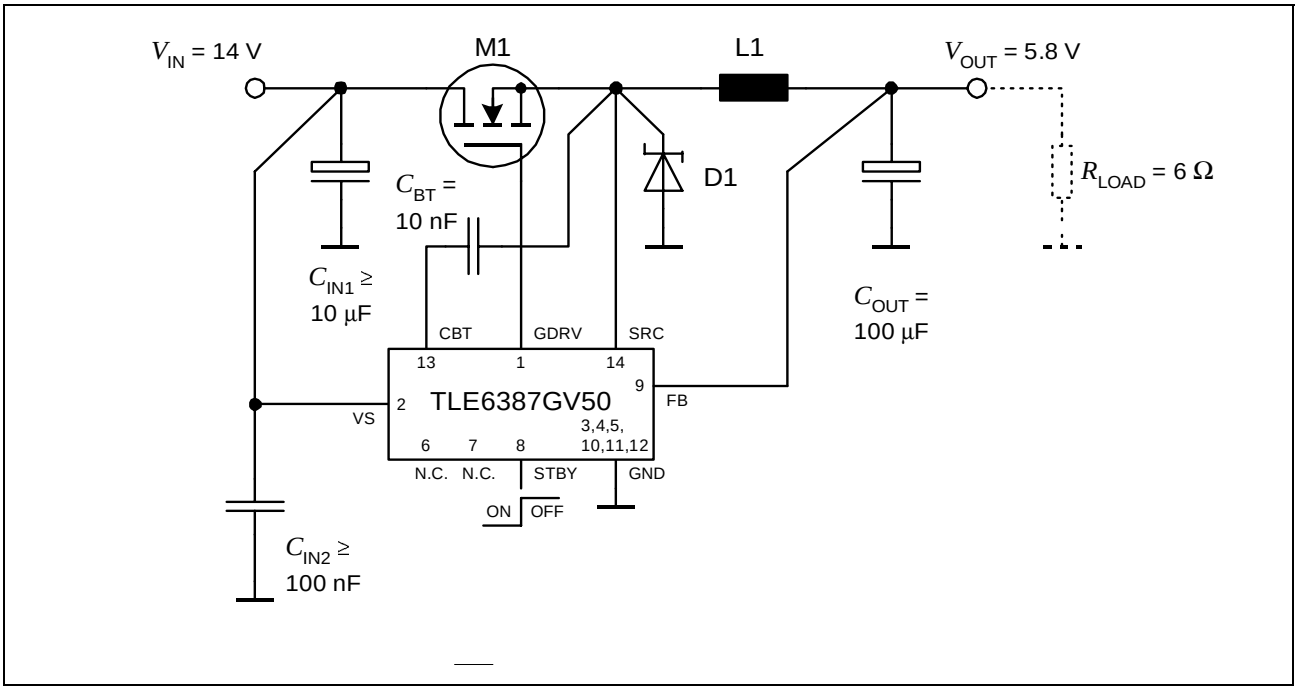


Figure 4 Typical application circuit TLE6387GV60

5.2 Component recommendation and PCB layout

Component	Supplier	Type	Remarks
L1	EPCOS	B82464-A4473-M	47µH,
	Coilcraft	DO3316P-473	47µH, 1.6A, 140mΩ
		DO5022P-473	47µH, 4.5A, 86mΩ
		DO3340P-473	47µH, 3.8A, 110mΩ
M1	Infineon	BSP296	RDSon=0.8Ω, 1.0A
D1	Motorola	MBRD360	Schottky, 60V, 3A
C_{IN1}	various	Electrolyte or low ESR tantalum	≥ 10µF, 63V
C_{IN2}	EPCOS	B37872-K1104-K62	Ceramic X7R, 100nF, 100V
	TDK	C3216X7R2A104M	Ceramic X7R, 100nF, 100V
C_{BT}	EPCOS	B37941-K0103-K60	Ceramic X7R, 10nF, 25V
	TDK	CKCL44X7R1E103M	Ceramic X7R, 10nF, 25V
C_{OUT}	EPCOS	B45194-E3107-+40*	Low ESR tantalum, 100µF, 16V
	EPCOS	B45194-E3476-+40*	Low ESR tantalum, 47µF, 16V

In order to largely avoid electromagnetic interference pin 2 (V_S), V_{IN} and the drain of the driven MOSFet should be directly connected to C_{IN1}. In a similar manner pin 14 (SRC), the source of the transistor, the bootstrap capacitor C_{BT} and the inductance L should be connected to the cathode of the freewheeling diode via a conducting area/surface on the PCB to avoid parasitric effects when being connected only through the conducting paths. Pin 9 (FB), R_{RST1}, R_{RST2}, the other terminal of L and the driven load R_{LOAD} should be directly connected to C_{OUT} and the GND-terminals of C_{IN1}, C_{IN2} TLE 6387 and the freewheeling diode should be star-connected to the GND terminal of C_{OUT}.

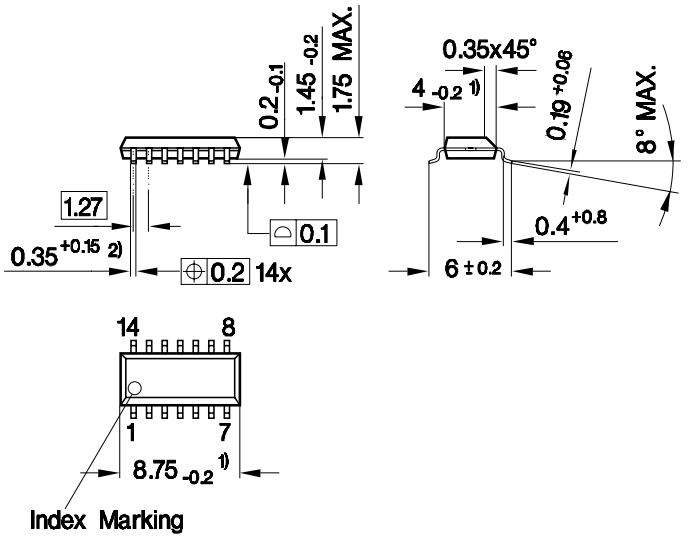
The line connecting pin 1 (GDRV) and the gate of the driven transistor as well as the wires connecting C_{BT} should be as short as possible. C_{IN1} should be placed as close as possible to the drain of the MOSFet and the path connecting pin 2 (V_S) and C_{IN1} should be as short as possible.

In order to enhance cooling of the TLE 6387 which may be necessary when operating at high ambient temperatures, any of its GND pins should be connected to a heatsink area.

To handle the increased start up currents it is strongly recommended to use a freewheeling diode which is capable of conducting three times the nominal load current. For the same reason the inductance has to be chosen accordingly to stay out of saturation during start-up.

6 Package Outlines

P-DSO-14-4
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS05093

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

Published by Infineon Technologies AG,
St.-Martin-Strasse 53
D-81541 München

Attention please!

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