TLE 6361 G

Multi-Voltage Processor Power Supply

Target Data

1 Overview

P-DSO-36-12

1.1 Features

- Switched mode pre-regulator 5.5V / 1.5A
- Three high current linear post-regulators:
  Version 1:
  5V / 800mA
  3.3V or 2.6V / 400mA
  5V or 3.3V / 300mA
  Version 2:
  5V / 800mA
  3.3V or 2.6V / 400mA
  3.1V or 2.6V / 300mA
- Three independent reset circuits
  for each linear post-regulator
- Six voltage trackers 5V / 15mA
- 5.5V to 60V input voltage
- Suitable for standard 12V /24 V supply and
  42V PowerNet
- High Efficiency
- Stand-by mode with 1mA stand-by linear regulator
- Power on reset
- SPI window watchdog
- SPI for post regulator and tracker control and diagnosis
- All outputs protected against short-circuit
- EMI and EME suitable for automotive electronics
- P-DSO-36-12 package

Type	Ordering Code	Package
TLE 6361 GV1	Q 67006-A9507	P-DSO-36-12
TLE 6361 GV2		P-DSO-36-12

SMD = Surface Mounted Device

1.2 Functional Description

The **TLE 6361 G** is a power supply circuit especially designed for automotive applications with standard 12V / 24 V supply voltage or the new 42 V powernet. The device is intended to supply 32 bit micro-controller systems requiring different supply voltages such as 5V, 3.3V, 3.1V and 2.6V.

The **TLE 6361 G** contains a buck converter that delivers a pre-regulated voltage of 5.5V. Three linear post-regulators generate 5V, 3.3V or 2.6V and depending on the version 5V or 3.3V and 3.1V or 2.6V output voltages. 6 voltage trackers with 5V are available in addition to supply sensors or other subsystems.

The tracker output voltages are linked to the 5V linear regulator output Q_LDO1. The tracker outputs are controlled by a 16 bit serial peripheral interface (SPI). Through this interface also status information can be read out.

To monitor the micro-controller and its supply voltage, an independent undervoltage reset function for each linear post-regulator and a window watchdog are available.

To save power, e. g. while the motor is turned off, the **TLE 6361 G** can be powered down with only a 1mA stand-by regulator remaining active.

The **TLE 6361 G** is based on Infineon Power technology SPT which allows bipolar , CMOS and Power DMOS circuitry to be integrated on the same monolithic circuitry.

2 Pin Configuration

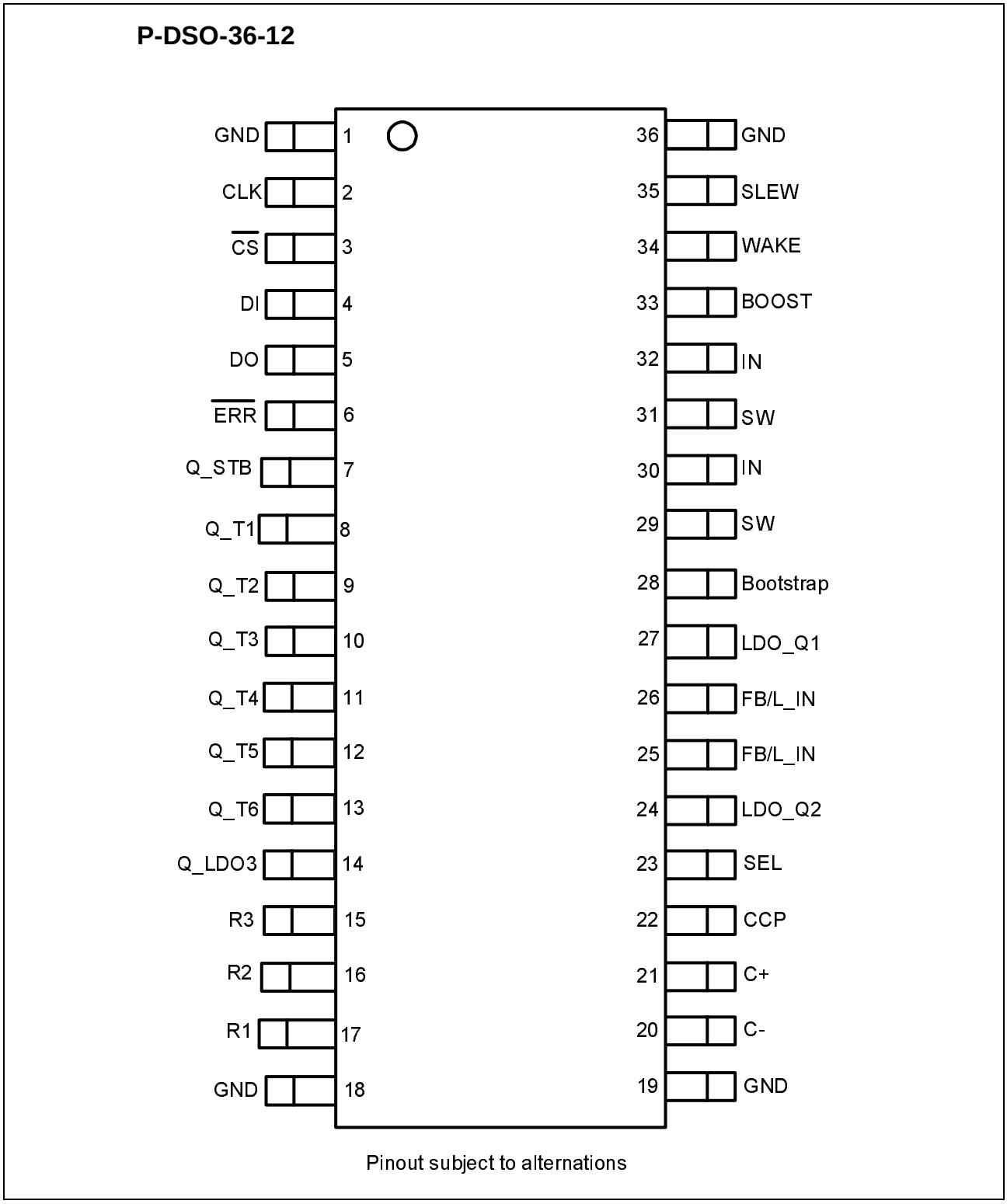


Figure 1 Pin Configuration (Top View)

rcuit Information

2.1 Pin Definitions and Functions

Pin No.	Symbol	Function
1,18,19, 36	GND	**Ground**; to reduce thermal resistance place cooling areas on PCB close to this pins.
30, 32	IN	**Supply Voltage Input;** connect both pins externally through short traces.
25, 26	FB/L_IN	**Feedback and Linear Regulator Input**;
33	BOOST	**Boost Input**; connect directly to IN in 12/24V applications. Connect to IN in 42V applications with 100nF ceramic capacitor and to the buck converter outout via a 22Ω resistor to reduce power dissipation.
28	Bootstrap	**Bootstrap Input**; add the bootstrap capacitor between pin SW and pin Bootstrap
29, 31	SW	**Switch Output;** connect both pins externally through short traces.
35	SLEW	**Slew control Input**; a resistor defines the current slope in the buck switch
20	C-	**Charge pump capacitor connection**; Add the fly-capacitor between C+ and C-
21	C+	**Charge pump capacitor connection**; Add the fly-capacitor between C+ and C-
22	CCP	**Charge Pump Storage Capacitor Output**; Add the storage capacitor between pin CCP and GND.
27	Q_LDO1	Voltage Regulator **Output 1; 5V output;** it is reference for the voltage trackers.The SPI and window watchdog logic is supplied from this voltage.
24	Q_LDO2	Voltage Regulator **Output 2; 3.3V or 2.6V output;** output voltage is selected by pin SEL (see also 3.4.2);
14	Q_LDO3	Voltage Regulator **Output 3; 5V (3.1V) or 3.3V (2.6V) output;** ouput voltage is selected by pin SEL (see also 3.4.2); it can be switched off by SPI command.
8	Q_T1	Voltage **Tracker Output T1** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.
9	Q_T2	Voltage **Tracker Output T2** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.

2.1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
10	Q_T3	Voltage **Tracker Output T3** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.
11	Q_T4	Voltage **Tracker Output T4** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.
12	Q_T5	Voltage **Tracker Output T5** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.
13	Q_T6	Voltage **Tracker Output T6** tracked to Q_LDO1; bypass with a 1uF electrolythic capacitor. It is switched on and off by SPI command. Keep open, if not needed.
23	SEL	**Select Pin** for output voltage Q_LDO2 and Q_LDO3 (see also 3.4.2)
34	WAKE	**Wake Up Input**;
17	R1	**Reset output 1** for output Q_LDO1 and watchdog reset; open drain output ; an external pullup resistor is required
16	R2	**Reset output 2** for output Q_LDO2; open drain output; an external pullup resistor is required
15	R3	**Reset output 3** for output Q_LDO3; open drain output; an external pullup resistor is required
2	CLK	**SPI Interface Clock input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs;see also chapter SPI
3	$\overline{CS}$	**SPI Interface chip select input**; $\overline{CS}$ is an active low input; serial communication is enabled by pulling the $\overline{CS}$ terminal low; $\overline{CS}$ input should only be switched when CLK is low; $\overline{CS}$ has an internal active pull up and requires CMOS logic level inputs ;see also chapter SPI
4	DI	**SPI Interface Date input;** receives serial data from the control device; serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) being transferred first; the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see also chapter SPI

2.1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
5	DO	**SPI Interface Data output;** this tristate output transfers diagnosis data to the controlling device; the output will remain 3-stated unless the device is selected by a low on Chip-Select $\overline{CS}$; see also the chapter SPI
6	$\overline{ERR}$	**Error output**; push-pull output. Monitors failures in parallel to the SPI diagnosis word, reset via SPI. $\overline{ERR}$ is a latched output.
7	Q_STB	**Standby Regulator Output**; the output is active even when the buck regulator and all other circuitry is in off mode

3 Circuit Information

3.1 Block Diagram

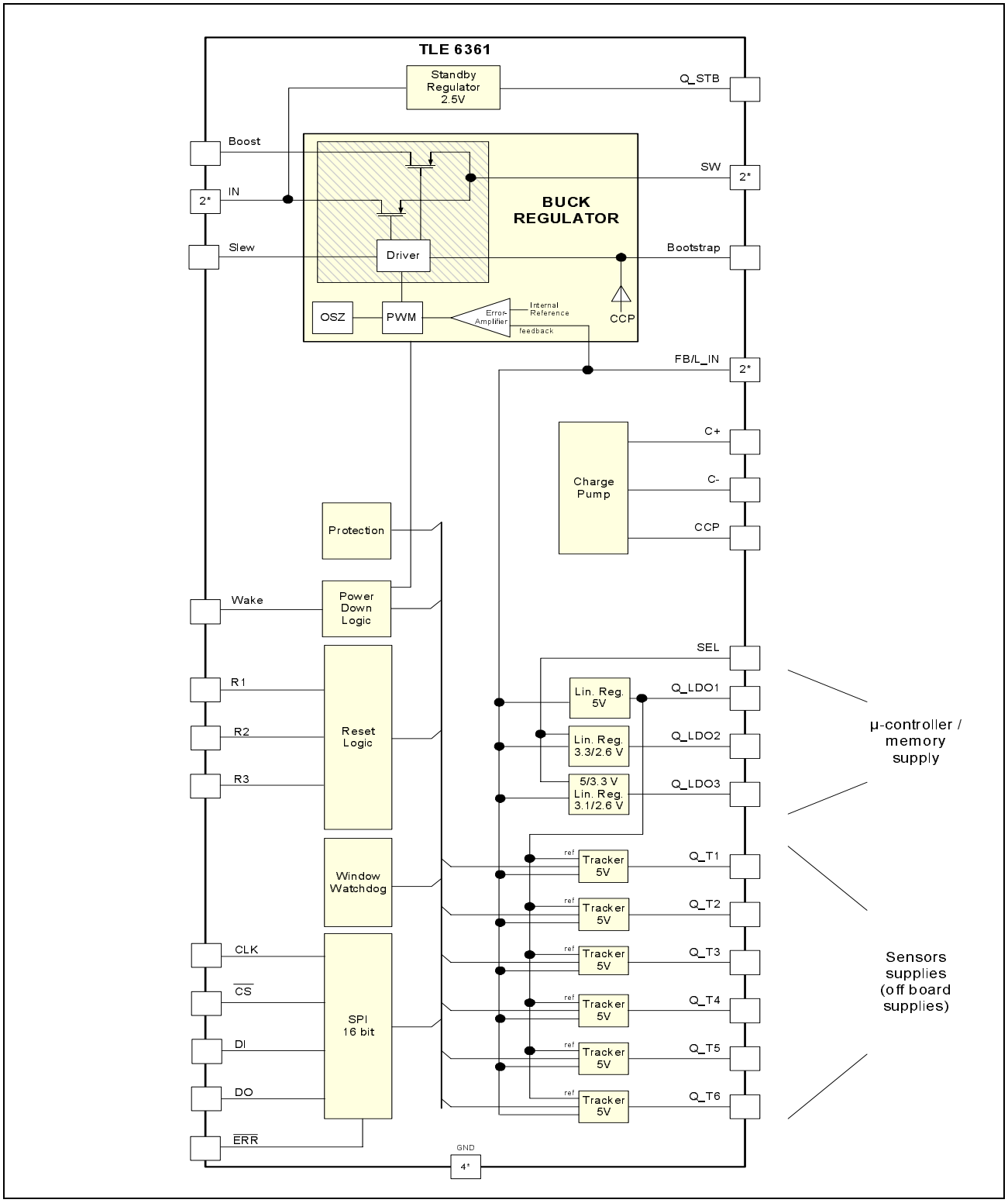


Figure 2 Block Diagram

3.2 General Description

The block diagram shows the major buck regulator blocks, the linear voltage regulators, reset, watchdog and SPI. In the application section also the required external components are shown and discribed.

3.3 Buck Regulator

The buck regulator consists of a DMOS power switch with driver, pulse width modulator, oscillator and feedback amplifier. The oscillator frequency is 330 kHz.

The error amplifier compares the feedback voltage to an internal reference and regulates the duty cycle of the PWM signal.

The pulse width modulator operates in current mode for best loop stability. The PWM can turn on the switch staticly if the IN-voltage is low.

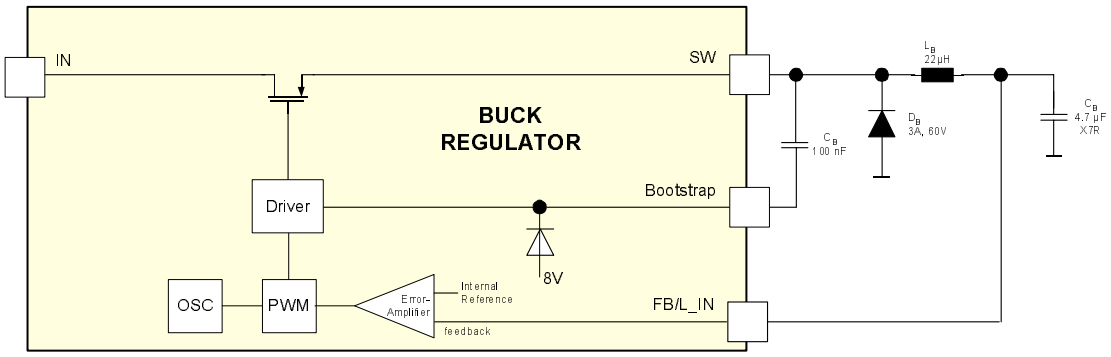


Figure 3 Buck Regulator Principle

The buck regulator is designed for output currents up to 1.5A.

3.3.1 Current Transition Time

To limit the bandwidth of the switching transients the current slope can be set by an external resistor within 20ns to 80ns transition time.

3.4 Linear Voltage Regulators

There are three voltage regulators, which operate as post-regulators for the switching regulator.

The voltage regulators are short circuit protected and have a low dropout voltage.

Q_LOD1 has 5V nominal output voltage.

Q_LOD2 has a hardware programmable output voltage of 3.3V or 2.6V (SEL input pin).

Q_LDO3 is programmable to 5V or 3.3V at version 1 and 3.1V or 2.6V at version 2 by pin SEL. It is on by default and can be switched off by SPI command.

3.4.1 Startup Sequence Linear Regulators

The following Startup-Sequence is defined:

$V_{Q\_LDO2} \leq V_{Q\_LDO1;}$ $V_{Q\_LDO3} \leq V_{Q\_LDO1,}$ if in 3.3V mode

Note:
The power sequencing refers to the regulator itself, externally voltages applied at Q_LDO2 and Q_LDO3 are not pulled down actively by the device if Q_LDO1 is at zero volts. That means if different output capacitors and different loads at the three outputs of the linear regulators are used the voltages at Q_LDO2 and Q_LDO3 might be higher than at Q_LDO1. To avoid this behaviour three Schottkydiodes have to be connected between the outputs of the linear regulators.

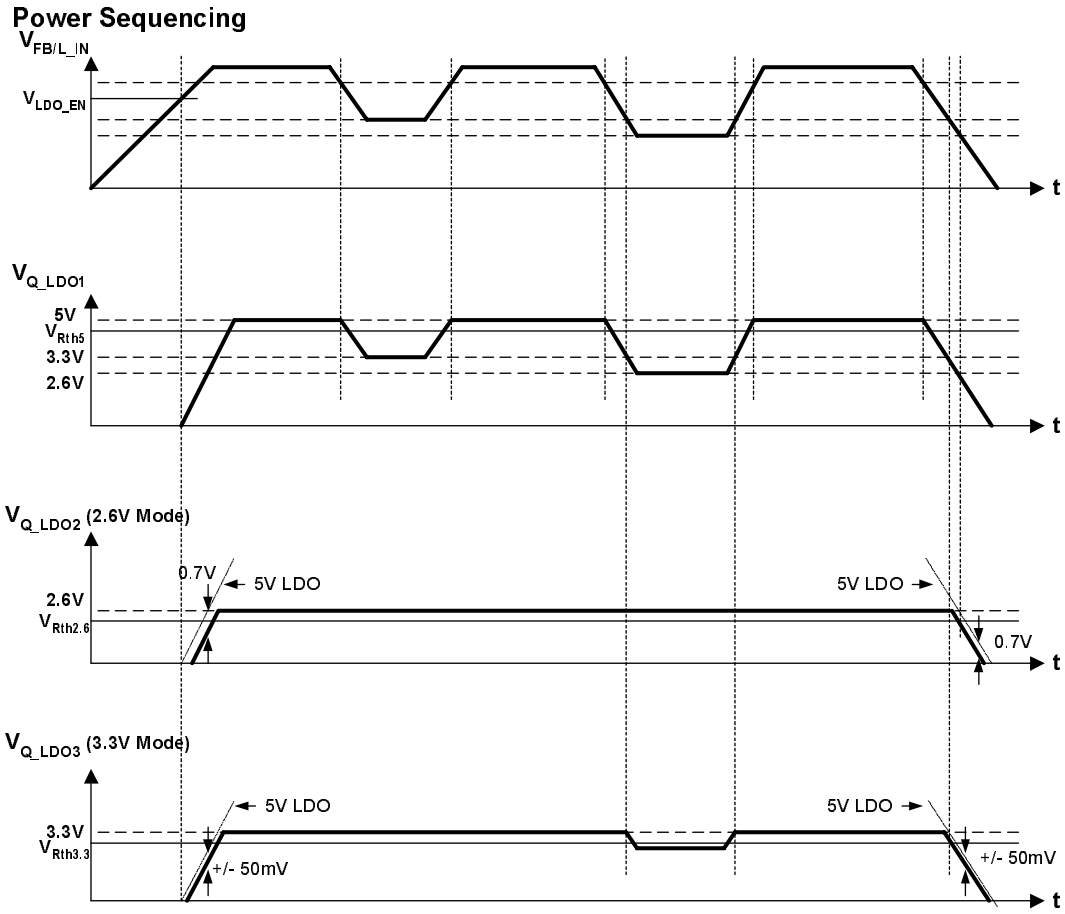


Figure 4 Power-up and -down sequence

3.4.2 Q_LDO2 and Q_LDO3 programming

Definition of Output voltage Q_LDO2 and Q_LDO3

	Version 1		Version 2	
Select Pin SEL connected to	**Q_LDO2 output voltage**	**Q_LDO3 output voltage**	**Q_LDO2 output voltage**	**Q_LDO3 output voltage**
GND	3.3 V	5 V	3.3 V	3.1 V
LDO_Q1	2.6 V	3.3 V	2.6 V	2.6 V
LDO_Q2	2.6 V	5 V	2.6 V	3.1 V

3.5 Voltage Trackers

Six voltage trackers Q_T1 to Q_T6 with 15mA output current each are intended for any subsystem that should be controlled by the microcontroller. They are especially designed to supply off board systems like sensors. The tracker outputs can withstand short circuit to Ground or battery.

The output voltages match Q1 within +5 / -15mV. They can be turned on and off individually by an SPI command and are protected against short circuit to voltages from -4V to +40V. A short circuit can be detected by reading out the SPI.

3.6 Standby Regulator

The standby regulator is an ultra low power 1mA - 2.5V linear voltage regulator. It is on all the time. It is intended to supply the microcontroller in stop mode. It requires only a minimum quiescent current to extend the battery lifetime.

3.7 Charge Pump

A 1.6 MHz charge pump will serve to supply the NPN linear regulators LDO_Q1, LDO_Q2 and LDO_Q3 as well as the buck transistor in 100% duty cycle mode.

3.8 Power On Reset

A power on reset is available for each LDO output which is active during start up and goes inactive with a reset delay time after V_LDO1, V_LDO2 or V_LDOV3 reached their reset threshold.

The reset delay time is 64 ms by default and can be set to 8 ms, 16 ms 32 ms or 64ms by SPI command. All reset outputs are open drain and active low. They can be wired OR'ed on the PCB.

3.9 RAM good flag

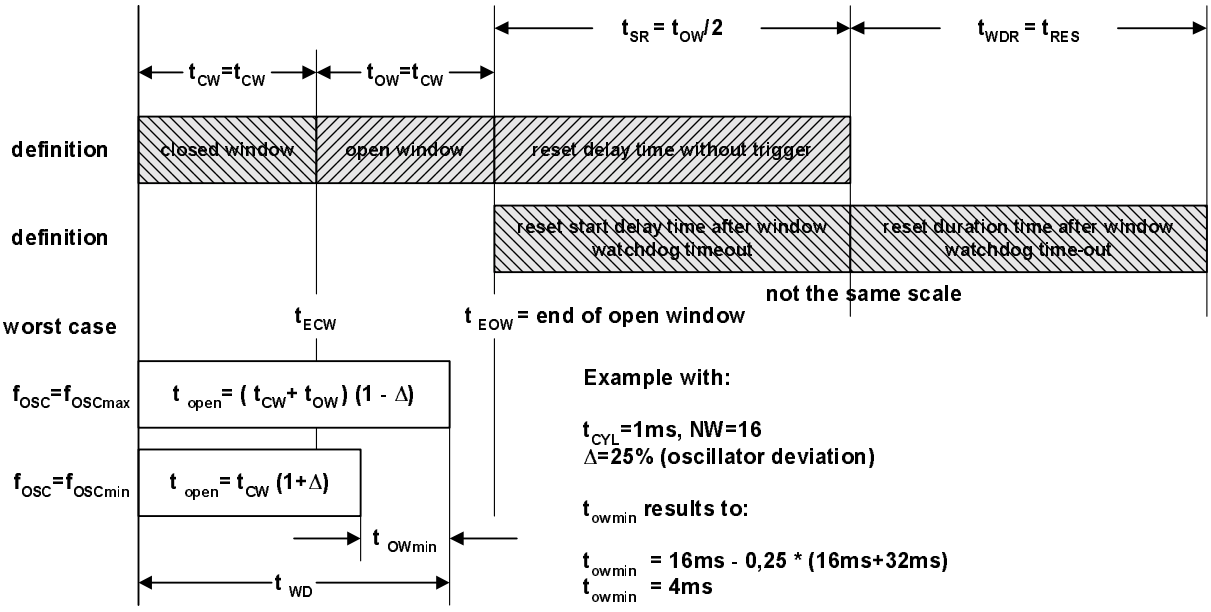
A RAM good flag will be set when the Q_LDO1 voltage drops below 2.5V. A second one will be set if Q_LDO2 drops below 1.5V. Both RAM good flags can be read after power up to determine if a cold or warm start needs to be processed. Both RAM good flags will be reset after each SPI cycle.

3.10 $\overline{\text{ERR}}$ Pin

An error pin indicates any fault conditions of the device. It should be connected to an interrupt input of the microcontroller. A low signal indicates an error condition. The microcontroller can read the root cause of the error by reading the SPI register.

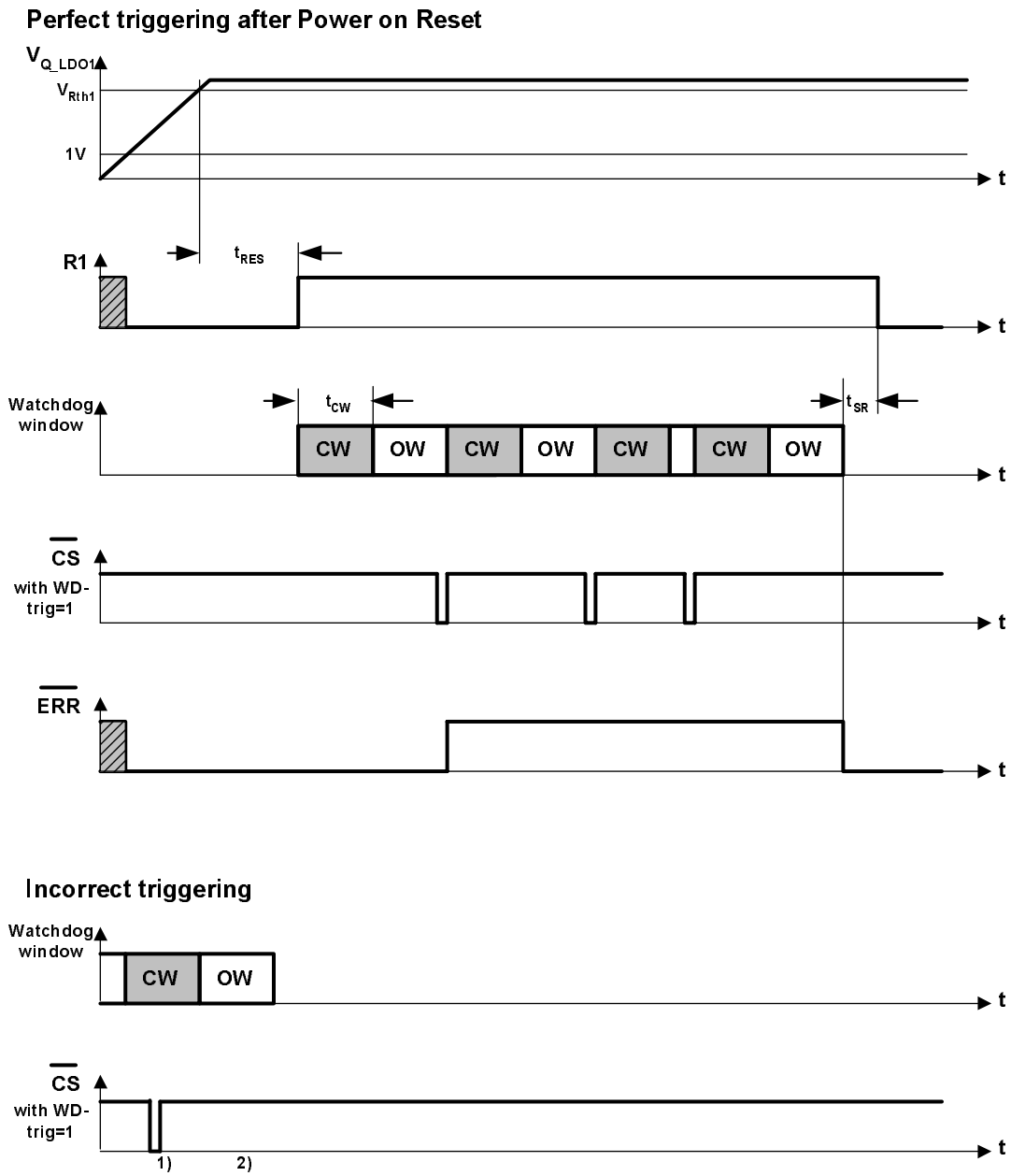
3.11 Window Watchdog

The window watchdog logic is triggered when $\overline{CS}$ is low and Bit WD-Trig is set 1. To allow reading the SPI at any time the WD-Trig bit has to be set 0 to avoid false trigger conditions. To disable the window watchdog the WD-OFF bits need to be set 010.



Worst case open window time: $t_{OWmin} = t_{OW} - \Delta * (t_{OW} + 2 * t_{CW})$

Figure 5 Window Watchdog Timing Definition



1) Pretrigger
2) Missing trigger

Legend: OW = Open window
CW = Closed window

Figure 6 Window Watchdog Timing

3.12 Overtemperature Protection

At a chip temperature of more than 150° an error flag is set and can be read through the SPI. The device is switched off if the device reaches the overtemperature threshold. The overtemperature shutdown has a hysteresis to avoid thermal pumping.

3.13 Power Down Mode

The **TLE 6361 G** is started by a static high signal at the wake input or a high pulse with 50us minimum duration at the Wake input.

By SPI command all voltage regulators including the switching regulator except the standby regulator can be turned off, if the wake input is low.

3.14 Serial Peripheral Interface

A standard 16bit SPI is available for control and diagnostics. It is capable to operate in a daisy chain. It can be written or read by a 16 bit SPI interface or a 8 bit SPI interface.

The 16-bit wide programming word (input word, see figure 7) is read in via the data input DI, and this is synchronised with the clock input CLK supplied by the µC. The diagnosis word appears synchronously at the data output DO (see figure 8).

The transmision cycle begins when the TLE6361 is selected by the chip select not input $\overline{CS}$ (H to L). After the $\overline{CS}$ input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses. For details of the SPI timing please refer to figure 9 to 11.

The SPI will be reset to default values if the RAM good flag of LDO1 indicates a cold start. The reset will be active as long as the power on reset is present.

The register content - including watch dog timings - is maintained if the RAM good flag of LDO1 indicates a warm start.

3.14.1 Write mode

3.14.2 Write mode bit assignment

BIT	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D 15
Name	WD_OF F1	LDO3-control	T1-control	T2-control	T6-control	T4-control	T5-control	T6-control	sleep	WD_OF F2	reset 1	reset 2	WD 1	WD 2	WD_OF F3	WD-Trig
Default	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0

Figure 7 Write Bit assignment

Write Bit meaning

Function	Bit	Combination	Default
Linear Regulator 3 - control: turn on/off LDO3	D1	0: OFF 1: ON	1
Tracker 1 to 6 - control: turn on/off the individual trackers	D2 D3 D4 D5 D6 D7	 0: OFF 1: ON	0
Power down: send device to sleep	D8	0: SLEEP 1: NORMAL	1
Reset timing: Reset delay time t_{RES}	D10D11	00: 64ms 10: 32ms 01: 16ms 11: 8ms	00
Window watchdog timing: Open window time t_{OW} and closed window time t_{CW}	D12D13	00: 128ms 10: 64ms 01: 32ms 11: 16ms	00
Window watchdog function: Enable /disable window watchdog	D0D9D14	010: OFF 1xx: ON x0x: ON xx1: ON	111
Window watchdog trigger: Enable / disable window watchdog trigger	D15	0: not triggered 1: triggered	1

3.14.3 Read mode

3.14.3.1 Read mode bit assignment

BIT	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D 15
Name	ERROR	temp_ warn	T1-status	T2-status	T3-status	T4-status	T5-status	T6-status	RAM Good 1	RAM Good 2	WD Window	R-Error1	R-Error2	R-Error3	WD Error	DC/DC status
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 8 Read Bit assignment

Read Bit meaning

Function	Type	Bit	Combination	Default
Errorindication, explanation see below	Latched	D0	0: normal operation 1: fail function	0
Overtemperature warning	Not latched	D1	0: normal operation 1: prewarning	0
Status of Tracker Output Q_T[1:6],only if output is ON	Not latched	D2 D3 D4 D5 D6 D7	0: settled output voltage 1:Tracker turned off or shorted output	0
Indication of cold start/ warm start	Latched	D8	0: cold start 1: warm start	0
Indication of cold start/ warm start	Latched	D9	0: cold start 1: warm start	0
Indication for open or closed window	Not latched	D10	0: open window 1: closed window	0
Reset condition at output Q_LDO1	Not latched	D11	0: normal operation 1: Reset R1	0
Reset condition at output Q_LDO2	Not latched	D12	0: normal operation 1: Reset R2	0
Reset condition at output Q_LDO3, only when Q_LDO3 on	Not latched	D13	0: normal operation 1: Reset R3	0
Watchdog Error	Latched	D14	0: normal operation 1: WD error	0
DC/DC converter status	Not latched	D15	0: off 1: on	1

The error output is high and the error bit indicates fail function if the temperature prewarning or the watchdog error is active, if one RAM good indicates cold start or if a voltage tracker does not settle within 1ms when it is turned on.

3.14.4 SPI Timings

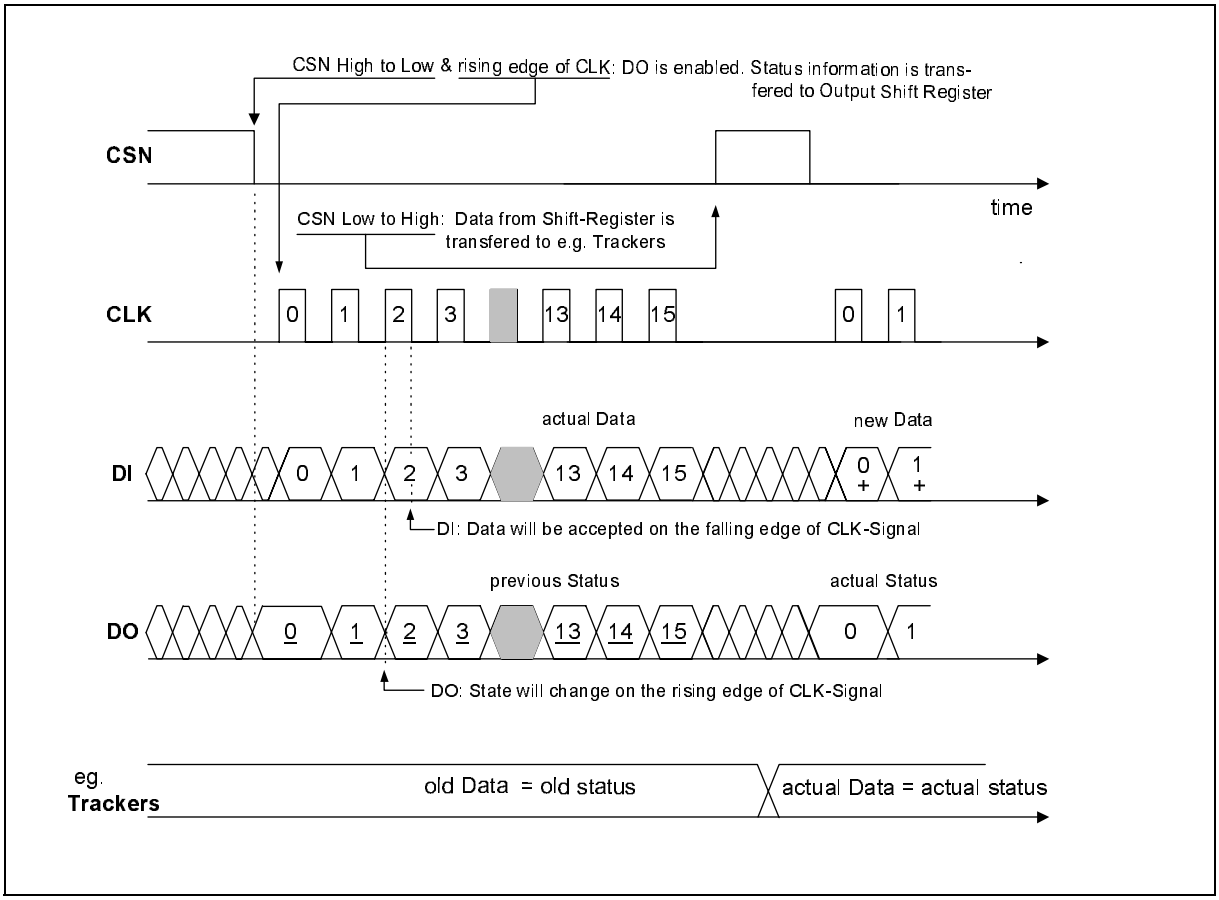


Figure 9 SPI Data Transfer Timing

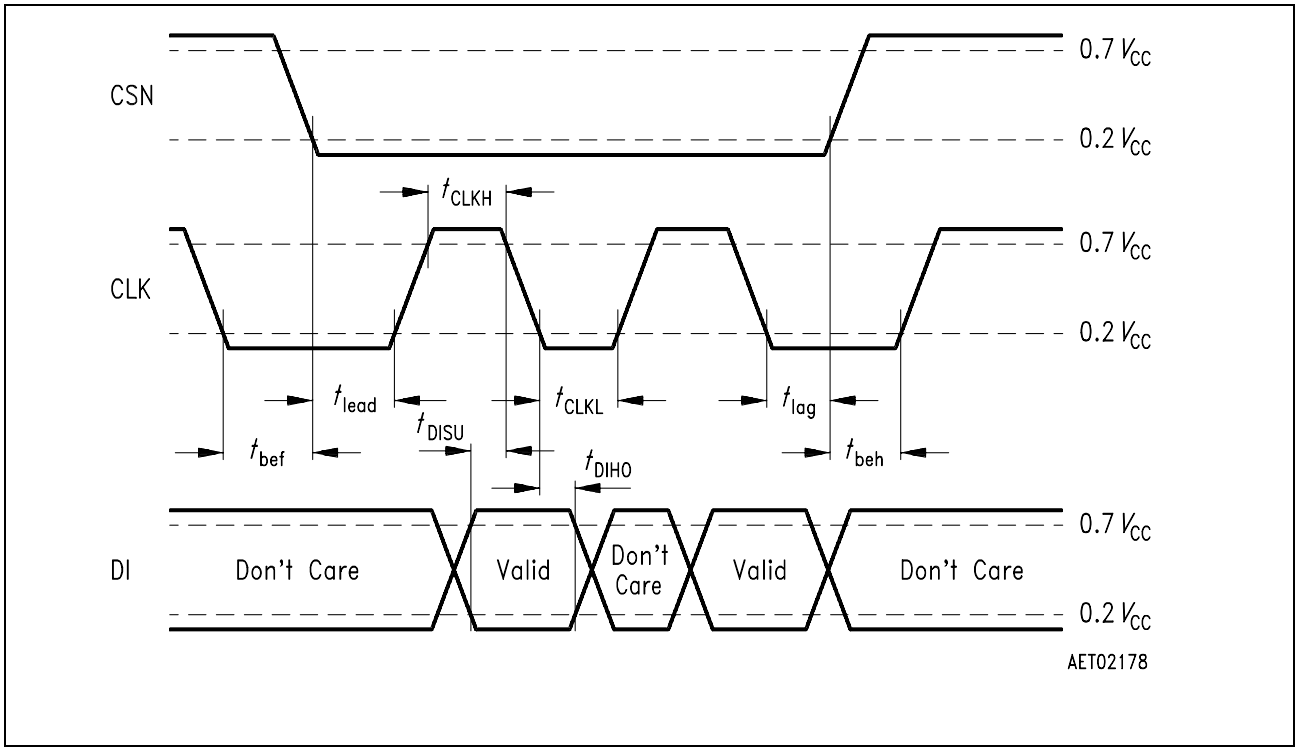


Figure 10 SPI-Input Timing (CSN = $\overline{CS}$)

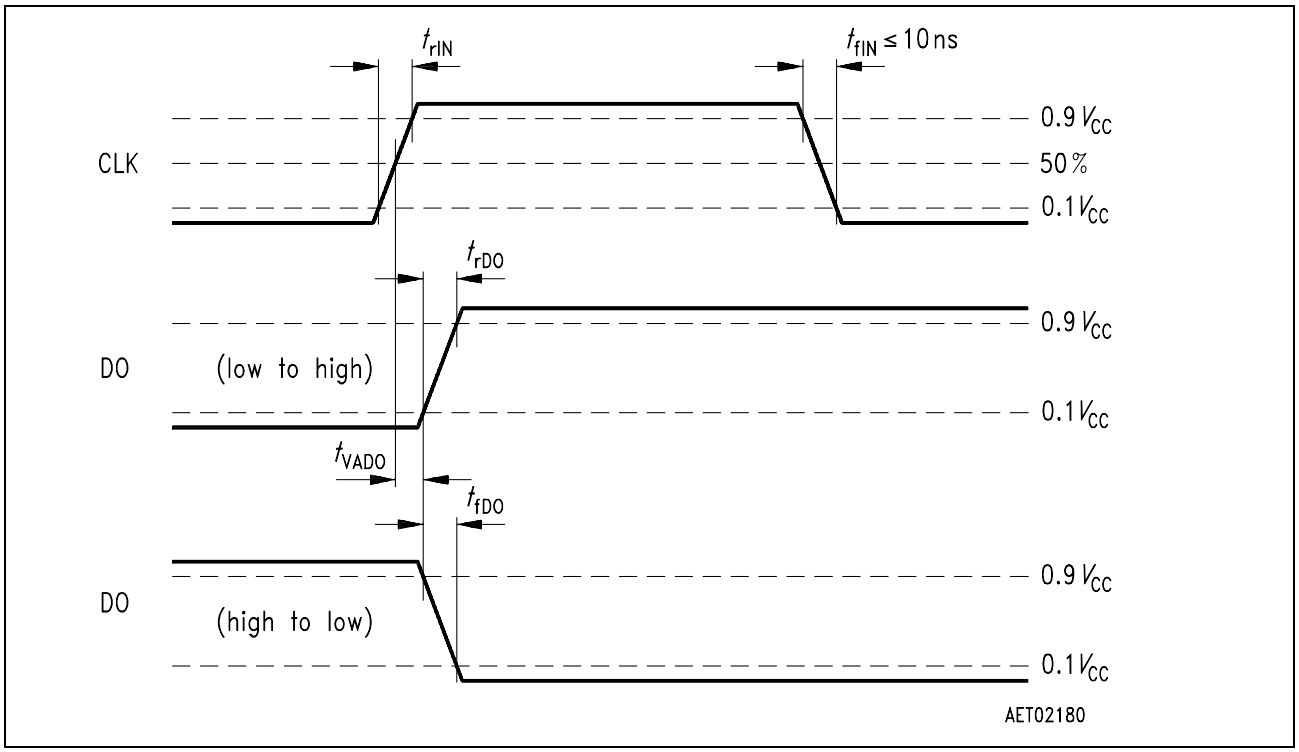


Figure 11 DO Valid Data Delay Time and Valid Time

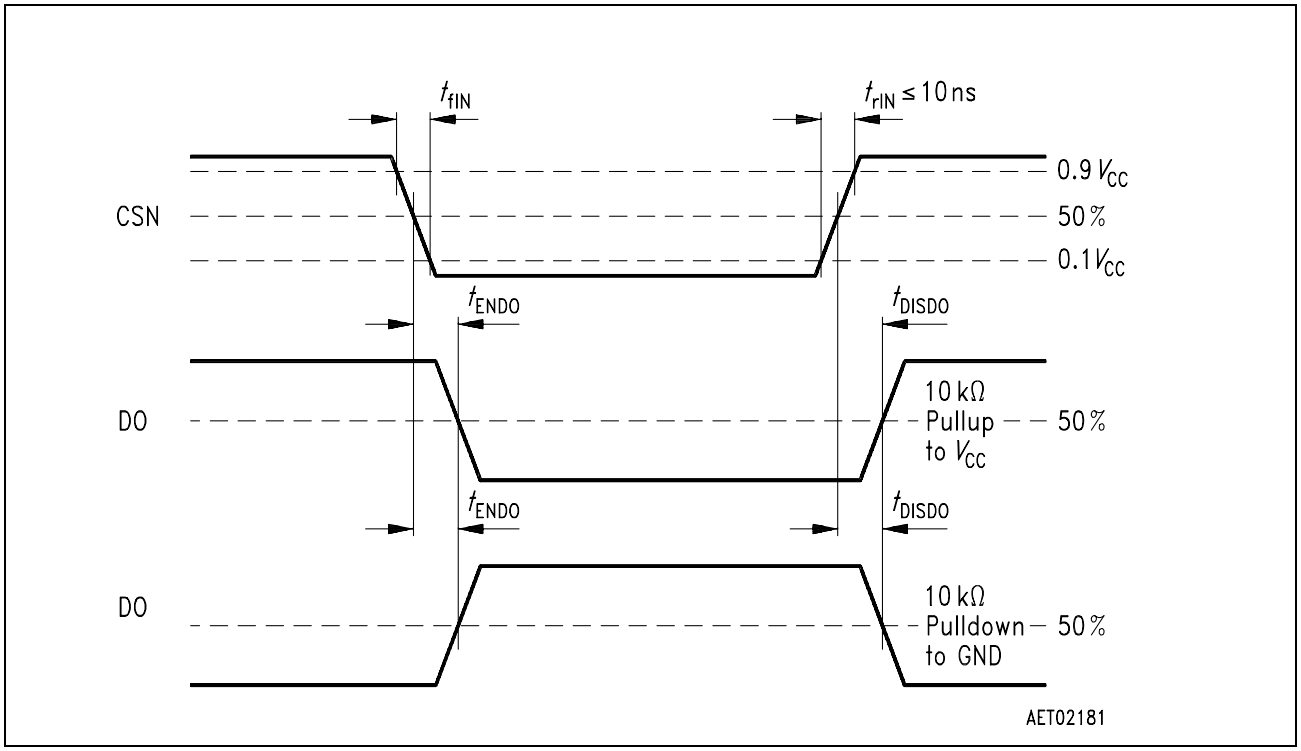


Figure 12 DO Enable and Disable Time (CSN = $\overline{CS}$)

4 Characteristics

4.1 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Test Condition
			Min.	Max.		
	Supply Voltage Input IN					
	Voltage	V_{VS}	-0.5	60	V	–
	Current	I_{VS}	–	–	–	
	Buck-Switch Output SW					
	Voltage	V_{SW}	-2	V_S+0.5	V	–
	Current	I_{SW}	–	–	–	
	Feedback and Linear Voltage Regulator Input					
	Voltage	V_{FB/L_IN}	-0.5	8	V	–
	Current	I_{FB/L_IN}	–	–	–	
	Bootstrap Connector Bootstrap					
	Voltage	$V_{Bootstrap}$	V_{SW}-0.5V	V_{SW}+8V	V	
	Voltage	$V_{Bootstrap}$	-0.5	66	V	
	Current	$I_{Bootstrap}$	–	–	–	Internally Limited
	Boost Input					
	Voltage	V_{Boost}	-0.5	60	V	–
	Current	I_{Boost}		TBD	A	
	Slope Control Input Slew					
	Voltage	V_{Slew}	-0.5	6	V	–
	Current	I_{Slew}	–	–	–	Internally Limited
	Charge Pump Capacitor Connector C-					
	Voltage	V_{CL}	-0.5	V_{FB/L_IN} +0.5	V	
	Current	I_{CL}	–	–	–	
	Charge Pump Capacitor Connector C+					
	Voltage	V_{CH}	-0.5	14	V	

	Current	I_{CH}	-150		mA	
	Charge Pump Storage Capacitor CCP					
	Voltage	V_{CCP}	-0.5	14	V	
	Current	I_{CCP}		150	mA	
	Standby Voltage Regulator output Q_STB					
	Voltage	V_{Q_Stb}	-0.5	6	V	–
	Current	I_{Q_Stb}	–	–	–	Internally limited
	Voltage Regulator output voltage Q_LDO1					
	Voltage	V_{Q_LDO1}	-0.5	6	V	–
	Current	I_{Q_LDO1}	–	–	–	Internally limited
	Voltage Regulator output voltage Q_LDO2					
	Voltage	V_{Q_LDO2}	-0.5	6	V	–
	Current	I_{Q_LDO2}	–	–	–	Internally limited
	Voltage Regulator output voltage Q_LDO3					
	Voltage	V_{Q_LDO3}	-0.5	6	V	–
	Current	I_{Q_LDO3}	–	–	–	Internally limited
	Voltage Tracker output voltage Q_T1					
	Voltage	V_{Q_T1}	-4	40	V	–
	Current	I_{Q_T1}	-10	–	mA	Internally limited
	Voltage Tracker output voltage Q_T2					
	Voltage	V_{Q_T2}	-4	40	V	–
	Current	I_{Q_T2}	-10	–	mA	Internally limited
	Voltage Tracker output voltage Q_T3					
	Voltage	V_{Q_T3}	-4	40	V	–
	Current	I_{Q_T3}	-10	–	mA	Internally limited
	Voltage Tracker output voltage Q_T4					
	Voltage	V_{Q_T4}	-4	40	V	–
	Current	I_{Q_T4}	-10	–	mA	Internally limited
	Voltage Tracker output voltage Q_T5					
	Voltage	V_{Q_T5}	-4	40	V	–

	Current	I_{Q_T5}	-10	–	mA	Internally limited
	Voltage Tracker output voltage Q_T6					
	Voltage	V_{Q_T6}	-4	40	V	–
	Current	I_{Q_T6}	-10	–	mA	Internally limited
	Select Input SEL					
	Voltage	V_{SEL}	-0.5	6	V	–
	Current	I_{SEL}	–	–	–	Internally limited
	Wake Up Input Wake					
	Voltage	V_{Wake}	-0.5	60	V	–
	Current	I_{Wake}	–	–	–	
	Reset Output R1					
	Voltage	V_{R1}	-0.5	6	V	–
	Current	I_{R1}	–	–	–	
	Reset Output R2					
	Voltage	V_{R2}	-0.5	6	V	–
	Current	I_{R2}	–	–	–	
	Reset Output R3					
	Voltage	V_{R3}	-0.5	6	V	–
	Current	I_{R3}	–	–	–	
	SPI Data Input DI					
	Voltage	V_{DI}	-0.5	6	V	–
	Current	I_{DI}	–	–	–	Internally limited
	SPI Data Output DO					
	Voltage	V_{DO}	-0.5	6	V	–
	Current	I_{DO}	–	–	–	
	SPI Clock Input CLK					
	Voltage	V_{CLK}	-0.5	6	V	–
	Current	I_{CLK}	–	–	–	Internally limited
	SPI Chip Select Not Input $\overline{CS}$					
	Voltage	$V_{\overline{CS}}$	-0.5	6	V	–

	Current	$I_{\overline{CS}}$	–	–	–	Internally limited
	Error Output Pin					
	Voltage	V_{Error}	-0.5	6	V	–
	Current	I_{Error}	–	–	–	
	Thermal Resistance					
	Junction-ambient	R_{thja}		TBD	K/W	
	Junction-case	R_{thjc}	–	5	K/W	
	Temperature					
	Junction temperature	T_j	-40	150	°C	
	Junction temp. transient	T_{jt}		175	°C	lifetime=TBD
	Storage temperature	T_{stg}	-50	150	°C	
	ESD					
	ESD	V_{ESD}	-2	2	kV	HBM-Model

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Note: ESD Protection according to ANSI EOS/ESD-S5.1-1993 ESD STM5.1-1998 .

4.2 Functional Range

-40°C < T_j < 150 °C

Item	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
	Supply Voltage	V_{IN}	5.5	60	V	
	T_j		-40	150	°C	
	Ripple at FB/L_IN	$V_{FB/L\_IN\ ripple}$	0	150	mV_{PP}	

Note: Within the operational range the IC operates as described in the functional description. The electrical characteristics, however, are not guaranteed.

4.3 Recommended Operation Range

-40°C < T_j < 150 °C

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Buck Inductor	L_B	18		100	µH	
	Buck Capacitor	C_B	4.7	22		µF	ESR <0.15 Ω, ceramic capacitor (X7R)
	Bootstrap Capacitor	C_{BTP}		2		% of C_B	
	SLEW resistor	R_{SLEW}	0		20	kΩ	

4.4 Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply volt-age and ambient temperature range. Typical values represent the median values, which are related to production processes.

$-40 < T_j < 150$ °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
	Buck regulator						
4.4.1	Switching frequency	f_{SW}	250	330	410	kHz	
4.4.2	Current rise time	$t_{r\_I\_SW}$	40		80	ns	R_{SL}=5kΩ
4.4.3	Current fall time	$t_{f\_I\_SW}$	40		80	ns	R_{SL}=5kΩ
4.4.4	Voltage rise / fall time	$t_{f\_V\_SW}$		70		ns	
4.4.5	Static on resistance	R_{ON}		150		mΩ	T_j=25°C in static operation
4.4.6	Static on resistance	R_{ON}		300	400	mΩ	T_j=150°C in static operation
4.4.7	Current limit	I_{MAX}	1.5		2.4	A	
4.4.8	Output voltage	V_{OUT}	5.4		5.7	V	I_{OUT}=1.5A V_{IN}=13.5 V
4.4.9	Output voltage	V_{OUT}	5.9		6.3	V	I_{OUT}=0.1A V_{IN}=13.5 V
4.4.10	Charge pump voltage	V_{CCP}	8		11	V	I_{Q_LDO1} = 800mA, C_{FLY}=100nF, C_{CCP}=220nF
4.4.11	Max. Duty Cycle	$duty_{max}$		95		%	Switching operation
4.4.12	Min. Duty Cycle	$duty_{min}$			0	%	

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
	Voltage Regulator Q_LDO1, Version 1 & 2						
4.4.13	Output voltage	V_{Q1}	4.9	5.0	5.1	V	100mA< I_{Q_LDO1} <800mA
4.4.14	Load Regulation	ΔV_{Q_LDO1}		25		mV	100mA< I_{Q_LDO1} <800mA; V_{FB/L_IN}=5,5V
4.4.15	Current limit	$I_{Q\_LDO1limit}$	800		1400	mA	V_{Q_LDO1}=4V
4.4.16	Ripple rejection	PSRR1	26	40		dB	f=400kHz
4.4.17	Output Capacitor	C_{Q_LDO1}	100			nF	
	Voltage Regulator Q_LDO2, Version 1 & 2						
4.4.18	Output voltage 3.3V	V_{Q_LDO2}	3.14	3.3	3.46	V	50mA< I_{Q_LDO2} <500mA; 3.3V mode
4.4.19	Output voltage 2.6V	V_{Q_LDO2}	2.500	2.625	2.750	V	50mA< I_{Q_LDO2} <500mA; 2.6V mode
4.4.20	Load Regulation	ΔV_{Q_LDO2}		25		mV	50mA< I_{Q_LDO3} <500mA; V_{FB/L_IN}=5,5V 3.3V mode
4.4.21	Load Regulation	ΔV_{Q_LDO2}		25		mV	50mA< I_{Q_LDO2} <500mA; V_{FB/L_IN}=5,5V 2.6V mode
4.4.22	Current limit	$I_{Q\_LDO2limit}$	400		700	mA	V_{Q_LDO2}= 2.8V; 3.3V mode
4.4.23	Current limit	$I_{Q\_LDO2limit}$	400		700	mA	V_{Q_LDO2}= 2V; 2.6V mode
4.4.24	Ripple rejection	PSRR2	26	40		dB	f=400kHz
4.4.25	Output Capacitor	C_{Q_LDO2}	100			nF	

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
	Voltage Regulator Q_LDO3, Version 1						
4.4.26	Output voltage 5V	V_{Q_LDO3}	4.9	5.0	5.1	V	20mA< I_{Q_LDO3} <300mA; 5V mode
4.4.27	Output voltage 3.3V	V_{Q_LDO3}	3.14	3.30	3.46	V	20mA< I_{Q_LDO3} <300mA; 3.3V mode
4.4.28	Load Regulation	ΔV_{Q_LDO3}		25		mV	20mA< I_{Q_LDO3} <300mA; V_{FB/L_IN}=5,5V 5V mode
4.4.29	Load Regulation	ΔV_{Q_LDO3}		25		mV	20mA< I_{Q_LDO3} <300mA; V_{FB/L_IN}=5,5V 3.3V mode
4.4.30	Current limit	$I_{Q\_LDO3\ limit}$	300		500	mA	V_{Q_LDO3}=4V; 5V mode
4.4.31	Current limit	$I_{Q\_LDO3\ limit}$	300		500	mA	V_{Q_LDO3}=2.8V; 3.3V mode
4.4.32	Ripple rejection	PSSR3	26	40		dB	f=400kHz
4.4.33	Output Capacitor	C_{Q_LDO3}	100			nF	
	Voltage Regulator Q_LDO3, Version 2						
4.4.34	Output voltage 3.1V	V_{Q_LDO3}	3.00	3.15	3.30	V	20mA< I_{Q_LDO3} <300mA; 3.1V mode
4.4.35	Output voltage 2.6V	V_{Q_LDO3}	2.500	2.625	2.750	V	20mA< I_{Q_LDO3} <300mA; 2.6V mode
4.4.36	Load Regulation	ΔV_{Q_LDO3}		25		mV	20mA< I_{Q_LDO3} <300mA; V_{FB/L_IN}=5,5V 3.1V mode

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.37	Load Regulation	ΔV_{Q_LDO3}		25		mV	20mA< I_{Q_LDO3} <300mA; V_{FB/L_IN}=5,5V 2.6V mode
4.4.38	Current limit	$I_{Q\_LDO3\ limit}$	300		500	mA	V_{Q_LDO3}=4V; 3.1V mode
4.4.39	Current limit	$I_{Q\_LDO3\ limit}$	300		500	mA	V_{Q_LDO3}=2.8V; 2.6V mode
4.4.40	Ripple rejection	PSSR3	26	40		dB	f=400kHz
4.4.41	Output Capacitor	C_{Q_LDO3}	100			nF	
	Voltage Tracker Q_T1						
4.4.42	Output voltage tracking accuracy	ΔV_{Q_T1}	-15		5	mV	V_{Q_T1}-V_{Q_LDO1}; 1mA<I_{Q_T1}<15mA
4.4.43	Overvoltage threshold	V_{OVQ_T1}		V_{Q_T1}+ 100mV		mV	
4.4.44	Undervoltage threshold	V_{UVQ_T1}		V_{Q_T1}- 200mV		mV	
4.4.45	Current limit	$I_{Q\_T1\ limit}$	20		30	mA	V_{Q_T1}=4V
4.4.46	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.47	Tracker load capacitor	C_{Q_T1}	1			µF	
	Voltage Tracker Q_T2						
4.4.48	Output voltage tracking accuracy	ΔV_{Q_T2}	-15		5	mV	V_{Q_T2}-V_{Q_LDO1}; 1mA<I_{Q_T2}<15mA
4.4.49	Overvoltage threshold	V_{OVQ_T2}		V_{Q_T2}+ 100mV		mV	

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.50	Undervoltage threshold	V_{UVQ_T2}		V_{Q_T2}-200mV		mV	
4.4.51	Current limit	$I_{Q\_T2\ limit}$	20		30	mA	V_{Q_T2}=4V
4.4.52	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.53	Tracker load capacitor	C_{Q_T2}	1			µF	
	Voltage Tracker Q_T3						
4.4.54	Output voltage tracking accuracy	ΔV_{Q_T3}	-15		5	mV	V_{Q_T3}-V_{Q_LDO1}; 1mA<I_{Q_T3}<15mA
4.4.55	Overvoltage threshold	V_{OVQ_T3}		V_{Q_T3}+100mV		mV	
4.4.56	Undervoltage threshold	V_{UVQ_T3}		V_{Q_T3}-200mV		mV	
4.4.57	Current limit	$I_{Q\_T3\ limit}$	20		30	mA	V_{Q_T3}=4V
4.4.58	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.59	Tracker load capacitor	C_{Q_T3}	1			µF	
	Voltage Tracker Q_T4						
4.4.60	Output voltage tracking accuracy	ΔV_{Q_T4}	-15		5	mV	V_{Q_T4}-V_{Q_LDO1}; 1mA<I_{Q_T4}<15mA
4.4.61	Overvoltage threshold	V_{OVQ_T4}		V_{Q_T4}+100mV		mV	
4.4.62	Undervoltage threshold	V_{UVQ_T4}		V_{Q_T4}-200mV		mV	

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.63	Current limit	$I_{Q\_T4\ limit}$	20		30	mA	V_{Q_T4}=4V
4.4.64	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.65	Tracker load capacitor	C_{Q_T4}	1			µF	
	Voltage Tracker Q_T5						
4.4.66	Output voltage tracking accuracy	ΔV_{Q_T5}	-15		5	mV	V_{Q_T5}-V_{Q_LDO1}; 1mA<I_{Q_T5}<15mA
4.4.67	Overvoltage threshold	V_{OVQ_T5}		V_{Q_T5}+ 100mV		mV	
4.4.68	Undervoltage threshold	V_{UVQ_T5}		V_{Q_T5}- 200mV		mV	
4.4.69	Current limit	$I_{Q\_T5\ limit}$	20		30	mA	V_{Q_T5}=4V
4.4.70	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.71	Tracker load capacitor	C_{Q_T5}	1			µF	
	Voltage Tracker Q_T6						
4.4.72	Output voltage tracking accuracy	ΔV_{Q_T6}	-15		5	mV	V_{Q_T6}-V_{Q_LDO1}; 1mA<I_{Q_T6}<15mA
4.4.73	Overvoltage threshold	V_{OVQ_T6}		V_{Q_T6}+ 100mV		mV	
4.4.74	Undervoltage threshold	V_{UVQ_T6}		V_{Q_T6}- 200mV		mV	
4.4.75	Current limit	$I_{Q\_T6\ limit}$	20		30	mA	V_{Q_T6}=4V
4.4.76	Ripple rejection	PSSR	26			dB	f=400kHz
4.4.77	Tracker load capacitor	C_{Q_T6}	1			µF	

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
	Standby Regulator						
4.4.78	Output voltage	V_{Q_STB}		2.5		V	0µA <I_{Q_STB}<500µA
4.4.79	Current limit	$I_{Q\_STB\ limit}$	1	3	6	mA	V_{Q_STB}=2V
4.4.80	Standby load capacitor	C_{Q_STB}	0.1			µF	
	Off-Mode						
4.4.81	Supply current from battery	$I_{q,off}$			50	µA	V_{IN}=13.5 V, V_{wake}=0 V, I_{Q_STB}=0µA T_j < 85°C
4.4.82	Supply current from battery	$I_{q,off}$		20	100	µA	V_{IN}=13.5V, V_{wake}=0 I_{Q_STB}=0µA
4.4.83	Supply current from battery	$I_{q,off}$			50	µA	V_{IN}=42 V, V_{wake}=0 V, I_{Q_STB}=0µA T_j < 85°C
4.4.84	Supply current from battery	$I_{q,off}$		30	100	µA	V_{IN}=42V, V_{wake}=0 I_{Q_STB}=0µA
4.4.85	Wake-up threshold	$V_{wake\ th}$	1.8		2.8	V	
4.4.86	Wake-up input current	I_{wake}		100		µA	V_{wake}=5V
4.4.87	Wake up input on time	$t_{wake,min}$	4	10	50	µs	V_{wake} > $V_{wake\ th}$
	Reset						
4.4.88	Reset output low voltage	$V_{R1\ L}$			0.4	V	I_{R1}=1.6mA; V_{Q_LDO1} =5V

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.89	Reset output low voltage	$V_{R1\ L}$			0.3	V	I_{R1}=0.3mA; V_{Q_LDO1} =1V
4.4.90	Reset High voltage	$V_{R1\ H}$	0.7*V_{Q_LDO1}				
4.4.91	Reset output low voltage	$V_{R2\ L}$			0.4	V	I_{R2}=1.6mA; V_{Q_LDO1} =2.5V
4.4.92	Reset output low voltage	$V_{R2\ L}$			0.3	V	I_{R2}=0.3mA; V_{Q_LDO2} =1V
4.4.93	Reset High voltage	$V_{R2\ H}$	0.7*V_{Q_LDO2}				
4.4.94	Reset output low voltage	$V_{R3\ L}$			0.4	V	I_{R3}=1.6mA; V_{Q_LDO1} =3.3V
4.4.95	Reset output low voltage	$V_{R3\ L}$			0.3	V	I_{R3}=0.3mA; V_{Q_LDO3} =1V
4.4.96	Reset High voltage	$V_{R3\ H}$	0.7*V_{Q_LDO3}				
4.4.97	Reset threshold Q_LDO1, V_LDO1 decreasing	$V_{RTH\ Q\_LDO1}$	4.5	4.65	4.8	V	
4.4.98	Power good threshold Q_LDO1, V_LDO1 increasing	$V_{RTH\ Q\_LDO1}$	4.6	4.75	4.9	V	
4.4.99	Reset threshold Q_LDO2	$V_{RTH\ Q\_LDO2}$		85		% of V_{Q_LDO2}	3.3V mode
4.4.100	Reset threshold Q_LDO2	$V_{RTH\ Q\_LDO2}$	2.3			V	2.6V mode

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.101	Reset threshold Q_LDO3	$V_{RTH\ Q\_LDO3}$		85		%of V_{Q_LDO3}	Version 1, 5V mode
4.4.102	Reset threshold Q_LDO3	$V_{RTH\ Q\_LDO3}$	2.7			V	Version 1, 3.3V mode
4.4.103	Reset threshold Q_LDO3	$V_{RTH\ Q\_LDO3}$	2.7			V	Version 2, 3.1V mode
4.4.104	Reset threshold Q_LDO3	$V_{RTH\ Q\_LDO3}$	2.3			V	Version 2, 2.6V mode
4.4.105	Reset reaction time	t_{rr}	1	2	10	µs	
4.4.106	Reset Delay Norm factor	$t_{NORM,RES}$	0.75	1	1.25		
	RAM Good						
4.4.107	V_{Q1} threshold	$V_{Th\ Q1}$	2.3	2.5	2.7	V	
4.4.108	V_{Q2} threshold	$V_{Th\ Q2}$		1.5		V	3.3V mode
4.4.109	V_{Q2} threshold	$V_{Th\ Q2}$		1.5		V	2.6V mode
	Window Watchdog						
4.4.110	Closed window time tolerance	t_{CW_tol}	0.75	1	1.25		
4.4.111	Open window time tolerance	t_{OW_tol}	0.75	1	1.25		
4.4.112	Watchdog reset low time	t_{WRL}		t_{RES}			

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.113	Watchdog reset delay time	t_{SR}		t_{CW}/2			
	SPI						
4.4.114	SPI clock frequency	f_{CLK}	0		2.5	MHz	
	SPI Input DI						
4.4.115	H-input voltage threshold	V_{IH}	–	–	0.7 * V_{Q_LDO1}	V	–
4.4.116	L-input voltage threshold	V_{IL}	0.2 * V_{Q_LDO1}	–	–	V	–
4.4.117	Hysteresis of input voltage	V_{IHY}	50	200	500	mV	guaranteed by design
4.4.118	Pull down current	I_I	5	25	100	µA	V_{DI} = 0.2 * V_{Q_LDO1}
4.4.119	Input capacitance	C_I	–	10	15	pF	0 V < V_{Q_LDO1} < 5.25 V
4.4.120	Input signal rise time	t_r	–	–	tbd	ns	
4.4.121	Input signal fall time	t_f	–	–	tbd	ns	
	SPI Clock Input CLK						
4.4.122	H-input voltage threshold	V_{IH}	–	–	0.7 * V_{Q_LDO1}	V	–
4.4.123	L-input voltage threshold	V_{IL}	0.2 * V_{Q_LDO1}	–	–	V	–
4.4.124	Hysteresis of input voltage	V_{IHY}	50	200	500	mV	guaranteed by design

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.125	Pull down current	I_I	5	25	100	µA	V_{CLK} = 0.2 * V_{Q_LDO1}
4.4.126	Input capacitance	C_I	–	10	15	pF	0 V < V_{Q_LDO1} < 5.25 V
4.4.127	Input signal rise time	t_r	–	–	tbd	ns	
4.4.128	Input signal fall time	t_f	–	–	tbd	ns	
	SPI Chip Select Input $\overline{CS}$						
4.4.129	H-input voltage threshold	V_{IH}	–	–	0.7 * V_{Q_LDO1}	V	–
4.4.130	L-input voltage threshold	V_{IL}	0.2 * V_{Q_LDO1}	–	–	V	–
4.4.131	Hysteresis of input voltage	V_{IHY}	50	200	500	mV	guaranteed by design
4.4.132	Pull up current at pin $\overline{CS}$	$I_{I,\overline{CS}}$	– 100	– 25	– 5	µA	$V_{\overline{CS}}$ = 0.7 * V_{Q_LDO1}
4.4.133	Input capacitance	C_I	–	10	15	pF	0 V < V_{Q_LDO1} < 5.25 V
4.4.134	Input signal rise time	t_r	–	–	tbd	ns	
4.4.135	Input signal fall time	t_f	–	–	tbd	ns	
	Logic Output DO						
4.4.136	H-output voltage level	V_{DOH}	V_{CC1} – 1.0	V_{CC1} – 0.7	–	V	I_{DOH} = 1 mA
4.4.137	L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

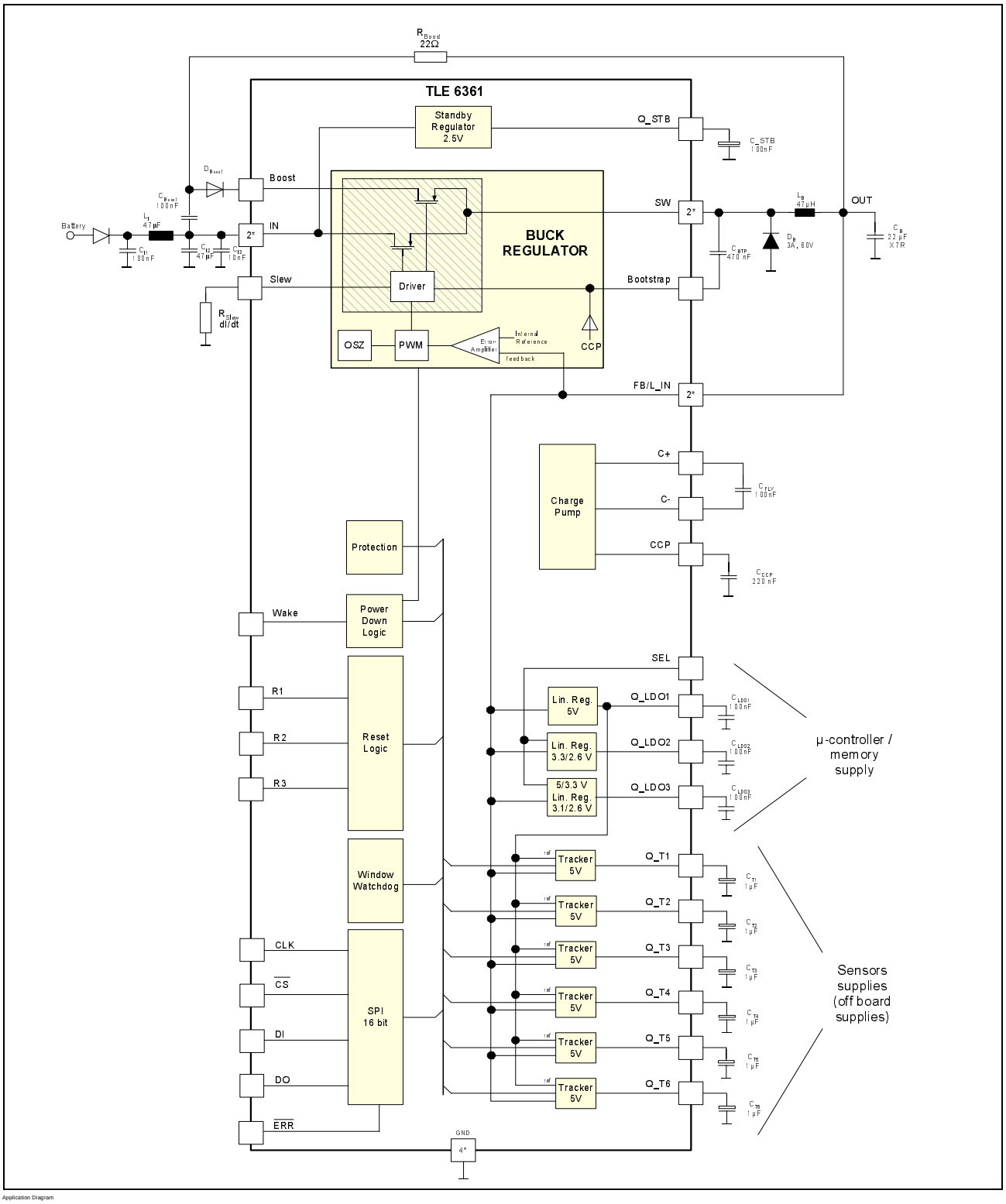
Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.138	Tri-state leakage current	I_{DO_TRI}	– 10	–	10	µA	$V_{\overline{CS}} = V_{Q\_LDO1}$; 0 V < V_{DO} < V_{Q_LDO1}
4.4.139	Tri-state input capacitance	C_{DO}	–	10	15	pF	$V_{\overline{CS}} = V_{Q\_LDO1}$ 0 V < V_{Q_LDO1} < 5.25 V
	Data Input Timing						
4.4.140	Clock period	t_{pCLK}	tbd	–	–	ns	–
4.4.141	Clock high time	t_{CLKH}	tbd	–	–	ns	–
4.4.142	Clock low time	t_{CLKL}	tbd	–	–	ns	–
4.4.143	Clock low before $\overline{CS}$ low	t_{bef}	tbd	–	–	ns	–
4.4.144	$\overline{CS}$ setup time	t_{lead}	tbd	–	–	ns	
4.4.145	CLK setup time	t_{lag}	tbd	–	–	ns	
4.4.146	Clock low after $\overline{CS}$ high	t_{beh}	tbd	–	–	ns	
4.4.147	DI setup time	t_{DISU}	tbd	–	–	ns	
4.4.148	DI hold time	t_{DIHO}	tbd	–	–	ns	
	Data Output Timing						
4.4.149	DO rise time	t_{rDO}	–	tbd	tbd	ns	C_L = 100 pF
4.4.150	DO fall time	t_{fDO}	–	tbd	tbd	ns	C_L = 100 pF
4.4.151	DO enable time	t_{ENDO}	–	–	tbd	ns	low impedance
4.4.152	DO disable time	t_{DISDO}	–	–	tbd	ns	high impedance

-40 < T_j <150 °C; V_{IN}=13.5V unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Measuring Conditions
			min.	typ.	max.		
4.4.153	DO valid time	t_{VADO}	–	tbd	tbd	ns	V_{DO} < 0.1 V_{Q_LDO1}; V_{DO} > 0.9 V_{Q_LDO1}; C_L = 100 pF
	General						
4.4.154	Temperature warning flag	$T_{J,Flag}$		150		°C	
4.4.155	Over Temperature shutdown	$T_{J,Shutdown}$	150	170	200	°C	
4.4.156	Over-Temperature shutdown Hysteresis	ΔT_{sd_hys}		30		°C	
4.4.157	Ratio TW to TSD	$T_{J,Shutdown}$ /$T_{J,Flag}$		1.13			

5 Application Information

5.1 Application Diagram



Application Diagram

Figure 13 Application Diagram

5.2 Application Recommendations

5.2.1 Recommended Components

Device	Type	Supplier	Remark
L_I	DO5022P-473	Coilcraft	47µH, 4.0A, 97mΩ
	DO5022P-223	Coilcraft	22µH, 6.0A, 59mΩ
	8532-17L	API Delevan	22µH, 2.6A, 50mΩ
	2474-17L	API Delevan	22µH, 2.6A, 50mΩ
C_{I1}	Ceramic	various	100nF, 60V
C_{I2}	Electrolyt or low ESR tantalum	various	47µF, 60V
C_{I3}	Ceramic	various	10nF, 60V
D_{Boost}			
L_B	DO5022P-473	Coilcraft	47µH, 4.0A, 97mΩ
	DO5022P-223	Coilcraft	22µH, 6.0A, 59mΩ
	8532-17L	API Delevan	22µH, 2.6A, 50mΩ
	2474-17L	API Delevan	22µH, 2.6A, 50mΩ
C_{BTP}	Ceramic	various	100nF, 10V
D_B	MBRD360	Motorola	Schottky, 60V, 3A
	SS34	various	Schottky, 40V, 3A
C_B	LMK316BJ475ML	Taiyo Yuden	Creamic X7R, 4.7µF, 10V
	TPSC476K010R350	AVX	Low ESR Tantalum, 47µF, 10V, C-case
	B45197-A2226	EPCOS	Low ESR Tantalum, 22µF, 10V, C-case

5.2.2 Input Filter for reduced EME

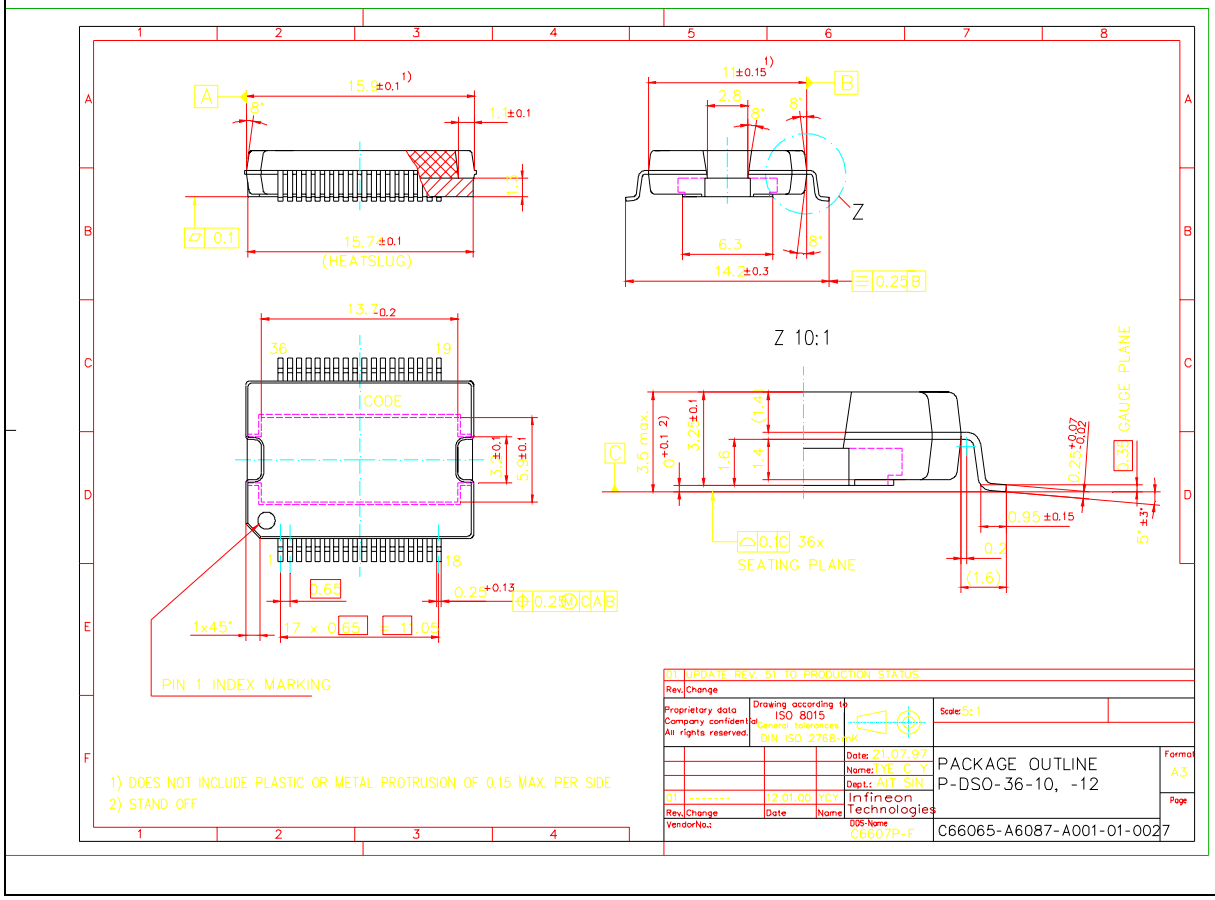
Most of the EME generated by the buck regulator is caused by the transitions of the load current flowing through the buck inductance. The current flows from the input line through the power switch to the inductor when the switch is on and recirculates through the external catch diode when the switch is off. The input bypass capacitor and the catch diode must be placed as close as possible to the IC to avoid high frequency EME through stray inductance. To limit the bandwidth of the switching transients the current slope can be set by an external resistor within 20ns to 80ns transition time.

5.2.3 Tracker outputs

Voltage Tracker outputs should bypass with a 1uF electrolytic capacitor with ESR for stability, an additional ceramic capacitor is recommended for improved EMI. Keep open, if not needed.

6 Package Outlines

P-DSO-36-12
(Plastic Transistor Outline)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

Edition 9.99

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