- **Provides Two-Chip Modem Solution**
- **Data Rates from 300 bps to 56 kbps**
- **Data Modulation Standards V.90, V.34, V.32bis, V.32, V.22bis, V.22, V.23, V.21 and V.23 reversible (Minitel), Bell 212, Bell 103**
- **V.42 Error Control and V.42bis Compression**
- **Caller ID**
- **Field-Proven Modem Algorithms Give Highest Performance, Reliability, and Compatibility**
- **Worldwide Telecom Approvals**
- **Protected Against Surge and Overvoltage on the Telephone Line**
- **Parallel Host Port Interface Supports a Variety of Industry Standard Busses**
- **Integral Serial Interface (UART)**
- **State-of-the-Art Integrated Transformerless Silicon DAA for Phone Line Interconnection**
- **Applications**
  - **Embedded Systems**
  - **Set Top Box**
  - **Gaming Consoles**
  - **Internet Appliances**
  - **Portable Devices (PDAs, digital cameras)**
  - **Remote Data Collection, Point-of-Sale**
  - **Meter Reading, Utility Monitoring**
- **40K x 16-Bit Dual-Access On-Chip RAM**
- **128K x 16-Bit On-Chip ROM**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank Switching**
  - **On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Enhanced 8-Bit Parallel Host-Port Interface (HPI8)**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **8.5-ns Single-Cycle Fixed-Point Instruction Execution Time (117.96 MIPS) for 3.3-V Power Supply (1.5-V Core)**
- **Available in a 144-Pin Plastic Low-Profile Quad Flatpack (LQFP) (PGE Suffix) and a 144-Pin Ball Grid Array (BGA) (GGU Suffix)**

ADVANCE INFORMATION

description

The TMS320C54V90 is used to implement a full-featured, high-performance modem technology, intended for use in embedded systems and similar applications. This highly integrated solution implements a complete modem using only two chips: the TMS320C54V90 DSP with on-chip RAM and ROM, and the PCT308W line-side DAA available from PCTEL, Inc.

The modem can connect to a host system serially (RS-232 functionality), or as an 8-bit peripheral to the processor in a host system. The TMS320C54V90 uses a standard Digital Signal Processor (DSP) and proprietary firmware to perform all the modem signal processing, the V.42/V.42bis compression, and AT commands interpretation for modem control functions.

The TMS320C54V90 also uses the latest silicon DAA technology. This technology does not require a transformer and results in lower cost, lower power, and a smaller area for the DAA function.

For serial interface applications, an integrated UART implements the serial interface with no additional hardware.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

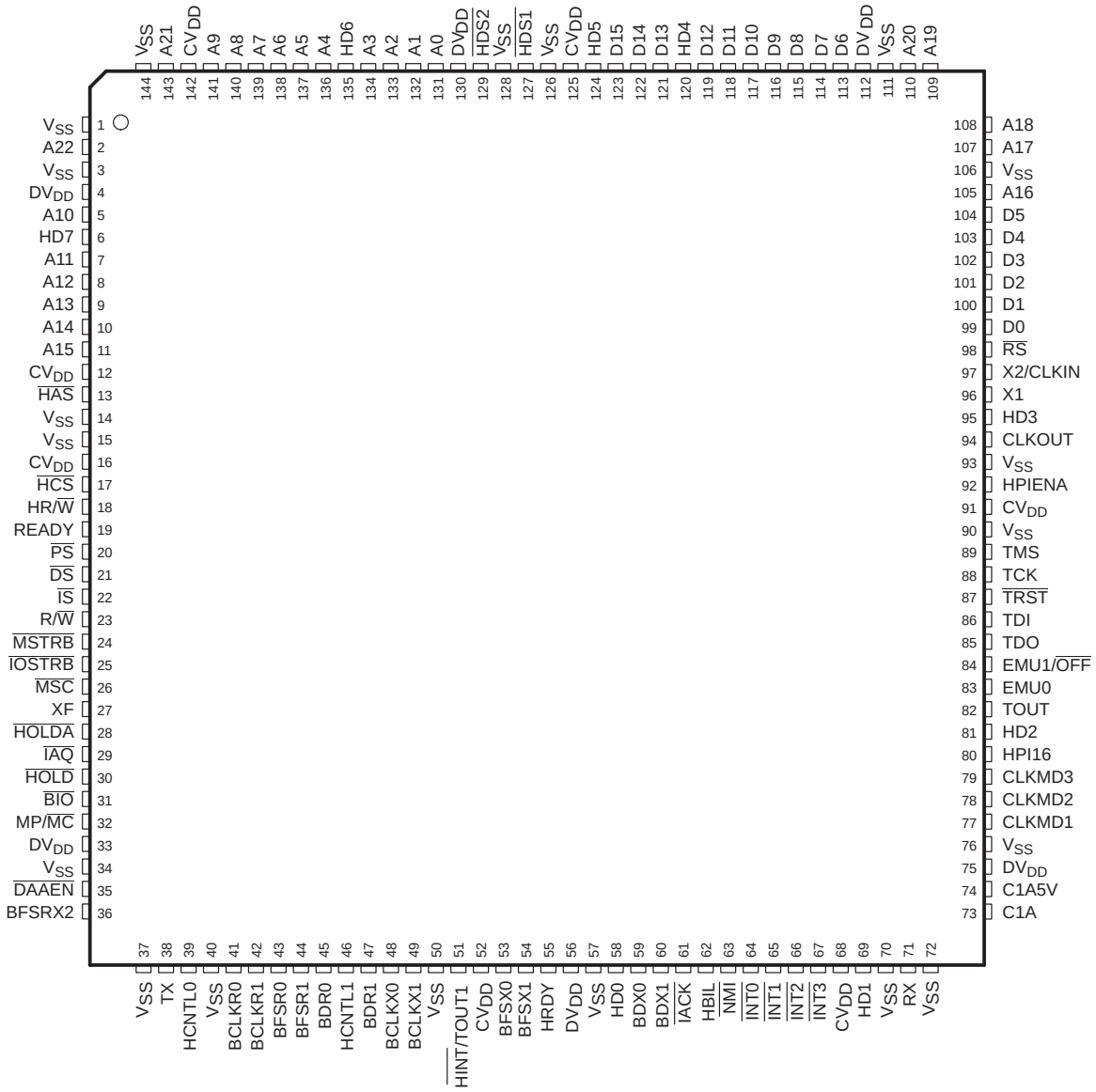
TABLE OF CONTENTS

REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
*	July 2001	Advanced Information	Original

ADVANCE INFORMATION

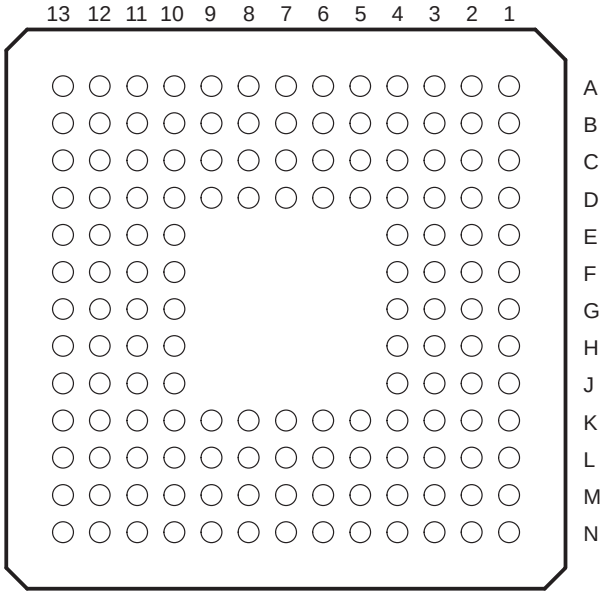
PGE PACKAGE†
(TOP VIEW)



† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

ADVANCE INFORMATION

GGU PACKAGE
(BOTTOM VIEW)



The pin assignments table to follow lists each signal name and BGA ball number for the TMS320C54V90 (144-pin BGA) package which is footprint compatible with the TMS320VC5402.

Pin Assignments for the TMS320C54V90GGU (144-Pin BGA) Package†

SIGNAL QUADRANT 1	BGA BALL #	SIGNAL QUADRANT 2	BGA BALL #	SIGNAL QUADRANT 3	BGA BALL #	SIGNAL QUADRANT 4	BGA BALL #
V_{SS}	A1	C1A	N13	V_{SS}	N1	A19	A13
A22	B1	C1A5V	M13	TX	N2	A20	A12
V_{SS}	C2	DV_{DD}	L12	HCNTL0	M3	V_{SS}	B11
DV_{DD}	C1	V_{SS}	L13	V_{SS}	N3	DV_{DD}	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	BCLKR1	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	HPI16	K13	BFSR1	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	BDR1	M5	D12	B9
CV_{DD}	E1	EMU1/$\overline{OFF}$	J13	BCLKX0	N5	HD4	A9
$\overline{HAS}$	F4	TDO	H10	BCLKX1	K6	D13	D8
V_{SS}	F3	TDI	H11	V_{SS}	L6	D14	C8
V_{SS}	F2	$\overline{TRST}$	H12	$\overline{HINT}$/TOUT1	M6	D15	B8
CV_{DD}	F1	TCK	H13	CVDD	N6	HD5	A8
$\overline{HCS}$	G2	TMS	G12	BFSX0	M7	CV_{DD}	B7
HR/$\overline{W}$	G1	V_{SS}	G13	BFSX1	N7	V_{SS}	A7
READY	G3	CV_{DD}	G11	HRDY	L7	$\overline{HDS1}$	C7
$\overline{PS}$	G4	HPIENA	G10	DV_{DD}	K7	V_{SS}	D7
$\overline{DS}$	H1	V_{SS}	F13	V_{SS}	N8	$\overline{HDS2}$	A6
$\overline{IS}$	H2	CLKOUT	F12	HD0	M8	DV_{DD}	B6
R/$\overline{W}$	H3	HD3	F11	BDX0	L8	A0	C6
$\overline{MSTRB}$	H4	X1	F10	BDX1	K8	A1	D6
$\overline{IOSTRB}$	J1	X2/CLKIN	E13	$\overline{IACK}$	N9	A2	A5
$\overline{MSC}$	J2	$\overline{RS}$	E12	HBIL	M9	A3	B5
XF	J3	D0	E11	$\overline{NMI}$	L9	HD6	C5
$\overline{HOLDA}$	J4	D1	E10	$\overline{INT0}$	K9	A4	D5
$\overline{IAQ}$	K1	D2	D13	$\overline{INT1}$	N10	A5	A4
$\overline{HOLD}$	K2	D3	D12	$\overline{INT2}$	M10	A6	B4
$\overline{BIO}$	K3	D4	D11	$\overline{INT3}$	L10	A7	C4
MP/$\overline{MC}$	L1	D5	C13	CV_{DD}	N11	A8	A3
DV_{DD}	L2	A16	C12	HD1	M11	A9	B3
V_{SS}	L3	V_{SS}	C11	V_{SS}	L11	CV_{DD}	C3
$\overline{DAAEN}$	M1	A17	B13	RX	N12	A21	A2
BFSRX2	M2	A18	B12	V_{SS}	M12	V_{SS}	B2

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

ADVANCE INFORMATION

Table 1. TMS320C54V90 Pin Functions

TERMINAL NAME	I/O†	DESCRIPTION
EXTERNAL MEMORY INTERFACE PINS		
A22 (MSB) A21 A20 A19 A18 A17 A16	O/Z	Parallel address bus A22 (MSB) through A0 (LSB). The lower sixteen address pins—A0 to A15—are multiplexed to address all external memory (program, data) or I/O, while the upper seven address pins—A22 to A16—are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when OFF is low.
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)		A15 (MSB), A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0 (LSB) — I: These pins can be used to address internal memory via the HPI when the HPI16 pin is high.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	D15 (MSB), D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0 (LSB) — I/O: Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when RS or HOLD is asserted. The data bus also goes into the high-impedance state when OFF is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
INITIALIZATION, INTERRUPT, AND RESET PINS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. IACK Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. IACK also goes into the high-impedance state when OFF is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupt inputs. $\overline{\text{INT0–3}}$ are prioritized and maskable via the interrupt mask register and interrupt mode bit. The status of these pins can be polled by way of the interrupt flag register.
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. NMI is an external interrupt that cannot be masked by way of the INTM or the IMR. When NMI is activated, the processor traps to the appropriate vector location.

† I = Input, O = Output, Z = High-impedance, S = Supply

Table 1. TMS320C54V90 Pin Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET PINS (CONTINUED)		
$\overline{RS}$	I	Reset input. RS causes the DSP to terminate execution and causes a re-initialization of the CPU and peripherals. When RS is brought to a high level, execution begins at location 0FF80h of program memory. RS affects various registers and status bits.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 16K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/MC bit of the PMST register can override the mode that is selected at reset.
MULTIPROCESSING AND GENERAL PURPOSE PINS		
$\overline{BIO}$	I	Branch control input. A branch can be conditionally executed when BIO is active. If low, the processor executes the conditional instruction. The BIO condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample BIO during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when OFF is low, and is set high at reset.
MEMORY CONTROL PINS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. DS, PS, and IS are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. DS, PS, and IS also go into the high-impedance state when OFF is low.
MSTRB	O/Z	Memory strobe signal. MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. MSTRB also goes into the high-impedance state when OFF is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/W indicates transfer direction during communication to an external device. Normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in high-impedance state in hold mode. R/W also goes into the high-impedance state when OFF is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. IOSTRB is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. IOSTRB also goes into the high-impedance state when OFF is low.
$\overline{HOLD}$	I	Hold input. HOLD is asserted to request control of the address, data, and control lines. When acknowledged by the C54x, these lines go into high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge signal. HOLDA indicates that the DSP is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing the external memory interface to be accessed by other devices. HOLDA also goes into the high-impedance state when is OFF low.
$\overline{MSC}$	O/Z	Microstate complete. $\overline{MSC}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{MSC}$ pin goes active at the beginning of the first software wait state, and goes inactive (high) at the beginning of the last software wait state. If connected to the ready input, $\overline{MSC}$ forces one external wait state after the last internal wait state is completed. $\overline{MSC}$ also goes into the high impedance state when $\overline{OFF}$ is low.
$\overline{IAQ}$	O/Z	Instruction acquisition signal. IAQ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when OFF is low.

† I = Input, O = Output, Z = High-impedance, S = Supply

ADVANCE INFORMATION

Table 1. TMS320C54V90 Pin Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
OSCILLATOR/TIMER PINS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when OFF is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1–CLKMD3 allows you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal oscillator is not being used, an external clock source can be applied to this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when OFF is low.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when OFF is low.
TOUT1	I/O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer1 counts down past zero. The pulse is a CLKOUT cycle wide. The TOUT1 output is multiplexed with the HINT pin of the HPI, and TOUT1 is only available when the HPI is disabled.
MULTI-CHANNEL BUFFERED SERIAL PORT PINS		
BCLKR0 BCLKR1	I/O/Z	Receive clock input. CLKR serves as the serial shift clock for the buffered serial port receiver. BCLKRX2 is McBSP2 transmit AND receive clock. This pin is optionally bondable as C1A (see DAA section).
BDR0 BDR1	I	Serial data receive input.
BFSR0 BFSR1 BFSRX2	I/O/Z	Frame synchronization pulse for receive input. The FSR pulse initiates the receive data process over DR. BFSRX2 is McBSP2 transit AND receive frame sync
BCLKX0 BCLKX1	I/O/Z	Transmit clock. CLKX serves as the serial shift clock for the buffered serial port transmitter. The CLKX pins are configured as inputs after reset. CLKX goes into the high-impedance state when OFF is low.
BDX0 BDX1	O/Z	Serial data transmit output. DX is placed in the high-impedance state when not transmitting, when RS is asserted or when OFF is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit output. The FSX pulse initiates the transmit data process over DX. The FSX pins are configured as inputs after reset. FSX goes into the high-impedance state when OFF is low.
INTEGRATED DAA		
C1A	I/O	DAA I/O connection.
C1A5V	S	Dedicated 5.0V power supply for I/O pin C1A.
$\overline{\text{DAAEN}}$	I	DAA Enable Input. Enables the DAA when low.
UART		
TX	O	UART asynchronous serial transmit data output.
RX	I	UART asynchronous serial receive data input.

† I = Input, O = Output, Z = High-impedance, S = Supply

Table 1. TMS320C54V90 Pin Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
HOST PORT INTERFACE PINS		
A0–A15	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is HIGH.
D0–D15	I/O	These pins can be used to read/write internal memory via the HPI when the HPI16 pin is high. The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when RS or HOLD is asserted. The data bus also goes into the high-impedance state when OFF is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
HD0–HD7	I/O/Z	Parallel bi-directional data bus. These pins can also be used as general-purpose I/O pins when the HPI16 pin is high. HD0–HD7 is placed in the high-impedance state when not outputting data or when OFF is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The HPI data bus holders are disabled at reset, and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control inputs. These inputs select a host access to one of the three HPI registers. (Pull-up only enabled when HPIENA=0, HPI16=1)
HBIL	I	Byte identification input. Identifies first or second byte of transfer. (Pull-up only enabled when HPIENA=0, invalid when HPI16=1)
$\overline{\text{HCS}}$	I	Chip select input. This pin is the select input for the HPI, and must be driven low during accesses. (Pull-up only enabled when HPIENA=0, or HPI16=1)
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	I	Data strobe inputs. These pins are driven by the host read and write strobes to control transfers. (Pull-up only enabled when HPIENA=0)
$\overline{\text{HAS}}$	I	Address strobe input. Address strobe input. Hosts with multiplexed address and data pins require this input, to latch the address in the HPIA register. (Pull-up only enabled when HPIENA=0)
HR/$\overline{\text{W}}$	I	Read/write input. This input controls the direction of an HPI transfer. (Pull-up only enabled when HPIENA=0)
HRDY	O/Z	Ready output. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when OFF is low.
$\overline{\text{HINT}}$	O/Z	Interrupt output. This output is used to interrupt the host. When the DSP is in reset, this signal is driven high. HINT can also be used for timer 1 output (TOUT1), when the HPI is disabled. The signal goes into the high-impedance state when OFF is low. (invalid when HPI16=1)
HPIENA	I	HPI enable input. This pin must be driven high during reset to enable the HPI. An internal pull-down resistor is always active and the HPIENA pin is sampled on the rising edge of RS. If HPIENA is left open or driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the DSP is reset.
HPI16	I	HPI 16-bit Select Pin. HPI16=1 selects the non-multiplexed mode. The non- multiplexed mode allows hosts with separate address/data buses to access the HPI address range via the 16 address pins A0–A15. 16-bit Data is also accessible through pins D0–D15. HOST-to-DSP and DSP-to-HOST interrupts are not supported. There are no HPIC and HPIA registers in the non-multiplexed mode since there are HCNTRL0,1 signals available. Internally pulled low.
SUPPLY PINS		
CV_{DD}	S	$+V_{DD}$. Dedicated 1.5V power supply for the core CPU.
DV_{DD}	S	$+V_{DD}$. Dedicated 3.3V power supply for I/O pins.
V_{SS}	S	Ground.

† I = Input, O = Output, Z = High-impedance, S = Supply

Table 1. TMS320C54V90 Pin Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
SUPPLY PINS (CONTINUED)		
TCK	I	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input, pin with internal pull-up device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when OFF is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pull-up device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard 1149.1 test reset. TRST, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If TRST is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator 0 pin. When TRST is driven low, EMU0 must be high for activation of the OFF condition. When TRST is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system.
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator 1 pin/disable all outputs. When TRST is driven high, EMU1/OFF is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When TRST is driven low, EMU1/OFF is configured as OFF. The EMU1/OFF signal, when active low, puts all output drivers into the high-impedance state. Note that OFF is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for the OFF feature, the following conditions apply: TRST=low, EMU0=high, EMU1/OFF = low

† I = Input, O = Output, Z = High-impedance, S = Supply

ADVANCE INFORMATION

pin descriptions: PCT308W

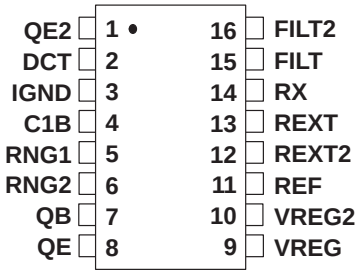


Table 2. PCT308W Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	QE2	**TRANSISTOR EMITTER 2.** Connects to the emitter of Q4.
2	DCT	**DC TERMINATION.** Provides DC termination to the telephone network.
3	IGND	**ISOLATED GROUND.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**ISOLATION CAPACITOR 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side module.
5	RNG1	**RING 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the PCT308W.
6	RNG2	**RING 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the PCT308W.
7	QB	**TRANSISTOR BASE.** Connects to the base of transistor Q3. Used to go on/off-hook.
8	QE	**TRANSISTOR EMITTER.** Connects to the emitter of transistor Q3. Used to go on/off-hook.
9	VREG	Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**REFERENCE.** Connects to an external resistor to provide a high accuracy reference current.
12	REXT2	**EXTERNAL RESISTOR 2.** Sets the complex AC termination impedance.
13	REXT	**EXTERNAL RESISTOR.** Sets the real AC termination impedance.
14	RX	**RECEIVE INPUT.** Serves as the receive side input from the telephone network.
15	FILT	**FILTER.** Provides filtering for the DC termination circuits.
16	FILT2	**FILTER 2.** Provides filtering for the bias circuits.

ADVANCE INFORMATION

functional description

TMS320C54V90 DSP and memory

The DSP is a 16-bit processor operating at up to 117 MIPS. It has 40K x 16 RAM and 128K x 16 program ROM on-chip. This provides complete “controller-based” modem functionality with no external memory.

The DSP firmware implements all the modem signal processing, V.42 error correction, V.42bis compression, AT command parser, and modem controller functions.

block diagram

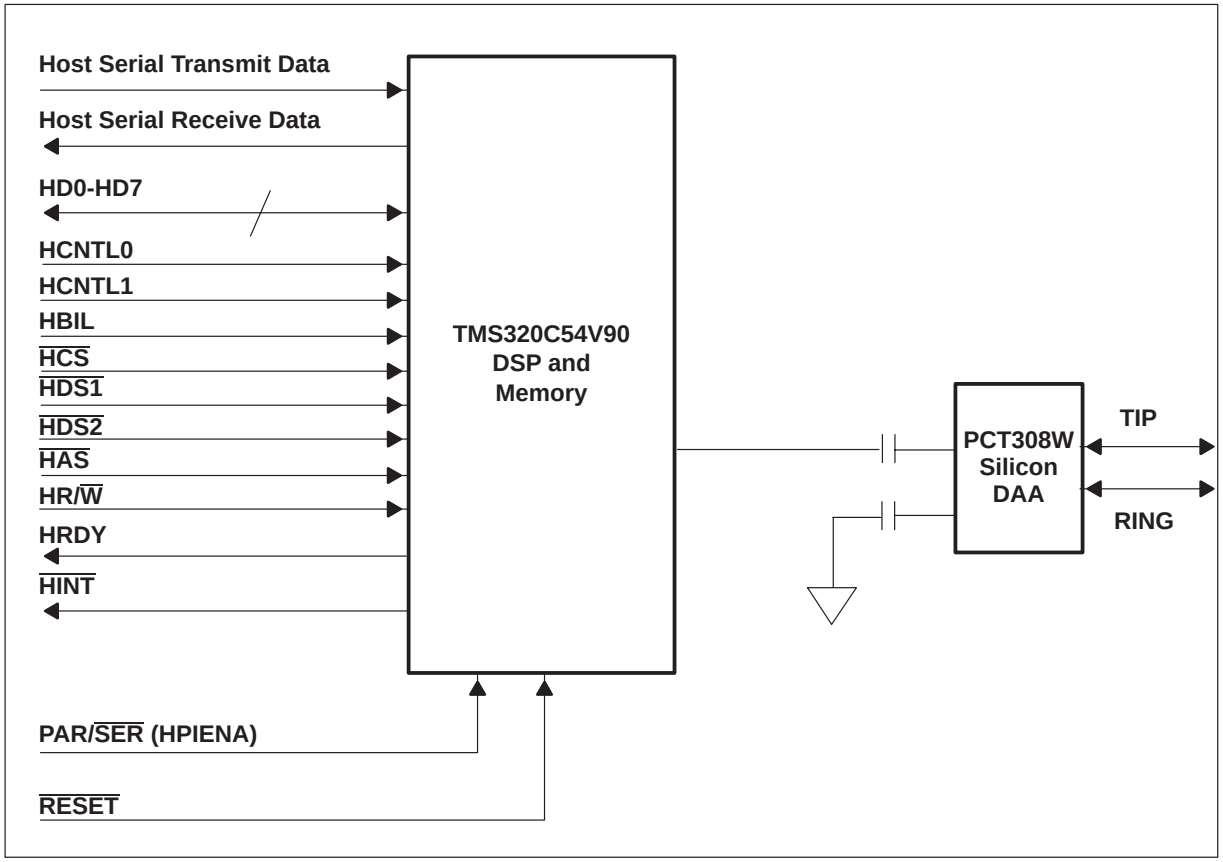


Figure 1. TMS320C54V90 Modem Block Diagram

PCT308W silicon DAA

The DAA block provides all the functions associated with the telephone line interface and the analog front end, including:

- On hook/off hook control
- DC termination
- AC termination
- Ring detect
- Dielectric isolation
- Surge protection
- Loop current monitor
- 2-wire/4-wire hybrid
- Receive and Transmit filters
- D/A and A/D converters
- On-hook loop voltage sensing (optional)

PCT308W silicon DAA (continued)

Certain characteristics of the DAA, such as DC and AC termination, are programmable to meet the requirements of different countries/administrations. Normally, these details are invisible to the user, and the proper characteristics are selected using an AT command and a country code.

Likewise, call origination, dialing, automatic answering, etc. are controlled by AT commands, and the TMS320C54V90 firmware controls the details of DAA functions. The DAA also supports power-down and wake-up-on-ring modes.

The interface between the DSP and the DAA carries both Transmit and Receive line signals as digitized samples, as well as control information for the DAA.

mode selection

The CLKMD inputs select various initial conditions for the clocking system and PLLs at power-up. The TMS320C54V90 also uses these inputs to select various operating modes. Use of any of the “reserved” combinations may prevent proper operation of the modem (for example, by disabling the crystal oscillator).

Table 3. Mode Selection with CLKMD pins

MODE	CKLMD1	CLKMD2	CLKMD3	CONFIGURATION
0	0	0	0	reserved
1	0	0	1	reserved
2	0	1	0	reserved
3	0	1	1	reserved
4	1	0	0	reserved
5	1	0	1	Normal mode, 117 MIPS
6	1	1	0	reserved
7	1	1	1	Normal mode, 58 MIPS

clock requirements

The standard reference design includes a crystal from which clocks are derived for the DSP and the DAA. The nominal clock frequency is 14.7456 MHz.

power requirements

The TMS320C54V90 requires 3.3V for the DSP I/Os and the DAA, 1.5V for the DSP core, and 5V for the capacitively-coupled interface between the DSP and DAA. The method of deriving these different voltages will depend on what power is available in the host system, cost, and efficiency considerations.

The reference design assumes that an active low power-on reset signal at 3.3V logic levels is available from the host system.

serial and parallel interface modes

The TMS320C54V90 modem can interface with the host system either serially, via an RS-232 connection, or in parallel, via the HPI.

The selection between these two types of interfaces is made using the PAR/$\overline{\text{SER}}$ (HPIENA) input pin.

For either interface, the same set of pins are used, but with different functionality.

Table 4 shows the functionality of the modem host interface pins in both the serial and parallel interface modes.

serial and parallel interface modes (continued)

Details of the operation of both these types of host interface are presented the following sections of this document.

Table 4. I/O Definition for Serial and Parallel Modes

SIGNAL NAME	FUNCTION IN PARALLEL MODE (HPIENA=3.3V)	FUNCTION IN SERIAL MODE (HPIENA=0V)
UARTRX	Not Used	TXD (Serial Transmit Data)
UARTTX	Modem Constellation X/Y Data	RXD (Serial Receive Data)
HD0	Host Port Data Bus bit 0	DTR (Data Terminal Ready)
HD1	Host Port Data Bus bit 1	RTS (Request to Send)
HD2	Host Port Data Bus bit 2	CTS (Clear to Send)
HD3	Host Port Data Bus bit 3	DSR (Data Set Ready)
HD4	Host Port Data Bus bit 4	DCD (Data Carrier Detect)
HD5	Host Port Data Bus bit 5	RI (Ring Indication)
HD6	Host Port Data Bus bit 6	Not Used
HD7	Host Port Data Bus bit 7	Not Used
HCNTL0	Host Port Control 0	Not Used
HCNTL1	Host Port Control 1	Not Used
HBIL	Byte Order Identifier	Not Used
$\overline{\text{HCS}}$	Chip Select	Not Used
$\overline{\text{HDS1}}$	Data Strobe 1	Not Used
$\overline{\text{HDS2}}$	Data Strobe2	Not Used
$\overline{\text{HAS}}$	Address Strobe	Not Used
HR/$\overline{\text{W}}$	Read/Write	Not Used
HRDY	Host Port Ready	Not Used
HINT	Host Port Interrupt	Not Used

serial interface

If the PAR/$\overline{\text{SER}}$ input is held low when $\overline{\text{RESET}}$ is released, the modem will operate with a serial interface instead of a parallel interface. The HD0-7 pins become general purpose I/O pins and are used for EIA-232 control signals as shown in Table 4 on page 14. The serial data is carried on SERIAL TRANSMIT DATA and SERIAL RECEIVE DATA. These signals are at 3.3V logic levels, and the polarity is correct for inverting EIA-232 drivers and receivers.

The serial interfaced is implemented with an on-chip UART. Data rates from 300 bits per second to 230400 bits per second are supported. The default rate is 115200 bits per second. Autobaud (automatic detection of data rate and character format) is not supported. The character format is 10 bit, i.e., 1 start, 8 data, and 1 stop bit. Both RTS/CTS and XON/XOFF flow control are supported.

host port interface (HPI)

The host port interface (HPI) is an 8-bit parallel port used to interface a host processor to the DSP. Information is exchanged between the DSP and the host processor through a 2K-word block of on-chip memory that is accessible by both the host and the DSP. The DSP has access to the HPI control register (HPIC) and the host can address the HPI memory through the HPI address register (HPIA).

Both the host and the DSP have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one HPI cycle.

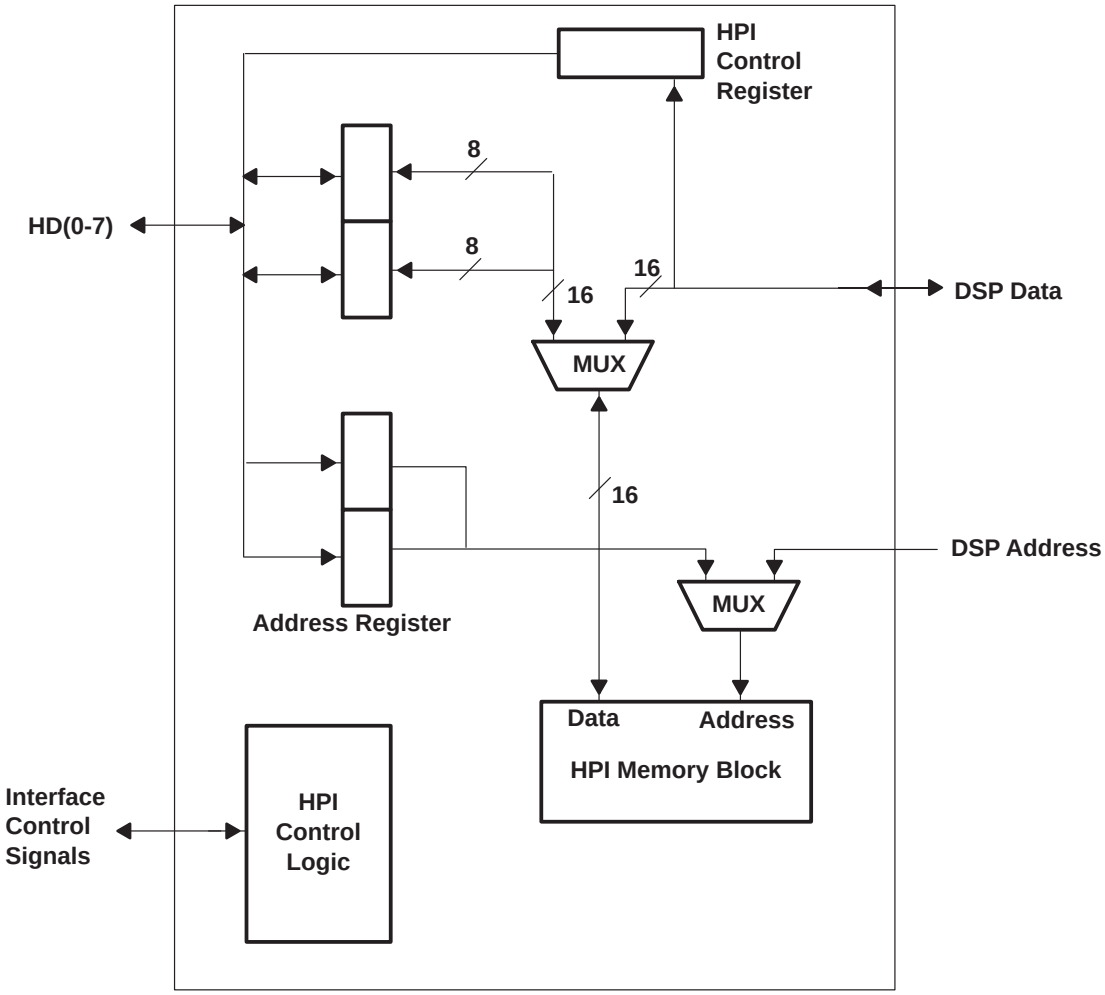


Figure 2. Host Processor Interface Block Diagram

The HPI interface consists of an 8-bit bidirectional data bus and various control signals. Data transfers of 16-bit words occur as two consecutive bytes with a dedicated pin (HBIL) indicating whether the high or low byte is being transmitted. Two control pins, HCNTL1 and HCNTL0, control host access to the HPIA, HPI data (with an optional automatic address increment), or the HPIC. The host can interrupt the DSP device by writing to HPIC. The DSP device can interrupt the host with a dedicated $\overline{\text{HINT}}$ pin that the host can acknowledge and clear.

host port interface (HPI) (continued)

The HPI control logic has two data strobes, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, a read/write strobe HR/W, and an address strobe $\overline{\text{HAS}}$, to enable a glueless interface to a variety of industry-standard host devices. The HPI is interfaced easily to hosts with multiplexed address/data bus, separate address and data buses, one data strobe and a read/write strobe, or two separate strobes for read and write. The HPI supports high-speed back-to-back accesses.

The HPI can handle one byte every five DSP device periods-that is, 64 Mbps with a 40-MIPS DSP, or 160 Mbps with a 100-MIPS DSP. The HPI is designed so that the host can take advantage of this high bandwidth and run at frequencies up to (f * n)/5, where *n* is the number of host cycles for an external access and *f* is the DSP device frequency.

basic host port interface functional description

The external HPI consists of the 8-bit HPI data bus and control signals that configure and control the interface. The interface can connect to a variety of host devices with little or no additional logic. Figure 3 shows a simplified diagram of a connection between the HPI and a host device. The 8-bit data bus (HD0-HD7) exchanges information with the host. Because of the 16-bit word structure of the DSP, all transfers with a host must consist of two consecutive bytes. The dedicated HBIL pin indicates whether the first or second byte is being transferred. An internal control register bit determines whether the first or second byte is placed into the most significant byte of a 16-bit word. The host must not break the first byte/second byte (HBIL low/high) sequence of an ongoing HPI access. If this sequence is broken, data can be lost, and unpredictable operation can result.

The two control inputs (HCNTL0 and HCNTL1) indicate which internal HPI register is being accessed and the type of access to the register. These inputs, along with HBIL, are commonly driven by host address bus bits or a function of these bits. Using the HCNTL0/1 inputs, the host can specify an access to the HPI control (HPIC) register, the HPI address (HPIA) register (which serves as the pointer into HPI memory), or HPI data (HPID) register. The HPID register can also be accessed with an optional automatic address increment.

The autoincrement feature provides a convenient way of reading or writing to subsequent word locations. In autoincrement mode, a data read causes a postincrement of the HPIA, and a data write causes a preincrement of the HPIA. By writing to the HPIC, the host can interrupt the DSP CPU, and the $\overline{\text{HINT}}$ output can be used by the DSP to interrupt the host. The host can also acknowledge and clear $\overline{\text{HINT}}$ by writing to the HPIC.

basic host port interface functional description (continued)

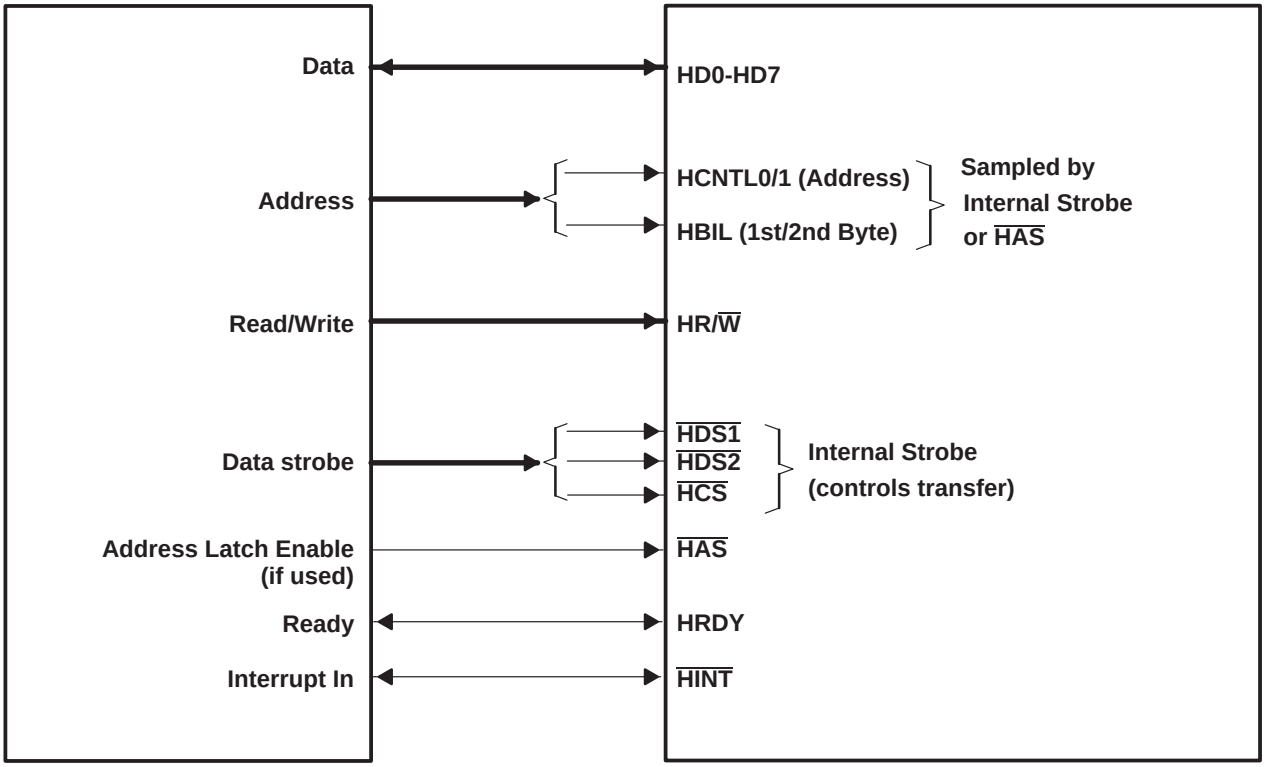


Figure 3. Generic System Block Diagram

Table 5 summarizes the three registers that the HPI utilizes for communication between the host device and the DSP CPU and their functions.

Table 5. HPI Registers Description

NAME	DESCRIPTION
HPIA	Directly accessible only by the host. Contains the address in the HPI memory at which the current access occurs.
HPIC	HPI control register. Directly accessible by either the host or by the DSP. Contains control and status bits for HPI operations.
HPID	HPI data register. Directly accessible only by the host. Contains the data that was read from the HPI memory if the current access is a read, or the data that will be written to HPI memory if the current access is a write.

The HPI ready pin (HRDY) allows insertion of wait states for hosts that support a ready input to allow deferred completion of access cycles and have faster cycle times than the HPI can accept due to DSP operating clock rates. If HRDY, when used directly from the DSP, does not meet host timing requirements, the signal can be resynchronized using external logic if necessary. HRDY is useful when the DSP operating frequency is variable, or when the host is capable of accessing at a faster rate than the maximum shared-access mode access rate. In both cases, the HRDY pin provides a convenient way to automatically (no software handshake needed) adjust the host access rate to a faster DSP clock rate.

All of these features combined allow the HPI to provide a flexible and efficient interface to a wide variety of industry-standard host devices. Also, the simplicity of the HPI interface greatly simplifies data transfers both from the host and the DSP sides of the interface. Once the interface is configured, data transfers are made with a minimum of overhead at a maximum speed.

details of host port interface operation

This subsection includes a detailed description of each HPI external interface pin function, as well as descriptions of the register and control bit functions. Logical interface timings and initialization and read/write sequences are discussed in section, *Host Read/Write Access to HPI*.

The external HPI interface signals implement a flexible interface to a variety of types of host devices. Devices with single or multiple data strobes and with or without address latch enable (ALE) signals can easily be connected to the HPI.

HPI signal names and functions

Table 6 describes the function HPI external interface pins in detail.

Table 6. HPI Signal Names and Functions

HPI PIN	HOST PIN	STATE†	SIGNAL FUNCTION
$\overline{\text{HAS}}$	Address latch enable (ALE) or Address strobe or unused (tied high)	I	Address strobe input. Hosts with a multiplexed address and data bus connect $\overline{\text{HAS}}$ to their ALE pin or equivalent. HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ are then latched on $\overline{\text{HAS}}$ falling edge. When used, $\overline{\text{HAS}}$ must precede the later of $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, or $\overline{\text{HDS2}}$ (see detailed HPI timing specifications on page 29). Hosts with separate address and data bus can connect $\overline{\text{HAS}}$ to a logic-1 level. In this case, HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ are latched by the later of $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, or $\overline{\text{HCS}}$ falling edge while $\overline{\text{HAS}}$ stays inactive (high).
HBIL	Address or control lines	I	Byte identification input. Identifies first or second byte of transfer (but not most significant or least significant - this is specified by the BOB bit in the HPIC register, described later in this section). HBIL is low for the first byte and high for the second byte.
HCNTL0 HCNTL1	Address or control lines	I	Host control inputs. Selects a host access to the HPIA register, the HPI data latches (with optional address increment), or the HPIC register.
$\overline{\text{HCS}}$	Address or control lines	I	Chip select. Serves as the enable input for the HPI and must be low during an access but may stay low between accesses. $\overline{\text{HCS}}$ normally precedes $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, but this signal also samples HCNTL0/1, HR/$\overline{\text{W}}$, and HBIL if $\overline{\text{HAS}}$ is not used and $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$ are already low (this is explained in further detail later in this subsection). Table 7 shows the equivalent circuit of the $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ inputs.
HD0-HD7	Data bus	I/O/Z	Parallel bidirectional 3-state data bus. HD7 (MSB) through HD0 (LSB) are placed in the high-impedance state when not outputting ($\overline{\text{HDS}} \mid \overline{\text{HCS}} = 1$).
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	Read strobe and write strobe or data strobe	I	Data strobe inputs. Control transfer of data during host access cycles. Also, when $\overline{\text{HAS}}$ is not used, used to sample HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ when $\overline{\text{HCS}}$ is already low (which is the case in normal operation). Hosts with separate read and write strobes connect those strobes to either $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$. Hosts with a single data strobe connect it to either $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$, connecting the unused pin high. Regardless of HDS connections, HR/$\overline{\text{W}}$ is still required to determine direction of transfer. Because $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are internally exclusive-NORed, hosts with a high true data strobe can connect this to one of the HDS inputs with the other HDS input connected low. Table 7 shows the equivalent circuit of the $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, and $\overline{\text{HCS}}$ inputs.
$\overline{\text{HINT}}$	Host interrupt input	O/Z	Host interrupt output. Controlled by the HINT bit in the HPIC. Driven high when the DSP is being reset.

† I = Input, O = Output, Z = High Impedance

Table 6. HPI Signal Names and Functions (Continued)

HPI PIN	HOST PIN	STATE†	SIGNAL FUNCTION
HRDY	Asynchronous ready	O/Z	HPI ready output. When high, indicates that the HPI is ready for a transfer to be performed. When low, indicates that the HPI is busy completing the internal portion of the previous transaction. $\overline{HCS}$ enables HRDY; that is, HRDY is always high when $\overline{HCS}$ is high.
HR/$\overline{W}$	Read/Write strobe, address line, or multiplexed address/data	I	Read/write input. Hosts must drive HR/$\overline{W}$ high to read HPI and low to write HPI. Hosts without a read/write strobe can use an address line for this function.

† I = Input, O = Output, Z = High Impedance

The $\overline{HCS}$ input serves primarily as the enable input for the HPI, and the $\overline{HDS1}$ and $\overline{HDS2}$ signals control the HPI data transfer; however, the logic with which these inputs are implemented allows their functions to be interchanged if desired. If $\overline{HCS}$ is used in place of $\overline{HDS1}$ and $\overline{HDS2}$ to control HPI access cycles, HRDY operation is affected (since $\overline{HCS}$ enables HRDY and HRDY is always high when $\overline{HCS}$ is high). The equivalent circuit for these inputs is shown in Table 7. The figure shows that the internal strobe signal that samples the HCNTL0/1, HBIL, and HR/$\overline{W}$ inputs (when $\overline{HAS}$ is not used) is derived from all three of the input signals, as the logic illustrates. Therefore, the latest of $\overline{HDS1}$, $\overline{HDS2}$, or $\overline{HCS}$ is the one which actually controls sampling of the HCNTL0/1, HBIL, and HR/$\overline{W}$ inputs. Because $\overline{HDS1}$ and $\overline{HDS2}$ are exclusive-NORed, both these inputs being low does not constitute an enabled condition.

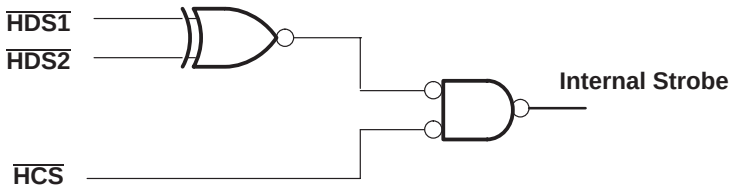


Figure 4. Select Input Logic

When using the $\overline{HAS}$ input to sample HCNTL0/1, HBIL, and HR/$\overline{W}$, this allows these signals to be removed earlier in an access cycle, therefore allowing more time to switch bus states from address to data information, facilitating interface to multiplexed address and data type buses. In this type of system, an ALE signal is often provided and would normally be the signal connected to HAS.

The two control pins (HCNTL0 and HCNTL1) indicate which internal HPI register is being accessed and the type of access to the register. The states of these two pins select access to the HPI address (HPIA), HPI data (HPID), or HPI control (HPIC) registers. The HPIA register serves as the pointer into HPI memory, the HPIC contains control and status bits for the transfers, and the HPID contains the actual data transferred. Additionally, the HPID register can be accessed with an optional automatic address increment. Table 7 describes the HCNTL0/1 bit functions.

On the DSP, HPI memory is a 2K 16-bit word block of dual-access RAM. From the host interface, the 2K-word block of HPI memory can conveniently be accessed at addresses 0 through 7FFh; however, the memory can also be accessed by the host starting with any HPIA values with the 11 LSBs equal to 0. For example, the first word of the HPI memory block can be accessed by the host with any of the following HPIA values: 0000h, 0800h,1000h,1800h, ... F800h.

HPI signal names and functions (continued)

Table 7. HPI Input Control Signals Function Selection Descriptions

HCNTL1	HCNTL0	
0	0	Host can read or write the HPI control register, HPIC.
0	1	Host can read or write the HPI data latches. HPIA is automatically postincremented each time a read is performed and preincremented each time a write is performed.
1	0	Host can read or write the address register, HPIA. This register points to the HPI memory.
1	1	Host can read or write the HPI data latches. HPIA is not affected.

The HPI autoincrement feature provides a convenient way of accessing consecutive word locations in HPI memory. In the autoincrement mode, a data read causes a postincrement of the HPIA, and a data write causes a preincrement of the HPIA. Therefore, if a write is to be made to the first word of HPI memory with the increment option, due to the preincrement nature of the write operation, the HPIA should first be loaded with any of the following values: 07FFh, 0FFFh, 17FFh, ... FFFFh. The HPIA is a 16-bit register and all 16 bits can be written to or read from, although with a 2K-word HPI memory implementation, only the 11 LSBs of the HPIA are required to address the HPI memory. The HPIA increment and decrement affect all 16 bits of this register.

HPI control register bits and function

Four bits control HPI operation. These bits are BOB (which selects first or second byte as most significant), SMOD (which selects host or shared-access mode), and DSPINT and HINT (which can be used to generate DSP and host interrupts, respectively) and are located in the HPI control register (HPIC). A detailed description of the HPIC bit functions is presented in Table 8.

Because the host interface always performs transfers with 8-bit bytes and the control register is normally the first register accessed to set configuration bits and initialize the interface, the HPIC is organized on the host side as a 16-bit register with the same high and low byte contents (although access to certain bits is limited, as described previously) and with the upper bits unused on the DSP side. The control/status bits are located in the least significant four bits. The host accesses the HPIC register with the appropriate selection of HCNTL0/1, as described previously, and two consecutive byte accesses to the 8-bit HPI data bus. When the host writes to HPIC, both the first and second byte written **must** be the same value.

The layout of the HPIC bits is shown in Figure 5 through Figure 8. In the tables for read operations, if 0 is specified, this value is always read; if X is specified, an unknown value is read. For write operations, if X is specified, any value can be written. On a host write, both bytes must be identical. Note that bits 4-7 and 12-15 on the host side and bits 4-15 on the DSP side are reserved for future expansion.

HPI control register bits and function (continued)

Table 8. HPI Control Register (HPIC) Bit Descriptions

BIT	HOST ACCESS	DSP ACCESS	DESCRIPTION
BOB	Read/Write	--	If BOB = 1, first byte is least significant. If BOB = 0, first byte is most significant. BOB affects both data and address transfers. Only the host can modify this bit and it is not visible to the DSP. BOB must be initialized before the first data or address register access.
SMOD	Read	Read/Write	If SMOD = 1, shared-access mode (SAM) is enabled: the HPI memory can be accessed by the DSP. (This is the only mode used in the TM-100 application. SMOD = 0 during reset; SMOD = 1 after reset. SMOD can be modified only by the DSP but can be read by both the DSP and the host.
DSPINT	Write	--	The host processor-to-DSP interrupt. This bit can be written only by the host and is not readable by the host or the DSP. When the host writes a 1 to this bit, an interrupt is generated to the DSP. Writing a 0 to this bit has no effect. Always read as 0. When the host writes to HPIC, both bytes must write the same value.
$\overline{\text{HINT}}$	Read/Write	Read/Write	This bit determines the state of the DSP $\overline{\text{HINT}}$ output, which can be used to generate an interrupt to the host. HINT = 0 upon reset, which causes the external $\overline{\text{HINT}}$ output to be inactive (high). The HINT bit can be set only by the DSP and can be cleared only by the host. The DSP writes a 1 to HINT, causing the $\overline{\text{HINT}}$ pin to go low. The HINT bit is read by the host or the DSP as a 0 when the external $\overline{\text{HINT}}$ pin is inactive (high) and as a 1 when the $\overline{\text{HINT}}$ pin is active (low). For the host to clear the interrupt, however, it must write a 1 to HINT. Writing a 0 to the HINT bit by either the host or the DSP has no effect.

15–12	11	10	9	8	7–4	3	2	1	0
X	HINT	0	SMOD	BOB	X	HINT	0	SMOD	BOB

Note: X = Unknown value is read.

Figure 5. HPIC Diagram - Host Reads from HPIC

15–12	11	10	9	8	7–4	3	2	1	0
X	HINT	DSPINT	X	BOB	X	HINT	DSPINT	X	BOB

Note: X = Any value can be written.

Figure 6. HPIC Diagram - Host Writes to HPIC

ADVANCE INFORMATION

HPI control register bits and function (continued)

15–4	3	2	1	0
X	HINT	0	SMOD	0

Note: X = Unknown value is read.

Figure 7. HPIC Diagram - DSP Reads from HPIC

15–4	3	2	1	0
X	HINT	X	SMOD	X

Note: X = Any value can be written.

Figure 8. HPIC Diagram - DSP Writes to HPIC

Because the DSP can write to the SMOD and HINT bits, and these bits are read twice on the host interface side, the first and second byte reads by the host may yield different data if the DSP changes the state of one or both of these bits in between the two read operations. The characteristics of host and DSP HPIC read/write cycles are summarized in Table 9.

Table 9. DSP HPIC Read/Write Cycles

DEVICE	READ	WRITE
Host	2 bytes	2 bytes (Both bytes must be equal)
DSP	16 bits	16 bits

host read/write access to HPI

The host begins HPI accesses by performing the external interface portion of the cycle; that is, initializing first the HPIC register, then the HPIA register, and then writing data to or reading data from the HPID register. Writing to HPIA or HPID initiates an internal cycle that transfers the desired data between the HPID and the dedicated internal HPI memory. Because this process requires several DSP cycles, each time an HPI access is made, data written to the HPID is not written to the HPI memory until after the host access cycle, and the data read from the HPID is the data from the previous cycle. Therefore, when reading, the data obtained is the data from the location specified in the previous access, and the current access serves as the initiation of the next cycle. A similar sequence occurs for a write operation: the data written to HPID is not written to HPI memory until after the external cycle is completed. If an HPID read operation immediately follows an HPID write operation, the same data (the data written) is read.

The autoincrement feature available for HPIA results in sequential accesses to HPI memory by the host being extremely efficient. During random (nonsequential) transfers or sequential accesses with a significant amount of time between them, it is possible that the DSP may have changed the contents of the location being accessed between a host read and the previous host data read/write or HPIA write access, because of the prefetch nature of internal HPI operation. If this occurs, data different from the current memory contents may be read. Therefore, in cases where this is of concern in a system, two reads from the same address or an address write prior to the read access can be made to ensure that the most recent data is read.

When the host performs an external access to the HPI, there are two distinctly different types of cycles that can occur: those for which wait states are generated (the HRDY signal is active) and those without wait states.

host read/write access to HPI (continued)

For accesses utilizing the HRDY signal, during the time when the internal portion of the transfer is being performed (either for a read or a write), HRDY is low, indicating that another transfer cannot yet be initiated. Once the internal cycle is completed and another external cycle can begin, HRDY is driven high by the HPI. This occurs after a fixed delay following a cycle initiation (refer to the DSP data sheet for detailed timing information for HPI external interface timings). Therefore, unless back-to-back cycles are being performed, HRDY is normally high when the first byte of a cycle is transferred. The external HPI cycle using HRDY is shown in the timing diagram in Figure 9.

In a typical external access, as shown in Figure 9, the cycle begins with the host driving HCNTL0/1, HR/$\overline{W}$, HBIL, and $\overline{HCS}$, indicating specifically what type of transfer is to occur and whether the cycle is to be read or a write. Then the host asserts the $\overline{HAS}$ signal (if used) followed by one of the data strobe signals. If HRDY is not already high, it goes high when the previous internal cycle is complete, allowing data to be transferred, and the control signals are deasserted. Following the external HPI cycle, HRDY goes low and stays low for a period of approximately five CLKOUT cycles (refer to the DSP data sheet for HPI timing information) while the DSP completes the internal HPI memory access, and then HRDY is driven high again. Note, however, HRDY is always high when $\overline{HCS}$ is high.

As mentioned previously, SAM accesses generally utilize the HRDY signal. The exception to the HRDY-based interface timings when in SAM occurs when reading HPIC or HPIA or writing to HPIC (except when writing 1 to either DSPINT or HINT). In these cases, HRDY stays high; for all other SAM accesses, HRDY is active.

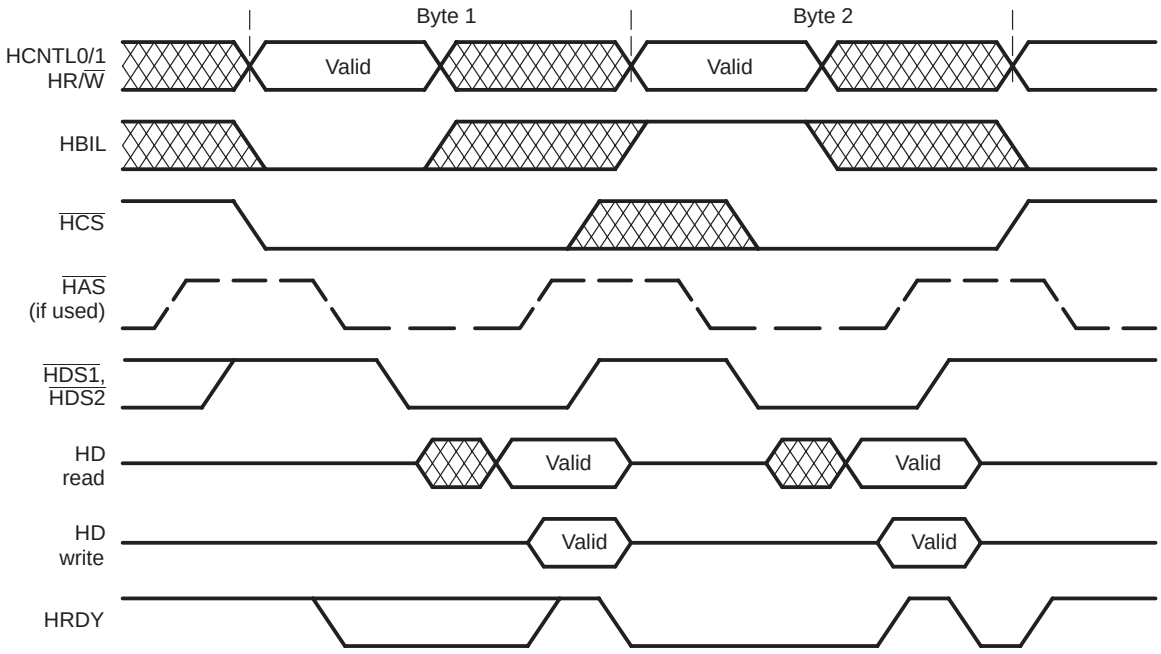


Figure 9. HPI Timing Diagram

host read/write access to HPI (continued)

Table 10. Wait-State Generation Conditions

REGISTER	WAIT STATE GENERATED	
	READS	WRITES
HPIC	No	1 to DSPINT/HINT - Yes All other cycles - No
HPIA	No	Yes
HPID	Yes	Yes

example access sequences

A complete host access cycle always involves two bytes, the first with HBIL low, and the second with HBIL high. This 2-byte sequence must be followed regardless of the type of host access (HPIA, HPIC, or data access) and the host must not break the first byte/second byte (HBIL low/high) sequence of an ongoing HPI access. If this sequence is broken, data may be lost, and unpredictable operation may result.

Before accessing data, the host must first initialize HPIC, in particular the BOB bit, and then HPIA (in this order, because BOB affects the HPIA access). After initializing BOB, the host can then write to HPIA with the correct byte alignment. On an HPI memory read operation, after completion of the HPIA write, the HPI memory is read and the contents at the given address are transferred to the two 8-bit data latches, the first byte data latch and the second byte data latch. Table 11 illustrates the sequence involved in initializing BOB and HPIA for an HPI memory read. In this example, BOB is set to 0 and a read is requested of the first HPI memory location (in this case 1000h), which contains FFFEh.

Table 11. Initialization of BOB and FPIA

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host writes HPIC, 1st byte	00	0	00	0	00xx	xxxx	xxxx	xxxx
Host writes HPIC, 2nd byte	00	0	00	1	0000	xxxx	xxxx	xxxx
Host writes HPIA, 1st byte	10	0	10	0	0000	10xx	xxxx	xxxx
Host writes HPIA, 2nd byte	00	0	10	1		1000	xxxx	
Internal HPI RAM read complete						1000	FF	FE

In the cycle shown in Table 11, BOB and HPIA are initialized, and by loading HPIA, an internal HPI memory access is initiated. The last line of Table 11 shows the condition of the HPI after the internal RAM read is complete; that is, after some delay following the end of the host write of the second byte to HPIA, the read is completed and the data has been placed in the upper and lower byte data latches. For the host to actually retrieve this data, it must perform an additional read of HPID. During this HPID read access, the contents of the first byte data latch appears on the HD pins when HBIL is low and the content of the second byte data latch appears on the HD pins when HBIL is high. Then the address is incremented if autoincrement is selected and the memory is read again into the data latches. The sequence involved in this access is shown in Table 12.

example access sequences (continued)

Table 12. Read Access to HPI with Autoincrement

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host reads data, 1st byte	FF	1	01	0	0000	1000	FF	FE
Host reads data, 2nd byte	FE	1	01	1	0000	1000	FF	FE
Internal HPI RAM read complete						1001	6A	BC

In the access shown in Table 12, the data obtained from reading HPID is the data from the read initiated in the previous cycle (the one shown in Table 11) and the access performed as shown in Table 12 also initiates a further read, this time at location 1001h (because autoincrement was specified in this access by setting HCNTL1/0 to 01). Also, when autoincrement is selected, the increment occurs with each 16-bit word transferred (not with each byte); therefore, as shown in Table 12, the HPIA is incremented by only 1. The last line of Table 12 indicates that after the second internal RAM read is complete, the contents of location 1001h (6ABCh) has been read and placed into the upper and lower byte data latches.

During a write access to the HPI, the first byte data latch is overwritten by the data coming from the host while the HBIL pin is low, and the second byte data latch is overwritten by the data coming from the host while the HBIL pin is high. At the end of this write access, the data in both data latches is transferred as a 16-bit word to the HPI memory at the address specified by the HPIA register. The address is incremented prior to the memory write because autoincrement is selected.

An HPI write access is illustrated in Table 13. In this example, after the internal portion of the write is completed, location 1002h of HPI RAM contains 1234h. If a read of the same address follows this write, the same data just written in the data latches (1234h) is read back.

Table 13. Write Access to HPI with Autoincrement

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host writes data, 1st byte	12	0	01	0	0000	1002	12	FE
Host writes data, 2nd byte	34	0	01	1	0000	1002	12	34
Internal HPI RAM write complete						1002	12	34

host device using DSPINT to interrupt the DSP

A DSP interrupt is generated when the host writes a 1 to the DSPINT bit in HPIC. The host and the DSP always read this bit as 0. A DSP write has no effect. Once a 1 is written to DSPINT by the host, a 0 need not be written before another interrupt can be generated, and writing a 0 to this bit has no effect. The host should not write a 1 to the DSPINT bit while writing to BOB or HINT, or an unwanted DSP interrupt is generated.

host port interface (DSP) using HINT to interrupt the host device

When the DSP writes a 1 to the HINT bit in HPIC, the $\overline{HINT}$ output is driven low; the HINT bit is read as a 1 by the DSP or the host. The HINT signal can be used to interrupt the host device. The host device, after detecting the $\overline{HINT}$ interrupt line, can acknowledge and clear the DSP interrupt and the HINT bit by writing a 1 to the HINT bit. The HINT bit is cleared and then read as a 0 by the DSP or the host, and the $\overline{HINT}$ pin is driven high. If the DSP or the host writes a 0, the HINT bit remains unchanged.

absolute maximum ratings

Differential Voltage Tip to Ring (steady-state, excluding surges) . . . . . 275 V
Voltage Tip-to-Ground or Ring-to-Ground . . . . . 2000 V
Supply voltage I/O range, DV_{DD} . . . . . –0.3 to 4.0 V
Supply voltage core range, CV_{DD} . . . . . –0.3 to 2.0 V
Input Voltage- Logic inputs . . . . . –0.3 to 4.5 V
Output Voltage . . . . . –0.3 to 4.5 V
Operating case temperature range . . . . . –40°C to 100°C
Storage temperature . . . . . –40°C to 150°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 14 describes the recommended operating conditions.

Table 14. Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
T_C	Operating Case Temperature		-40		100	°C
DV_{DD}	Supply Voltage, I/O†		2.7	3.3	3.6	V
CV_{DD}	Supply Voltage, DSP core		1.42	1.5	1.65	V
C1A5V	Supply Voltage, DAA‡		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{RESET}$, INTn, NMI, X2/CLKIN, BIO, BCLKR0, BCLKR1, BCLKR2, BCLKX0, BCLKX1, BCLKX2, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, TCK, CLKMDn	2.2		V_{cc} + 0.3	V
		All other inputs	1.8		V_{cc} + 0.3	
V_{IL}	Low-level input voltage	$\overline{RESET}$, INTn, NMI, X2/CLKIN, BIO, BCLKR0, BCLKR1, BCLKR2, BCLKX0, BCLKX1, BCLKX2, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, TCK, CLKMDn	-0.3		0.6	V
		All other inputs	-0.3		0.8	
I_{OH}	High-level output current				-300	µA
I_{OL}	Low-level output current				1.5	mA

† DV_{DD} must be > C1A5V – 3.3 V during power-up.
‡ C1A5V must be > DV_{DD} – 0.5 V during power-up.

absolute maximum ratings (continued)

Table 15 describes the electrical characteristics of the TMS320C54V90.

Table 15. Electrical Characteristics Over Recommended Operating Case Temperature Range

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		DV_{DD} = 3.3 ±0.3 V, I_{OH} = Max	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.4	V
I_{IZ}	Input current for outputs in high impedance	D0-D15, HD0-HD7	Bus holders enabled, DV_{DD} = MAX, V_I = V_{SS} to DV_{DD}	-50		50	µA
		All other inputs	CV_{DD} = MAX, V_I = V_{SS} to DV_{DD}	-5		5	
I_I	Input current	X2/CLKIN	V_I = V_{SS} to DV_{DD}	-40		40	µA
		TRST		-5		300	
		HPIENA		-5		300	
		TMS, TCK, TDI, HPI†		-300		5	
		All other input-only pins		-5		5	
I_{cc}	Supply current, 3.3V		DV_{DD} = 3.3 V, f_{clock} = 40 MHz, T_C = 25°C				mA
I_{core}	Supply current, 1.5V		DV_{DD} = 1.5 V, f_{clock} = 40 MHz, T_C = 25°C				mA
I	Supply current, standby		IDLE2				mA
I	Supply current, standby		IDLE3				mA
I_{C1}	Supply current, C1A5V		internal DAA active				
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

† HPI input signals except for HPIENA

switching characteristics

In the standard configuration, the oscillator frequency (or optionally the CLKIN input frequency) is 14.7456 MHz ±50 ppm. An internal PLL multiplies this by 8, giving 117.9648 MHz or a cycle time ($t_{c(CO)}$) of 8.5 ns. This frequency appears on CLKOUT.

In the following sections, many timing parameters are defined in terms of a parameter H which is 0.5 $t_{c(CO)}$. For the standard configuration, H = 4.24 ns. See *Clock* on page 13 and *Mode Selection* on page 13 for additional information on clock options.

The HPI interface, Reset, and interrupt can be completely asynchronous to CLKOUT.

Table 16. Reset and Interrupt Timings†

PARAMETER		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, $\overline{\text{RESET}}$ after CLKOUT low	0		ns
$t_{h(INT)}$	Hold time, INTn after CLKOUT low‡	0		ns
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RESET}}$ low§	4H+5		ns
$t_{w(INTH)S}$	Pulse duration, INTn high (synchronous)	2H+7		ns
$t_{w(INTH)A}$	Pulse duration, INTn high (asynchronous)	4H		ns
$t_{w(INTL)S}$	Pulse duration, INTn low (synchronous)	2H+7		ns
$t_{w(INTL)A}$	Pulse duration, INTn low (asynchronous)	4H		ns
$t_{su(INT)}$	Setup time, INTn, $\overline{\text{RESET}}$ before CLKOUT low	8	10	ns

† Note that $\overline{\text{RESET}}$ may cause a change in clock frequency, therefore changing the value of H.
‡ The external interrupt INTn is synchronized to the core CPU by way of a two-flip-flop synchronizer which samples the input with consecutive falling edges of CLKOUT. The input to the interrupt pin is required to represent a 1-0-0 sequence at the timing that is corresponding to three CLKOUT sampling sequences.
§ If the PLL mode is selected, then at power-on sequence, $\overline{\text{RESET}}$ must be held low for at least 50 ms to ensure synchronization and lock-in of the PLL.

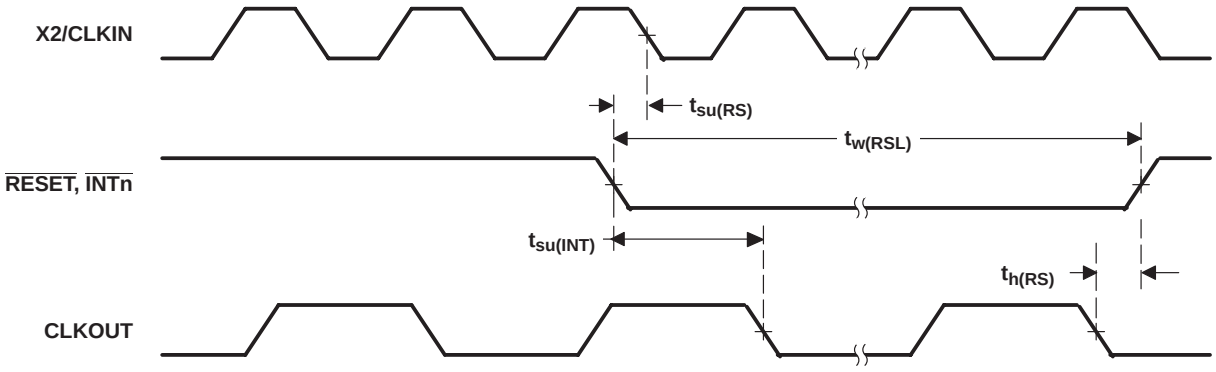


Figure 10. Reset and Interrupt Timing

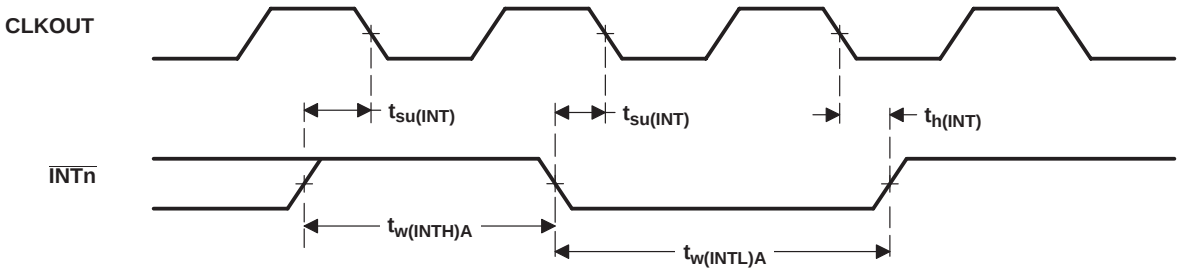


Figure 11. Interrupt Timing

HPI timing

Switching characteristics over recommended operating conditions (see notes A, B, C) [H = 0.5$t_{c(CO)}$]. See Figure 12, Figure 13, and Figure 14).

NOTES: A. DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$ and $\overline{HDS2}$.
B. HDx refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.)
C. DMAC stands for direct memory access (DMA) controller. The HPI shares the internal DMA bus with the DMAC, thus HPI access times are affected by DMAC activity.

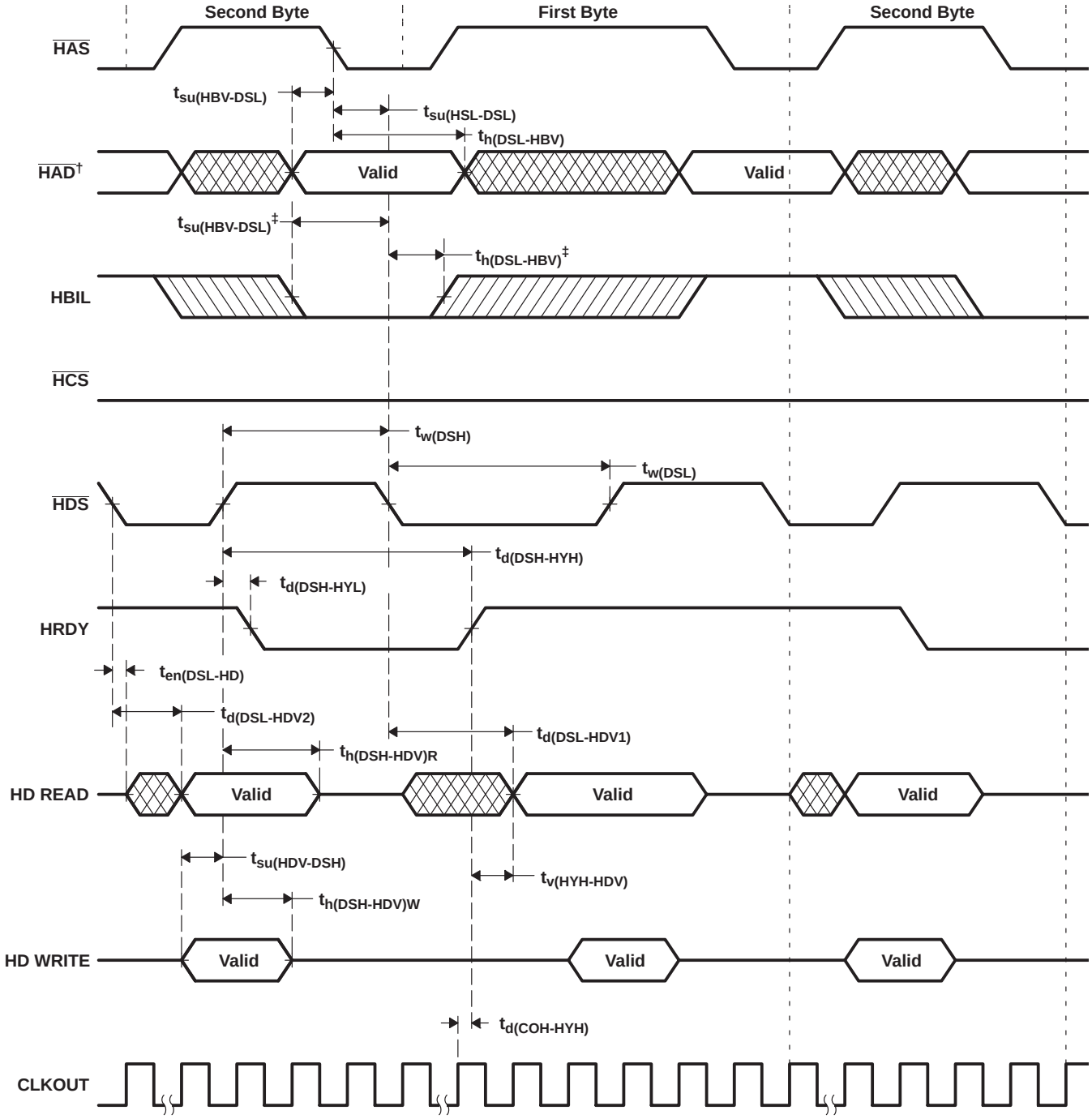
Table 17. HPI Timing

PARAMETER			MIN	MAX	UNIT
$t_{en(DSL-HD)}$	Enable time, HD driven from DS low		2	15	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HDx valid for first byte of an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)}$ < 18H		18H+15 – $t_{w(DSH)}$	ns
		Case 1b: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} \geq$ 18H		15	ns
		Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)}$ < 10H		10H+15 – $t_{w(DSH)}$	ns
		Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \geq$ 10H		15	ns
		Case 3: Register accesses		15	ns
$t_{d(DSL-HDV2)}$	Delay time, DS low to HDx valid for second byte of an HPI read			15	ns
$t_{h(DSH-HDV)R}$	Hold time, HDx valid after DS high, for a HPI read		3	5	ns
$t_{v(HYH-HDV)}$	Valid time, HDx valid after HRDY high			4	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low†			9	ns
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high	Case 1: Memory accesses when DMAC is active		18H+10	ns
		Case 2: Memory accesses when DMAC is inactive		10H+10	ns
		Case 3: Write accesses to HPIC register‡		6H+10	ns
$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ low/high to HRDY low/high			8	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT high to HRDY high			10	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT high to HINT change			10	ns
$t_{su(HBV-DSL)}$	Setup time, HBIL valid before DS low		10		ns
$t_{h(DSL-HBV)}$	Hold time, HBIL valid after DS low		5		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before DS low		5		ns
$t_{w(DSL)}$	Pulse duration, DS low		20		ns
$t_{w(DSH)}$	Pulse duration, DS high		10		ns
$t_{su(HDV-DSH)}$	Setup time, HDx valid before DS high, HPI write		5		ns
$t_{h(DSH-HDV)W}$	Hold time, HDx valid after DS high, HPI write		3		ns

† The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.
‡ This timing applies when writing a one to the DSPINT bit or HINT bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.

ADVANCE INFORMATION

HPI timing (continued)



† HAD refers to HCNTL0, HCNTL1, and HR/W
‡ When HAS not used (HAS always high.)

Figure 12. Using HDS to Control Accesses (HCS Always Low)

HPI timing (continued)

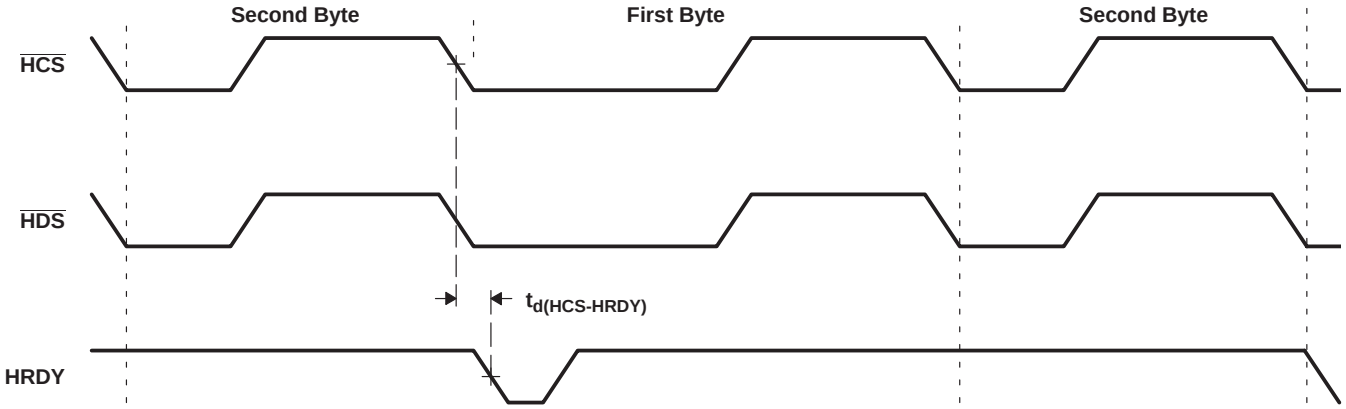


Figure 13. Using $\overline{\text{HCS}}$ to Control Accesses

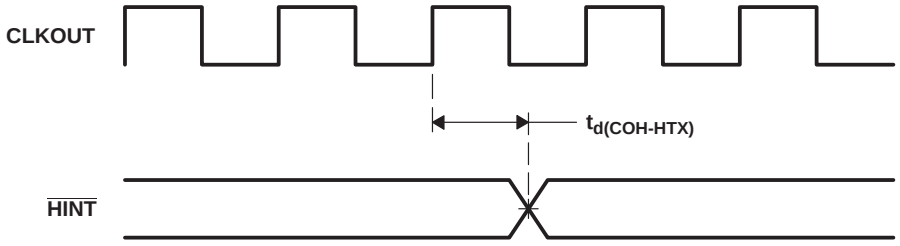
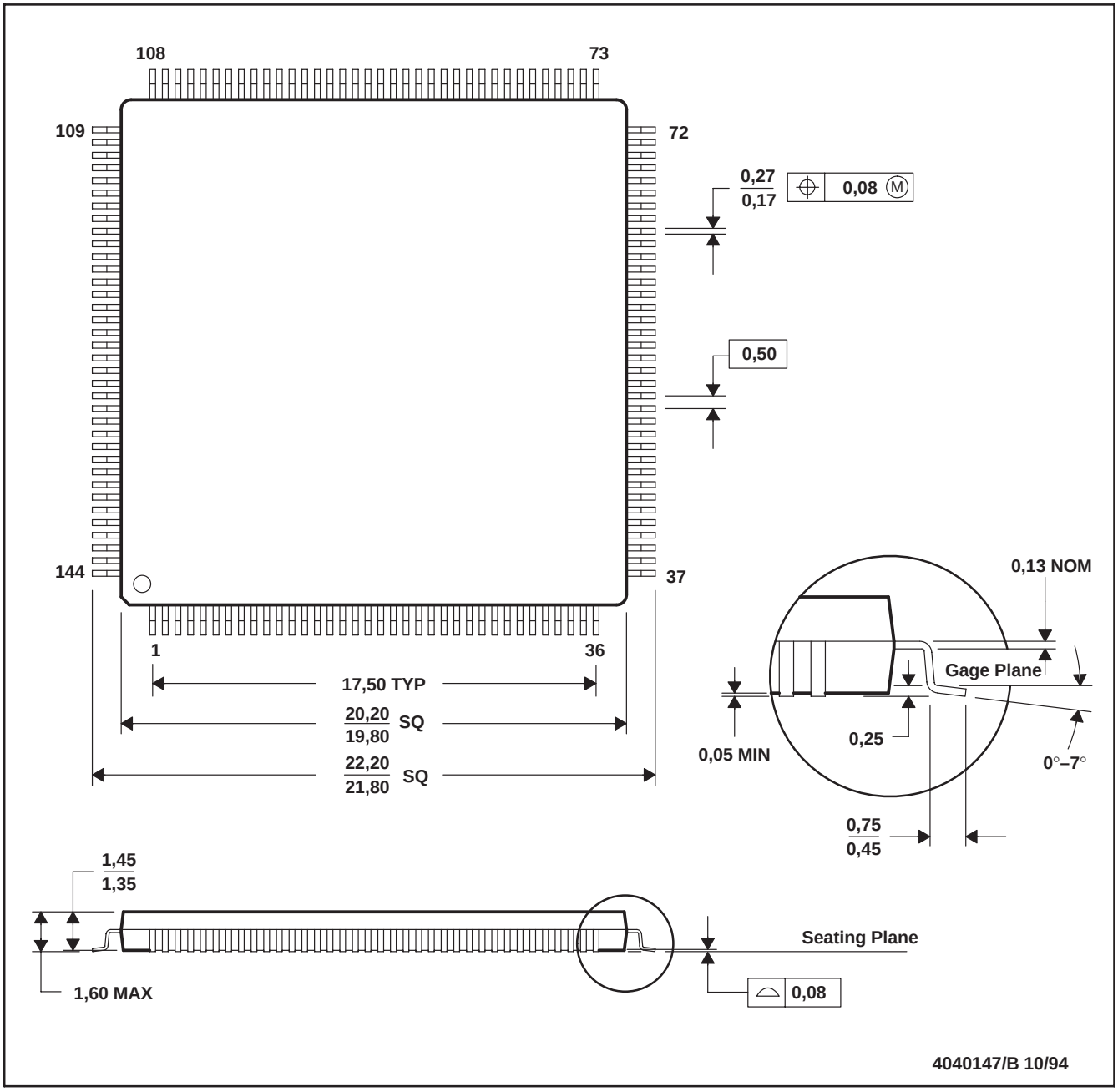


Figure 14. $\overline{\text{HINT}}$ Timing

ADVANCE INFORMATION

MECHANICAL DATA

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



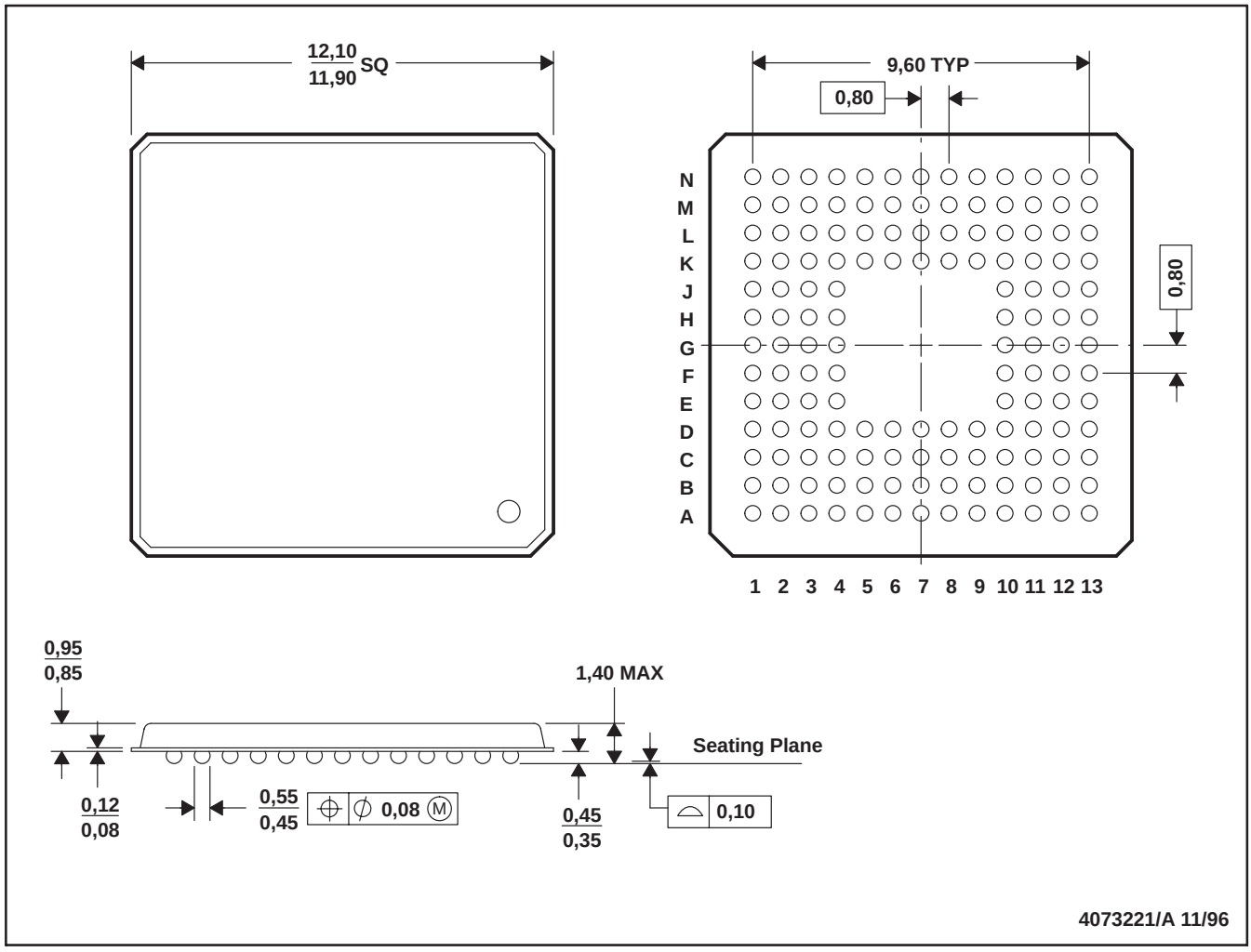
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	56
$R_{\Theta JC}$	5

MECHANICAL DATA

GGU (S-PBGA-N144) **PLASTIC BALL GRID ARRAY PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Thermal Resistance Characteristics

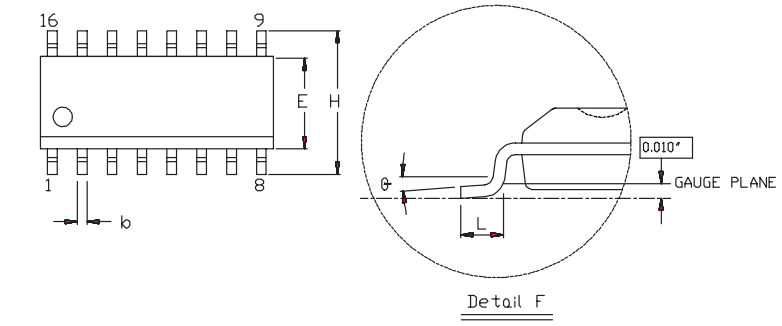
PARAMETER	°C/W
$R_{\Theta JA}$	38
$R_{\Theta JC}$	5

ADVANCE INFORMATION

MicroStar BGA is a trademark of Texas Instruments Incorporated.

MECHANICAL DATA

PCT308W **16-PIN SMALL OUTLINE PLASTIC PACKAGE (SOIC)**



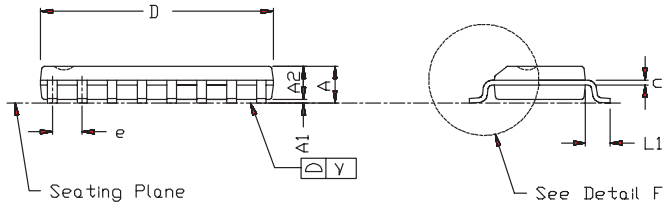


Table 18. Package Diagram Dimensions

CONTROLLING DIMENSION: MM				
SYMBOL	**INCHES**		**MILLIMETERS**	
	MIN	**MAX**	**MIN**	**MAX**
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.051	0.059	1.30	1.50
b	0.013	0.020	0.330	0.51
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC	—	1.27 BSC	—
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
L1	0.042 BSC	—	1.07 BSC	—
γ	—	0.004	—	0.10
θ	0°	8°	0°	8°