- **Complete Discrete Multitone (DMT)-Based Asymmetric Digital Subscriber Line (ADSL) Coder/Decoder (Codec) Solution**
- **Complies With ANSI Std T1.413, Issue 2 and ITU Std G.992.1**
- **Supports up to 8-Mbit/s Downstream and 800-kbit/s Upstream Duplex**
- **Integrated 14-Bit Converters for Transmitter/Echo-Canceller/Receiver (TX/EC/RX)**
- **Integrated 12-Bit Digital-to-Analog Converter (DAC) for Voltage-Controlled Oscillator (VCXO) Control**
- **Integrated TX/EC/RX Channel Filters**
- **Integrated TX/EC/RX Attenuation/Gain**
- **Integrated Voltage Reference**
- **Selectable 2.2-Mega Samples Per Second (MSPS) or 4.4-MSPS Parallel Data Transfer Rate**
- **Serial-Configuration Port**
- **Eight General-Purpose (GP) Output Terminals**
- **Single 3.3-V ±10% Supply Operation**
- **Hardware/Software Power Down**
- **–40°C to 85°C Operation**
- **Packaged in 100-Pin Plastic Quad Flatpack**

description

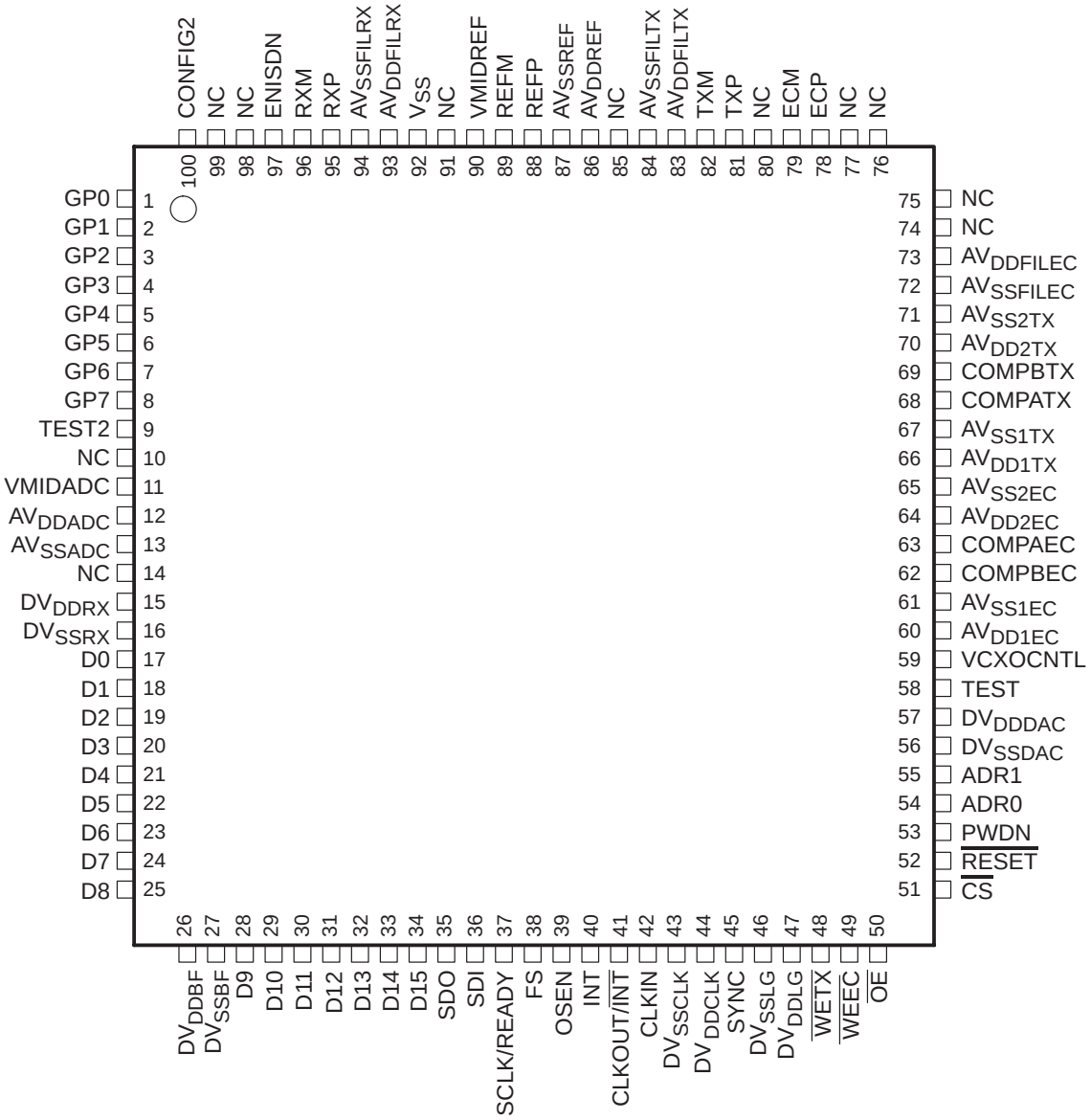
The TLV320AD13A is a high-speed coder/decoder (codec) for remote terminal (RT)-side modems that supports ADSL over integrated services digital network (ISDN) solution. The TLV320AD13A is a low-power device composed of five major functional groups for transmit (TX), receive (RX), clock, reference, and host interface. It is designed to work with the Texas Instruments (TI™) TNETD2022D central office (CO)-side codec for ISDN.

The TX channel consists of a 138-kHz to 276-kHz digital bandpass filter, a 14-bit high-speed digital-to-analog converter (DAC), a 276-kHz analog low-pass filter (LPF), a TX attenuator, and an echo-cancellation (EC) channel. The RX channel consists of a 1.104-MHz digital LPF, a 1.104-MHz analog LPF, a frequency equalizer, and a programmable-gain amplifier (PGA). The clock circuit divides a 35.328-MHz frequency from an external voltage-controlled oscillator (VCXO) down to the necessary frequencies used throughout the device. The frequency of the external VCXO is controlled by a 12-bit onboard voltage-output DAC. An onboard reference circuit generates a 1.5-V reference for the converters.

The device has a parallel port for data transfer and a serial port for control. The parallel port is 16 bits wide and is reserved for moving data between the codec and a host transceiver such as the TI C6x DSP. Configuration is done via a serial port. The device can be powered down via a dedicated pin, or through software control, to reduce heat dissipation. Additionally, there is a general-purpose (GP) port consisting of eight output terminals for control of external circuitry.

The TLV320AD13A codec is characterized for operation in the temperature range of –40°C to 85°C and is available in a 100-pin PQFP (PZ) package.

PZ PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADR0 ADR1	54 55	I	Serial-port chip ID address. ADR0 is the least significant bit.
AV_{DDADC}	12	I	RX-channel analog power supply
$AV_{DDFILEC}$	73	I	EC-channel filter analog power-supply return
$AV_{DDFILRX}$	93	I	RX-channel filter analog power supply
$AV_{DDFILTX}$	83	I	TX-channel filter analog power supply
AV_{DDREF}	86	I	Reference analog power supply
AV_{DD1EC}	60	I	EC-channel analog power-supply 1
AV_{DD2EC}	64	I	EC-channel analog power-supply 2
AV_{DD1TX}	66	I	TX-channel analog power-supply 1
AV_{DD2TX}	70	I	TX-channel analog power-supply 2
AV_{SSADC}	13	I	RX-channel analog power-supply return
$AV_{SSFILEC}$	72	I	EC-channel filter analog power-supply return
$AV_{SSFILRX}$	94	I	RX-channel filter analog power-supply return
$AV_{SSFILTX}$	84	I	TX-channel filter analog power-supply return
AV_{SSREF}	87	I	Reference analog power-supply return
AV_{SS1EC}	61	I	EC-channel analog power-supply return 1
AV_{SS2EC}	65	I	EC-channel analog power-supply return 2
AV_{SS1TX}	67	I	TX-channel analog power-supply return 1
AV_{SS2TX}	71	I	TX-channel analog power-supply return 2
CLKIN	42	I	35.328-MHz VCXO clock input
CLKOUT/$\overline{INT}$	41	O	If CONFIG2 is low, this terminal is 4.416-MHz clock output. If CONFIG2 is high, this terminal functions as $\overline{INT}$.
COMPAEC	63	O	EC-channel decoupling cap input A (add 500-pF ceramic capacitor between this terminal and AV_{DD1EC})
COMPATX	68	O	TX-channel decoupling cap input A (add 500-pF ceramic capacitor between this terminal and AV_{DD1TX})
COMPBEC	62	O	EC-channel decoupling cap input B (add 1-μF ceramic capacitor between this terminal and AV_{DD1EC})
COMPBTX	69	O	TX-channel decoupling cap input B (add 1-μF ceramic capacitor between this terminal and AV_{DD1TX})
CONFIG2	100	I	I/O configuration. A high on this terminal redefines the function of terminals 37 and 41. The default state of this terminal is low. Refer to Figure 2 for details.
$\overline{CS}$	51	I	Parallel-port chip select
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	(MSB) 34 33 32 31 30 29 28 25 24 23 22 21 20 19 18 17 (LSB)	I/O	Parallel-port data. D0 is the least significant bit (LSB) (drive up to 50 pF).

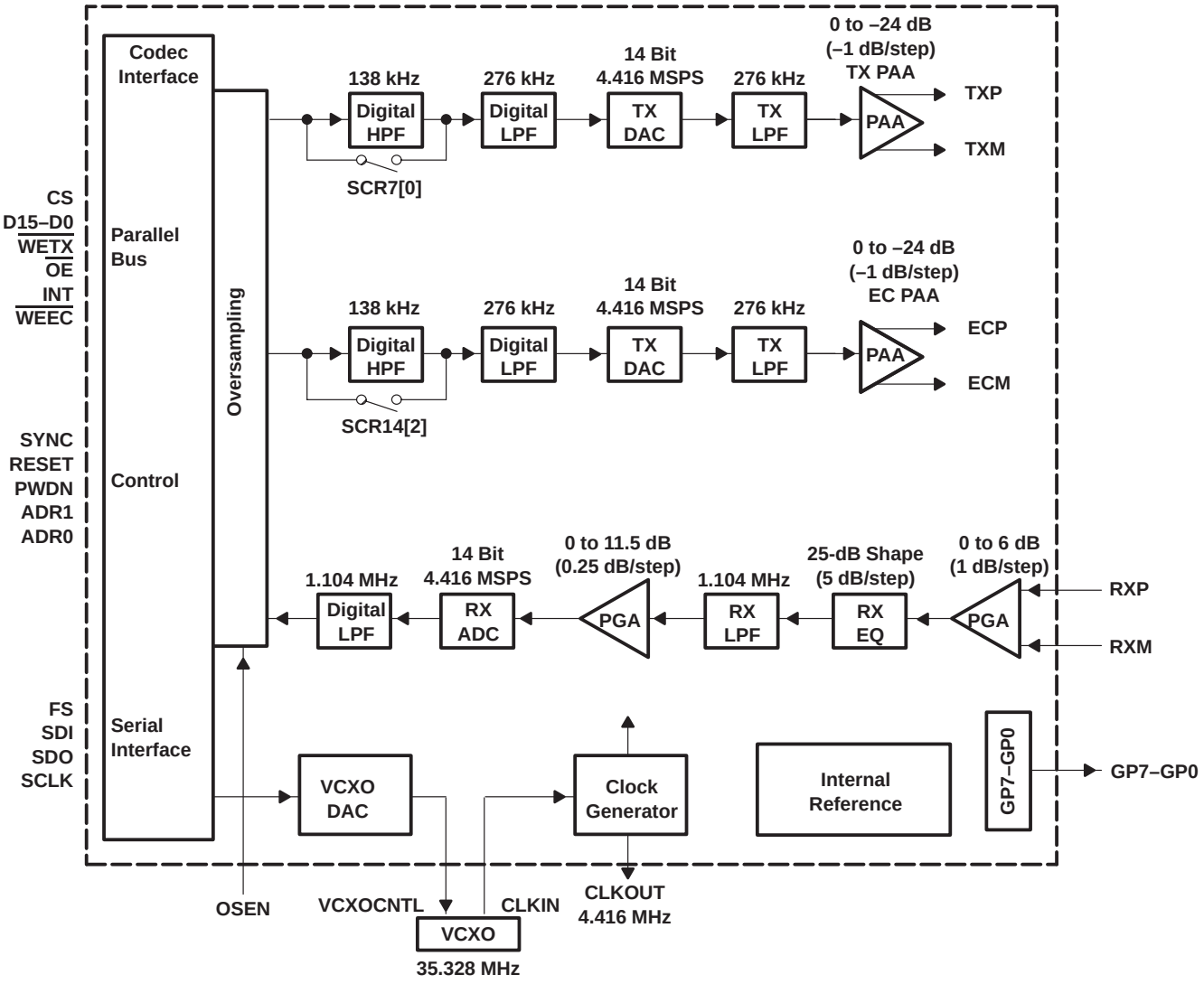
Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DV_{DDBF}	26	I	Digital I/O buffer power supply
DV_{DDCLK}	44	I	Digital-clock power supply
DV_{DDDAC}	57	I	Digital power supply for TX channel
DV_{DDLG}	47	I	Digital-logic power supply
DV_{DDRX}	15	I	RX-channel digital power supply
DV_{SSBF}	27	I	Digital I/O buffer power-supply return
DV_{SSCLK}	43	I	Digital clock power-supply return
DV_{SSDAC}	56	I	Digital power-supply return for TX channel
DV_{SSLG}	46	I	Digital logic power-supply return
DV_{SSRX}	16	I	RX-channel digital power-supply return
ECM	79	O	EC output minus
ECP	78	O	EC output plus
ENISDN	97	I	ISDN configuration input. This terminal must be tied high for ISDN operation. The terminal setting should be done before the chip is reset. The default of the terminal is low.
FS	38	I	Frame synchronization input
GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0	8 7 6 5 4 3 2 1	O	General-purpose output port
INT	40	O	Data-rate clock (INT is 4.4 MHz when OSEN = 1, 2.2 MHz when OSEN = 0)
NC	10, 14, 74, 75, 76, 77, 80, 85, 91, 98, 99		No connection. All NC terminals should be left open.
$\overline{OE}$	50	I	Parallel-port output enable
OSEN	39	I	Oversampling enable. OSEN = 1 enables oversampling mode (INT = 4.4 MHz).
PWDN	53	I	Power down. When PWDN = 0, the device is in normal operating mode. When PWDN = 1, the device is in power-down mode.
REFM	89	O	Decoupling reference voltage minus (add 10-μF tantalum and 0.1-μF ceramic capacitors between this terminal and AV_{SSREF}). The nominal dc voltage at this terminal is 0.5 V.
REFP	88	O	Decoupling reference voltage plus (add 10-μF tantalum and 0.1-μF ceramic capacitors between this terminal and AV_{SSREF}). The nominal dc voltage at this terminal is 2.5 V.
$\overline{RESET}$	52	I	Hardware system reset. An active low level resets the device.
RXM	96	I	RX input minus. RXM is self biased to $AV_{DDFILRX}/2$.
RXP	95	I	RX input plus. RXP is self biased to $AV_{DDFILRX}/2$.
SCLK/READY	37	O	If CONFIG2 is low, this terminal is serial clock output. If CONFIG2 is high, it indicates the period in which parallel data can be transferred.
SDI	36	I	Serial data input
SDO	35	O	Serial data output
SYNC	45	I	Synchronization pulse for clock synchronization (see Figure 3). A high pulse to this terminal synchronizes the clock operation. Tie SYNC to DV_{SSLG} for auto-synchronization.
TEST	58	I	Test mode terminal. Tie this terminal low for normal operation.
TEST2	9	I	Test mode terminal. Tie this terminal low for normal operation.
TXM	82	O	TX output minus

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TXP	81	O	TX output plus
VCXOCNTL	59	O	VCXO DAC control output
VMIDADC	11	O	Decoupling 1.5 V for analog-to-digital converter (ADC) (add 10-µF tantalum and 0.1-µF ceramic capacitors between this terminal and AV_{SSADC}).
VMIDREF	90	O	Decoupling 1.5-V reference voltage (add 10-µF tantalum and 0.1-µF ceramic capacitors between this terminal and AV_{SSREF}).
V_{SS}	92	I	Substrate. Connect V_{SS} to analog ground.
$\overline{WEEC}$	49	I	Write enable for EC channel
$\overline{WETX}$	48	I	Write enable for TX channel

functional block diagram



functional description

TX channel/EC channel

The TX channel is powered by a high-performance DAC. This is a 4.416-MHz, 14-bit DAC that provides 16× oversampling to reduce DAC noise so that it does not contribute to the receive noise. An LPF limits its output to 276 kHz. A programmable attenuator (PAA), with a range of 24 dB in 1-dB steps, drives the output into the external ADSL line driver. The TX high-pass filter (HPF) can be bypassed.

A second transmitter is used to perform pre-EC. This analog EC helps reduce the dynamic-range requirements of the RT receiver. It has the same function as the first transmitter channel. It drives a separate external line driver to perform the cancellation.

RX channel

The RX channel has two PGAs and an equalizer to match the loop loss and flatten signal-to-noise ratio (SNR). This results in a reduction in the dynamic-range requirement for the high-resolution ADC. The RX channel also has a 1.104-MHz LPF with a 4.416-mega samples per second (MSPS) 14-bit ADC to provide a 2× oversampling (OSEN = 1).

VCXO-control DAC

A 12-bit serial DAC is used to control the external 35.328-MHz VCXO that provides the system clock to the codec. In a typical application, the update rate of the DAC is about 4 kHz, depending on the ADSL frame rate. The host transceiver initiates the update through the serial interface. The two 8-bit registers, SCR4 and SCR5 (each 2s complement), are used to generate the 12-bit code for the DAC. This requires the use of 16 bits to obtain a 12-bit number. The lower four bits of the most significant bit register (SCR5[3:0]) are added (2s complement) to the higher four bits of the least significant bit register (SCR4[7:4]). Refer to Figure 1 for code generation. The updated code is sent to the DAC two SCLKs after the SCR4 register is received. If SCR5 does not need to be updated, only one write cycle to SCR4 is needed to update the VCXO DAC. In this case, the lower eight bits of the 12-bit word are updated.

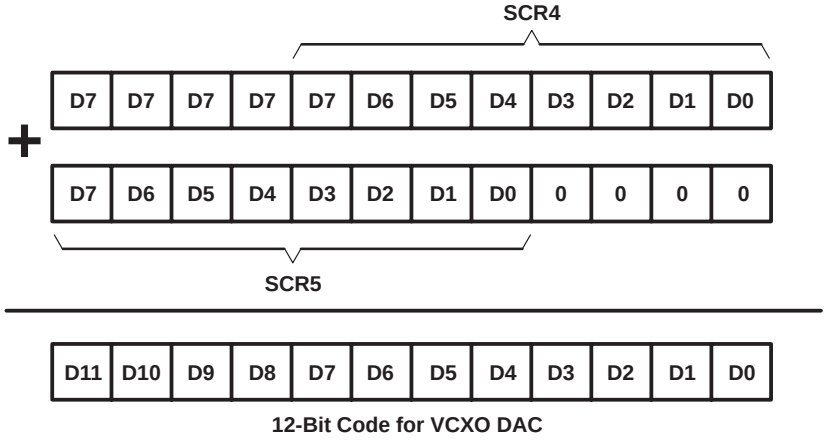


Figure 1. 12-Bit Code Generation for VCXO DAC

clock generation

The clock-generation block provides the necessary clock signals for the device, with minimum skew and jitter. This is closely dependent on the performance of the external VCXO. The external VCXO specifications are:

- 3.3-V supply
- 35.328 MHz, ±50 PPM
- Minimum duty cycle is 60/40 (50/50 is optimum).

clock generation (continued)

Table 1 describes the major clocks generated internally.

Table 1. Clock Description

CLOCK	FREQUENCY (MHz)	
	OSEN = 0	OSEN = 1
INT	2.208	4.416
CLKOUT	4.416	4.416
SCLK	4.416	4.416

interrupt (INT)

INT to the host processor is 4.416 MHz when OSEN = 1 and 2.208 MHz when OSEN = 0.

serial clock (SCLK)

SCLK used in the serial codec interface has a fixed frequency of 4.416 MHz and is synchronous with the master clock (35.328 MHz).

clock output (CLKOUT)

CLKOUT is 4.416 MHz and is synchronous with the master clock (35.328 MHz).

interface

parallel interface

The device has a 16-bit parallel interface for transmitter and receiver data. Strobes $\overline{OE}$, $\overline{WETX}$, $\overline{WEEC}$, and $\overline{CS}$ from the host are edge-triggered signals. Incoming data is registered on the rising edge of $\overline{WETX}$/$\overline{WEEC}$ as long as it meets the minimum setup and hold times. Output data from the codec is enabled with delay after the falling edge of the $\overline{OE}$ strobe, and disabled after the rising edge of the $\overline{OE}$ strobe. Two kinds of interrupt (INT and $\overline{INT}$) to the host controller are generated onboard. The INT cycle time is hardware configurable for either 4.416 MHz (2× oversampling mode, OSEN = 1) or 2.208 MHz (1× oversampling mode, OSEN = 0). SYNC is used to synchronize the operation between the codec and the host transceiver. SCLK/READY is used to indicate the parallel data transfer period in configuration mode 2 (see Figure 2).

The 16-bit data is left justified, i.e., D15 is the most significant bit (MSB) and D0 is the least significant bit (LSB). The TX and RX data contains 16 valid bits. All 16 bits are used in the digital filtering.

keep-out zones (KOZs)

The last CLKIN cycle before a transition of CLKOUT is defined as a KOZ. These zones are reserved for the sampling of analog signals. All digital I/O (except CLKIN) should be quiet during these KOZs.

oversampling mode

OSEN selects 2× oversampling mode (INT running at 4.416 MHz), or 1× oversampling mode (INT running at 2.208 MHz) for receive-channel ADC.

serial interface

The serial port is used for codec configuration and register reading. The word length is 16 bits. Two hardware configuration terminals, ADR[1:0] are used to configure the device ID. Up to four codecs can be identified for each host transceiver peripherals port.

The master codec (ADR[1:0] = [0,0]) provides the SCLK to the host processor. The SCLK terminals on the other codecs are left unconnected. All the codecs in a multicodec system should be synchronized so that their SCLK signals are in phase – even though the signals themselves are not being used. This ensures that, even though the individual SCLK signals of each codec are not being used, the data is being latched into the codec properly.

serial interface (continued)

The SCLK is a continuously running 4.416-MHz fixed-frequency clock, synchronized to the codec internal events and CLKOUT (to the host) so that the KOZs can be monitored. A host transceiver can drive the frame synchronization (FS) (synchronized to the CLKOUT from the codec) into the codec to initiate a 16-bit serial I/O frame.

If SCR5 needs to be updated, the host controller must first write the SCR5 register of the VCXO DAC data and then the SCR4 register of the VCXO DAC data. The VCXO DAC gets updated only after the SCR4 register is written.

GP port

The GP port provides eight outputs, each capable of delivering 0.5 mA, for control of external circuitry such as LEDs, gain control, and power down.

voltage reference

The built-in reference provides the needed reference voltage and current to individual analog blocks. It also is brought out to external terminals for noise decoupling.

register programming

See Figure 4 for timing and format details.

Table 2. System Control Registers (SCRs)

REGISTER		MODE	DEFAULT VALUE	FUNCTION
NAME	ADDRESS S3, S2, S1, S0			
SCR0	0000	R	00000000	
		W		D0: Software reset (self clearing)
SCR1	0001	R/W	00000000	D[4:0] = TX channel PAA gain select. D[4:0] = 00000 for 0 dB, D[4:0] = 11000 for –24 dB.
SCR2	0010	R/W	00000000	D[5:0] = RX PGA2. D[5:0] = 000000 for 0 dB, D[5:0] = 101110 for 11.5 dB.
SCR3	0011	R/W	00000000	D[2:0] = RX EQ slope select. D[2:0] = 000 for 0 dB/MHz, D[2:0] = 001 for 5 dB/MHz, D[2:0] = 101 for 25 dB/MHz
SCR4	0100	R/W	00000000	D[7:0] = VCXODAC (low 8 bits of 12-bit DAC code)
SCR5	0101	R/W	00000000	D[7:0] = VCXODAC (high 8 bits of 12-bit DAC code)
SCR6	0110	R/W	00000000	D[7:0] = GP[7:0]
SCR7	0111	R/W	00000000	Miscellaneous control (set to 1 to enable) D0: Bypass TX ISDN HPF (138 kHz) D1: Software power-down RX channel D2: Software power-down TX channel D3: Analog loopback (TX channel) D4: Digital loopback (TX and EC channel) D5: Parallel interface (read back) test-mode enable D6: EC channel power down D7: EC analog loopback
SCR8	1000	R/W	00000000	D[4:0] = EC channel PAA gain select. D[4:0] = 00000 for 0 dB. D[4:0] = 11000 for –24 dB.
SCR9	1001	R/W	00000000	D[7:0] = RX offset low
SCR10	1010	R/W	00000000	D[7:0] = RX offset high
SCR11	1011	R/W	00000000	D[4:0] = TX digital gain select. The gain range is –1 dB to 1 dB in 0.1-dB steps. D[4:0] = 00000 for 0 dB D[4:0] = 00001 for 0.1 dB. D[4:0] = 01010 for 1 dB. D[4:0] = 10000 for –1 dB. D[4:0] = 11001 for –0.1 dB.
SCR12	1100	R/W	00000000	D[2:0] = RX PGA1. D[2:0] = 000 for 0 dB. D[2:0] = 110 for 6 dB.
SCR13	1101	R/W	00000000	D[4:0] = EC digital gain select. The gain range is –1 dB to 1 dB in 0.1-dB steps. D[4:0] = 00000 for 0 dB. D[4:0] = 00001 for 0.1 dB D[4:0] = 01010 for 1 dB. D[4:0] = 10000 for –1 dB. D[4:0] = 11001 for –0.1 dB.
SCR14	1110	R/W	00000000	D0: Reserved D1: enable FIFO (first in, first out) (see Note 1) D2: bypass EC ISDN HPF (138 kHz) D3: ECNULL. When D3 is set to 1, ECP and ECM are connected to weakly driven mid supply. It can be used only during EC power-down mode.

NOTE 1: It is a two-stage FIFO buffer, and can store up to two write samples if asynchronous write operation is required.

Table 2. System-Control Registers (SCRs) (Continued)

SCR0 – SYSTEM CONTROL
(address: 0000b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	1	01	Software reset (self clearing). All control registers are set to reset content.

SCR1 – TX PAA CONTROL
(address: 0001b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	TX PAA gain = 0 dB
0	0	0	0	0	0	0	1	01	TX PAA gain = –1 dB
0	0	0	0	0	0	1	0	02	TX PAA gain = –2 dB
0	0	0	0	0	0	1	1	03	TX PAA gain = –3 dB
0	0	0	0	0	1	0	0	04	TX PAA gain = –4 dB
0	0	0	0	0	1	0	1	05	TX PAA gain = –5 dB
0	0	0	0	0	1	1	0	06	TX PAA gain = –6 dB
0	0	0	0	0	1	1	1	07	TX PAA gain = –7 dB
0	0	0	0	1	0	0	0	08	TX PAA gain = –8 dB
0	0	0	0	1	0	0	1	09	TX PAA gain = –9 dB
0	0	0	0	1	0	1	0	0A	TX PAA gain = –10 dB
0	0	0	0	1	0	1	1	0B	TX PAA gain = –11 dB
0	0	0	0	1	1	0	0	0C	TX PAA gain = –12 dB
0	0	0	0	1	1	0	1	0D	TX PAA gain = –13 dB
0	0	0	0	1	1	1	0	0E	TX PAA gain = –14 dB
0	0	0	0	1	1	1	1	0F	TX PAA gain = –15 dB
0	0	0	1	0	0	0	0	10	TX PAA gain = –16 dB
0	0	0	1	0	0	0	1	11	TX PAA gain = –17 dB
0	0	0	1	0	0	1	0	12	TX PAA gain = –18 dB
0	0	0	1	0	0	1	1	13	TX PAA gain = –19 dB
0	0	0	1	0	1	0	0	14	TX PAA gain = –20 dB
0	0	0	1	0	1	0	1	15	TX PAA gain = –21 dB
0	0	0	1	0	1	1	0	16	TX PAA gain = –22 dB
0	0	0	1	0	1	1	1	17	TX PAA gain = –23 dB
0	0	0	1	1	0	0	0	18	TX PAA gain = –24 dB
–	–	–	–	–	–	–	–	19–FF	TX PAA gain = –24 dB

Table 2. System-Control Registers (SCRs) (Continued)

SCR2 – RX PGA2 CONTROL
(address: 0010b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA2 = 0 dB
0	0	0	0	0	0	0	1	01	RX PGA2 = 0.25 dB
0	0	0	0	0	0	1	0	02	RX PGA2 = 0.5 dB
0	0	0	0	0	0	1	1	03	RX PGA2 = 0.75 dB
0	0	0	0	0	1	0	0	04	RX PGA2 = 1.0 dB
0	0	0	0	0	1	0	1	05	RX PGA2 = 1.25 dB
0	0	0	0	0	1	1	0	06	RX PGA2 = 1.5 dB
0	0	0	0	0	1	1	1	07	RX PGA2 = 1.75 dB
0	0	0	0	1	0	0	0	08	RX PGA2 = 2.0 dB
0	0	0	0	1	0	0	1	09	RX PGA2 = 2.25 dB
0	0	0	0	1	0	1	0	0A	RX PGA2 = 2.5 dB
0	0	0	0	1	0	1	1	0B	RX PGA2 = 2.75 dB
0	0	0	0	1	1	0	0	0C	RX PGA2 = 3.0 dB
0	0	0	0	1	1	0	1	0D	RX PGA2 = 3.25 dB
0	0	0	0	1	1	1	0	0E	RX PGA2 = 3.5 dB
0	0	0	0	1	1	1	1	0F	RX PGA2 = 3.75 dB
0	0	0	1	0	0	0	0	10	RX PGA2 = 4.0 dB
0	0	0	1	0	0	0	1	11	RX PGA2 = 4.25 dB
0	0	0	1	0	0	1	0	12	RX PGA2 = 4.5 dB
0	0	0	1	0	0	1	1	13	RX PGA2 = 4.75 dB
0	0	0	1	0	1	0	0	14	RX PGA2 = 5.0 dB
0	0	0	1	0	1	0	1	15	RX PGA2 = 5.25 dB
0	0	0	1	0	1	1	0	16	RX PGA2 = 5.5 dB
0	0	0	1	0	1	1	1	17	RX PGA2 = 5.75 dB
0	0	0	1	1	0	0	0	18	RX PGA2 = 6.0 dB
0	0	0	1	1	0	0	1	19	RX PGA2 = 6.25 dB
0	0	0	1	1	0	1	0	1A	RX PGA2 = 6.5 dB
0	0	0	1	1	0	1	1	1B	RX PGA2 = 6.75 dB
0	0	0	1	1	1	0	0	1C	RX PGA2 = 7.0 dB
0	0	0	1	1	1	0	1	1D	RX PGA2 = 7.25 dB
0	0	0	1	1	1	1	0	1E	RX PGA2 = 7.5 dB
0	0	0	1	1	1	1	1	1F	RX PGA2 = 7.75 dB
0	0	1	0	0	0	0	0	20	RX PGA2 = 8.0 dB
0	0	1	0	0	0	0	1	21	RX PGA2 = 8.25 dB
0	0	1	0	0	0	1	0	22	RX PGA2 = 8.5 dB
0	0	1	0	0	0	1	1	23	RX PGA2 = 8.75 dB
0	0	1	0	0	1	0	0	24	RX PGA2 = 9.0 dB
0	0	1	0	0	1	0	1	25	RX PGA2 = 9.25 dB
0	0	1	0	0	1	1	0	26	RX PGA2 = 9.5 dB

Table 2. System-Control Registers (SCRs) (Continued)

SCR2 – RX PGA2 CONTROL
(address: 0010b, contents at reset: 00000000b) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	1	0	0	1	1	1	27	RX PGA2 = 9.75 dB
0	0	1	0	1	0	0	0	28	RX PGA2 = 10.0 dB
0	0	1	0	1	0	0	1	29	RX PGA2 = 10.25 dB
0	0	1	0	1	0	1	0	2A	RX PGA2 = 10.5 dB
0	0	1	0	1	0	1	1	2B	RX PGA2 = 10.75 dB
0	0	1	0	1	1	0	0	2C	RX PGA2 = 11.0 dB
0	0	1	0	1	1	0	1	2D	RX PGA2 = 11.25 dB
0	0	1	0	1	1	1	0	2E	RX PGA2 = 11.5 dB
–	–	–	–	–	–	–	–	2F–FF	RX PGA2 = 11.5 dB

SCR3 – RX EQ CONTROL
(address: 0011b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX EQ = 0 dB/MHz
0	0	0	0	0	0	0	1	01	RX EQ = 5 dB/MHz
0	0	0	0	0	0	1	0	02	RX EQ = 10 dB/MHz
0	0	0	0	0	0	1	1	03	RX EQ = 15 dB/MHz
0	0	0	0	0	1	0	0	04	RX EQ = 20 dB/MHz
0	0	0	0	0	1	0	1	05	RX EQ = 25 dB/MHz
–	–	–	–	–	–	–	–	06–FF	RX EQ = 25 dB/MHz

SCR4 – VCXO DATA
(address: 0100b, contents at reset: 00000000b)

SCR5 – VCXO DATA
(address: 0101b, contents at reset: 00000000b)

The following page shows some representative VCXO DAC analog outputs. The read-back values of SCR4 and SCR5 are different from the values written to the registers.

Table 2. System-Control Registers (SCRs) (Continued)

VCXO DAC DIGITAL-ANALOG MAPPING
(representative analog outputs)

OPERATION	HEX RESULT	ANALOG OUTPUT	COMMENTS
SRC5[7:0] × 2^4 + SCR4[7:0]	0x800	0 V	Min scale
	0x801	ΔV	Just above min
	• • •	• • •	• • •
	0xFFF	2047 ΔV	Just below mid
	0x000	2048 ΔV	Mid scale
	0x001	2049 ΔV	Just above mid
	• • •	• • •	• • •
	0x7FE	4094 ΔV	Just below max
	0x7FF	4095 ΔV	Max scale

NOTES: 2. Δ = (3/4095) V
3. The analog output is computed as follows:
((SCR%[7:0] * 2^4 + SCR4[7:0])) + 2048(decimal) * Δ

Examples:

- Positive SCR5 + positive SCR4

  (0x24 * 2^4 + 0x42) = 0x240 + 0x42 = 0x282 = 642 decimal
  Analog output = (642 + 2048) ΔV = 2690 ΔV = 1.971 V
  The read-back values of SCR5 and SCR4 are 0x02 and 0x82.

- Positive SCR5 + negative SCR4

  (0x24 * 2^4 + 0xC2) = 0x240 + 0xFC2 = 0x202 = 514 decimal
  Analog output = (514 + 2048) ΔV = 2562 ΔV = 1.877 V
  The read-back values of SCR5 and SCR4 are 0x02 and 0x02.

- Negative SCR5 + positive SCR4

  (0xA2 * 2^4 + 0x42) = 0xA20 + 0x42 = 0xA62 = –1438 decimal
  Analog output = (–1438 + 2048) ΔV = 610 ΔV = 0.447 V
  The read-back values of SCR5 and SCR4 are 0x0A and 0x62

- Negative SCR5 + negative SCR4

  (0xA2 * 2^4 + 0xC2) = 0xA20 + 0xFC2 = 0x9E2 = –1566 decimal
  Analog output = (–1566 + 2048) ΔV = 482 ΔV = 0.353 V
  The read-back values of SCR5 and SCR4 are 0x09 and 0xE2

Table 2. System-Control Registers (SCRs) (Continued)

SCR6 – GP OUTPUT DATA
(address: 0110b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0/1	–	–	–	–	–	–	–	GP7 = low(0)/high(1)
–	0/1	–	–	–	–	–	–	GP6 = low(0)/high(1)
–	–	0/1	–	–	–	–	–	GP5 = low(0)/high(1)
–	–	–	0/1	–	–	–	–	GP4 = low(0)/high(1)
–	–	–	–	0/1	–	–	–	GP3 = low(0)/high(1)
–	–	–	–	–	0/1	–	–	GP2 = low(0)/high(1)
–	–	–	–	–	–	0/1	–	GP1 = low(0)/high(1)
–	–	–	–	–	–	–	0/1	GP0 = low(0)/high(1)

SCR7 – MISCELLANEOUS CONTROL 1
(address: 0111b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
–	–	–	–	–	–	–	1	Bypass TX digital HPF (138 kHz)
–	–	–	–	–	–	1	–	Software power-down RX channel
–	–	–	–	–	1	–	–	Software power-down TX channel
–	–	–	–	1	–	–	–	Analog loopback (TX channel) (see Note 4)
–	–	–	1	–	–	–	–	Digital loopback (TX and EC channel) (see Note 5)
–	–	1	–	–	–	–	–	TX parallel interface (read back) test mode enable (see Note 6)
–	1	–	–	–	–	–	–	EC channel power down
1	–	–	–	–	–	–	–	EC analog loopback

NOTES: 4. Analog loopback: Analog outputs (TXP/TXM or ECP/ECM) are internally connected to RXP/RXM.
5. Digital loopback: RX digital output buffer (16-bit word) is internally connected to the TX/EC digital input buffer.
6. The input digital data is read back from RX output buffer without going through the DAC.

SCR8 – EC PAA CONTROL
(address: 1000b, contents at reset: 00000000b)†

† SCR8 has the same format as SCR1 (see SCR1 – TX PAA Control).

SCR9 – RX OFFSET CONTROL [7:0]
(address: 1001b, contents at reset: 00000000b)‡

SCR10 – RX OFFSET CONTROL [15:8]
(address: 1010b, contents at reset: 00000000b)‡

‡ Registers SCR9 and SCR10 are combined to form a 16-bit word in 2s complement data format. The 16-bit word is used to adjust the RX channel DC offset error. The 16-bit word is added to the 16-bit data from the RX digital filter before the data goes to the RX output buffer.

Table 2. System-Control Registers (SCRs) (Continued)

SCR11 – TX CHANNEL DIGITAL GAIN CONTROL
(address: 1011b, contents at reset: 00000000b)†

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	1	1	0	0	1	19	TX digital gain = –0.1 dB
0	0	0	1	1	0	0	0	18	TX digital gain = –0.2 dB
0	0	0	1	0	1	1	1	17	TX digital gain = –0.3 dB
0	0	0	1	0	1	1	0	16	TX digital gain = –0.4 dB
0	0	0	1	0	1	0	1	15	TX digital gain = –0.5 dB
0	0	0	1	0	1	0	0	14	TX digital gain = –0.6 dB
0	0	0	1	0	0	1	1	13	TX digital gain = –0.7 dB
0	0	0	1	0	0	1	0	12	TX digital gain = –0.8 dB
0	0	0	1	0	0	0	1	11	TX digital gain = –0.9 dB
0	0	0	1	0	0	0	0	10	TX digital gain = –1 dB
0	0	0	0	0	0	0	0	00	TX digital gain = 0 dB
0	0	0	0	0	0	0	1	01	TX digital gain = 0.1 dB
0	0	0	0	0	0	1	0	02	TX digital gain = 0.2 dB
0	0	0	0	0	0	1	1	03	TX digital gain = 0.3 dB
0	0	0	0	0	1	0	0	04	TX digital gain = 0.4 dB
0	0	0	0	0	1	0	1	05	TX digital gain = 0.5 dB
0	0	0	0	0	1	1	0	06	TX digital gain = 0.6 dB
0	0	0	0	0	1	1	1	07	TX digital gain = 0.7 dB
0	0	0	0	1	0	0	0	08	TX digital gain = 0.8 dB
0	0	0	0	1	0	0	1	09	TX digital gain = 0.9 dB
0	0	0	0	1	0	1	0	0A	TX digital gain = 1 dB
–	–	–	–	–	–	–	–	All others	Reserved (see Note 7)

† Digital gain is used to compensate the TX-channel gain error.

NOTE 7: Performance of the codec for an invalid combination of bits is not ensured, and such combinations should not be used. The user should make no assumption that the code bits saturate to a maximum or minimum value or wrap around to a valid combination.

SCR12 – RX PGA1 CONTROL
(address: 1100b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA1 = 0 dB
0	0	0	0	0	0	0	1	01	RX PGA1 = 1 dB
0	0	0	0	0	0	1	0	02	RX PGA1 = 2 dB
0	0	0	0	0	0	1	1	03	RX PGA1 = 3 dB
0	0	0	0	0	1	0	0	04	RX PGA1 = 4 dB
0	0	0	0	0	1	0	1	05	RX PGA1 = 5 dB
0	0	0	0	0	1	1	0	06	RX PGA1 = 6 dB
–	–	–	–	–	–	–	–	07–FF	RX PGA1 = 6 dB

SCR13 – EC CHANNEL DIGITAL GAIN CONTROL
(address: 1101b, contents at reset: 00000000b)†

† SCR13 has the same format as SCR11 (see SCR11 – TX Channel Digital Gain Control).

Table 2. System Control Registers (SCRs) (Continued)

SCR14 – MISCELLANEOUS CONTROL 2
(address: 1110b, contents at reset: 00000000b)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	0	0	0	–	–	1	0	Enable FIFO
0	0	0	0	–	1	–	0	Bypass EC digital HPF (138 kHz)
0	0	0	0	1	–	–	0	ECP and ECM are connected to weakly driven mid supply. It can be used only during EC power-down mode.

device initialization time

The TLV320AD13A completes all calibration and initialization in less than 1 second. This includes reference settling time (≈950 μs), one rest after power up (one serial frame), VCXODAC configuration (two serial frames), TX/RX gain select (four serial frames), and calibration of the DAC (256 × 113 ns). Each 16-bit frame requires up to 5 μs. The host processor must initiate this process upon a successful power up.

power down

Both hardware and software power-down modes are provided. The serial interface is operative when the codec is in power-down mode. By sending commands through the serial interface, either the codec or part of the codec can be software powered down. All the references are kept on in the software power-down mode. The codec also can be hardware powered down by setting the PWDN terminal to high. All the references are shut off in the hardware power-down mode. The contents of the registers do not change in either power-down mode.

power-supply grouping recommendation

The following power-supply grouping is recommended for best performance of this device. It is recommended for each power supply group to have a separate ferrite bead.

- Group 1: $AV_{DDFILTX}$, $AV_{DDFILEC}$, AV_{DD1TX}, AV_{DD2TX}, AV_{DD1EC}, AV_{DD2EC}
- Group 2: $AV_{DDFILRX}$, AV_{DDADC}
- Group 3: AV_{DDREF}
- Group 4: DV_{DDBF}, DV_{DDCLK}, DV_{DDLG}, DV_{DDRX}, DV_{DDDAC}

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AV_{DD} to AV_{SS}, DV_{DD} to DV_{SS} . . . . . –0.3 V to 4.5 V
Analog input voltage range to AV_{SS} . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range to DV_{SS} . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DDADC}, AV_{DD1EC}, AV_{DD2EC}, AV_{DD1TX}, AV_{DD2TX}, $AV_{DDFILEC}$, $AV_{DDFILTX}$, $AV_{DDFILRX}$, AV_{DDREF}, DV_{DDBF}, DV_{DDCLK}, DV_{DDLG}, DV_{DDDAC}, DV_{DDRX}	3	3.3	3.6	V
PSSR					dB

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	I_I = 0.75 mA	2			V
Low-level input voltage, V_{IL}	I_I = –0.75 mA			0.8	V

analog input

		MIN	NOM	MAX	UNIT
Analog-input signal range	$AV_{DDFILRX}$ = 3.3 V, input signal is measured single ended		$AV_{DDFILRX}/2$ ±0.75		V
	$AV_{DDFILRX}$ = 3.3 V, input signal is measured differentially		3		V_{PP}

clock

		MIN	NOM	MAX	UNIT
Input clock frequency	DV_{DDCLK} = 3.3 V		35.328		MHz
Input clock duty cycle	DV_{DDCLK} = 3.3 V		50%		

electrical characteristics over recommended operating free-air temperature range, typical at T_A = 25°C, CLKIN = 35.328 MHz, analog power supply = 3.3 V, digital power supply = 3.3 (unless otherwise noted)

TX and EC channel (measured differentially unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal bandwidth			138		kHz
Conversion rate	OSEN = 1		4.416		MHz
	OSEN = 0		2.208		
Channel gain error	PAA = 0 dB, Input = 99.1875 kHz at 6 dB	–0.1		0.1	dB
PAA step gain error		–0.2		0.2	dB
DC offset		–70		70	mV
Cross-talk	RX to TX channel (43.125 kHz at –1 dB)†		–65		dB
Group delay			6		µs
PSRR Power-supply reject ratio	200 mV_{PP} at 99.1875 kHz		50		dB
Full-scale output voltage	Load = 2000 Ω, Single-ended measured		$AV_{DD1TX/2}$ ±0.75		V
	Load = 4000 Ω, Differentially measured		3		V_{PP}
AC Performance					
SNR Signal-to-noise ratio	43.125 kHz at –1dB†		81		dB
THD Total harmonic distortion ratio	43.125 kHz at –1dB†		86		dB
TSNR Signal-to-noise + harmonic distortion ratio	43.125 kHz at –1dB†		80		dB
MT‡ Missing tone test	120.750 kHz (missing tone)		76		dB
Channel Frequency Response					
Gain relative to gain at 99.1875 kHz (25.875-kHz digital HPF is bypassed)	30 kHz	–0.25		0.25	dB
	60 kHz	–0.25		0.25	
	138 kHz		–3		
	276 kHz		–55		

† The input signal is the digital equivalent of a sinewave (digital full scale = 0 dB). The nominal differential output with this input condition is 3 V_{PP}.
‡ 27 tones, 25.875 kHz to 138 kHz, 4.3125 kHz/step, –1 dB

reference output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFP	REF plus voltage	AV_{DDREF} = 3.3 V		2.5		V
REFM	REF minus voltage	AV_{DDREF} = 3.3 V		0.5		V
VMIDREF	REF mid voltage	AV_{DDREF} = 3.3 V		1.5		V
VMIDADC	RX channel mid voltage	AV_{DDREF} = 3.3 V		1.5		V

digital outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = –0.5 mA			0.6	V

electrical characteristics over recommended operating free-air temperature range, typical at T_A = 25°C, CLKIN = 35.328 MHz, analog power supply = 3.3 V, digital power supply = 3.3 (unless otherwise noted) (continued)

RX channel (measured differentially unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal bandwidth				1104		kHz
Conversion rate				4.416		MHz
Channel gain error		PGA1 = 0 dB, PGA2 = 2.5 dB, Input = 99.1875 kHz at –1 dB	–1.5		1.5	dB
PGA gain error		PGA1 (0 dB to 6 dB at 1 dB/step)	–0.2		0.2	dB
		PGA2 (2.5 dB to 14 dB at 0.25 dB/step)	–0.03		0.03	
DC offset		PGA1 = 0 dB, PGA2 = 2.5 dB		3		mV
Crosstalk		TX to RX channel (99.1875 kHz at –1 dB)†		63		dB
Group delay				8		µs
CMRR	Common-mode reject ratio	99.1875 kHz at –1 dB†		70		dB
PSRR	Power-supply reject ratio	200 mV_{PP} at 99.1875 kHz		50		dB
Analog-input self-bias dc voltage				$AV_{DDFILRX/2}$ ±0.75		V
Input impedance				10		kΩ
AC Performance						
SNR	Signal-to-noise ratio	99.1875 kHz at 0 dB†		68		dB
THD	Total harmonic distortion ratio	99.1875 kHz at 0 dB†		77		dB
TSNR	Signal-to-noise + harmonic distortion ratio	99.1875 kHz at 0 dB†		68		dB
MT‡	Missing-tone test	120.750 kHz (missing tone)		66		dB
		750.375 kHz (missing tone)		66		
Channel Frequency Response (EQ[2:0] = 0 dB/MHz)						
Gain relative to gain at 99.1875 kHz		60 kHz	–0.25		0.25	dB
		300 kHz	–0.25		0.25	
		800 kHz		1		
		1000 kHz		0.7		

† The analog input test signal is a sine wave with 0 dB = 3 V_{PP} as the reference level.
‡ 250 tones, 25.875 kHz to 1104 kHz, 4.3125 kHz/step, 0 dB

VCXO DAC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			12		Bit
DNL	Differential nonlinearity			±1		LSB
INL	Integral nonlinearity			±4		LSB
	Offset error			30		mV
Analog output	Full-scale output voltage	Load = 50 kΩ, V_{DD} = 3.3 V		3		V

power dissipation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	Active mode			800	850	mW
	Power-down mode	Hardware power down		65		
		Software power down		70		

timing requirements

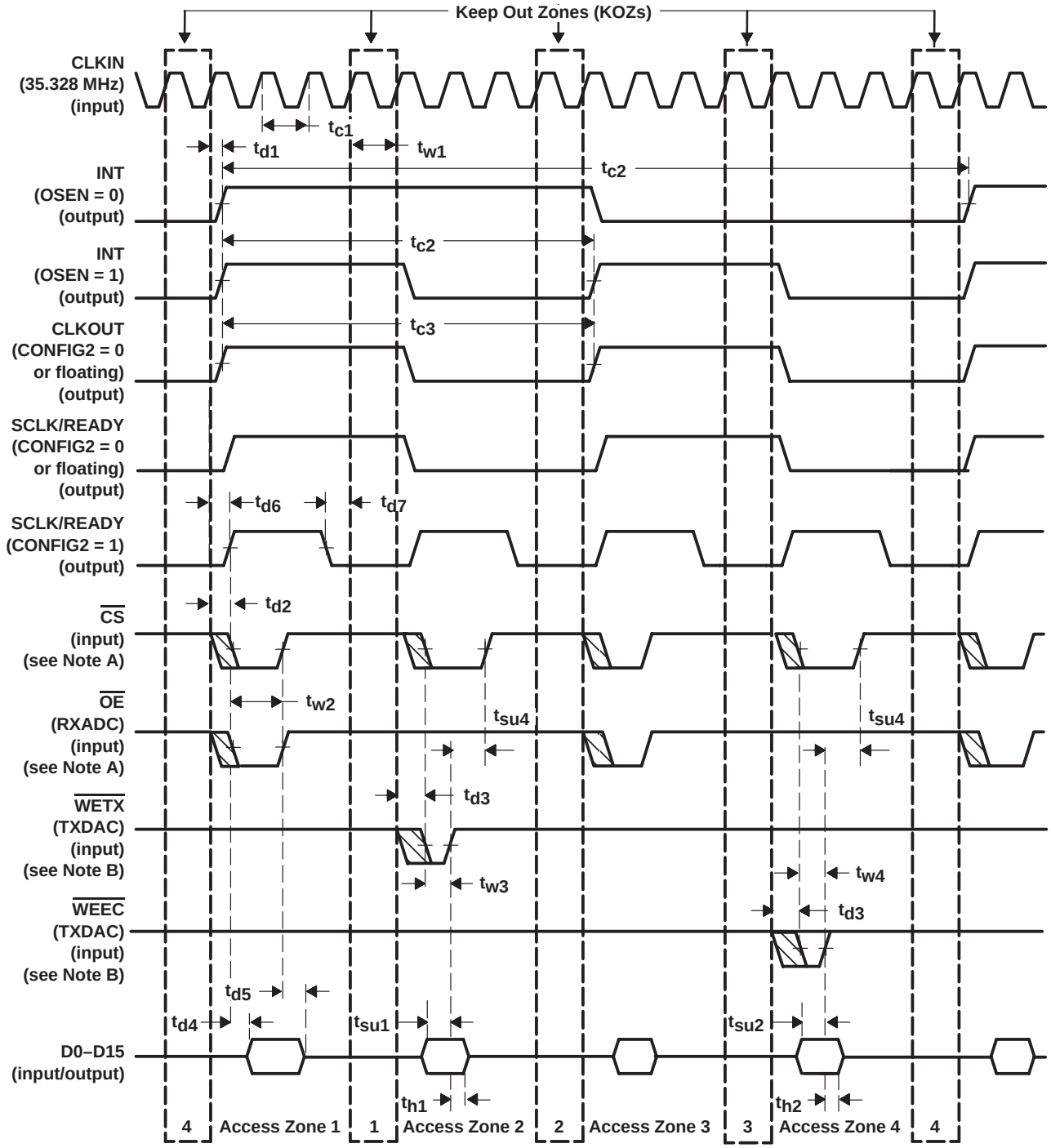
parallel port (see Figures 2 and 3)

		MIN	NOM	MAX	UNIT
t_{c1}	Cycle time, CLKIN		28.3		ns
t_{h1}	Hold time, D0–D15 valid after $\overline{WETX}\uparrow$	5			ns
t_{h2}	Hold time, D0–D15 valid after $\overline{WEEC}\uparrow$	5			ns
t_{h3}	Hold time, SYNC high after CLKIN$\uparrow$	5			ns
t_{su1}	Setup time, D0–D15 valid before $\overline{WETX}\uparrow$	15			ns
t_{su2}	Setup time, D0–D15 valid before $\overline{WEEC}\uparrow$	15			ns
t_{su3}	Setup time, SYNC high before CLKIN$\uparrow$	10			ns
t_{su4}	Setup time, $\overline{WETX}$/$\overline{WEEC}$ high before $\overline{CS}\uparrow$	5			ns
t_{w1}	Pulse duration, KOZ		1		CLKIN cycle
t_{w2}	Pulse duration, $\overline{OE}$ low	20			ns
t_{w3}	Pulse duration, $\overline{WETX}$ low	28			ns
t_{w4}	Pulse duration, $\overline{WEEC}$ low	28			ns
t_{w5}	Pulse duration, SYNC high		28		ns

switching characteristics over recommended operating conditions (unless otherwise noted)

parallel port (see Figures 2 and 3)

PARAMETER			MIN	TYP	MAX	UNIT
t_{c2}	Cycle time, INT	OSEN = 0		16		CLKIN cycles
		OSEN = 1		8		
t_{c3}	Cycle time, CLKOUT			8		CLKIN cycles
t_{d1}	Delay time, KOZ end to $\overline{INT}\uparrow$				5	ns
t_{d2}	Delay time, KOZ end (CLKIN$\uparrow$) to $\overline{OE}\downarrow$/$\overline{CS}\downarrow$		0			ns
t_{d3}	Delay time, KOZ end to $\overline{WETX}\downarrow$/$\overline{CS}\downarrow$ or $\overline{WEEC}\downarrow$/$\overline{CS}\downarrow$		0			ns
t_{d4}	Delay time, from $\overline{OE}\downarrow$/$\overline{CS}\downarrow$ (and READY$\uparrow$ if CONFIG2 = 1) to D0–D15 valid				15	ns
t_{d5}	Delay time, from $\overline{OE}\uparrow$/$\overline{CS}\uparrow$ to D0–D15 Hi-Z				5	ns
t_{d6}	Delay time, KOZ end to SCLK/READY$\uparrow$			14.2		ns
t_{d7}	Delay time, SCLK/READY$\downarrow$ to KOZ			14.2		ns



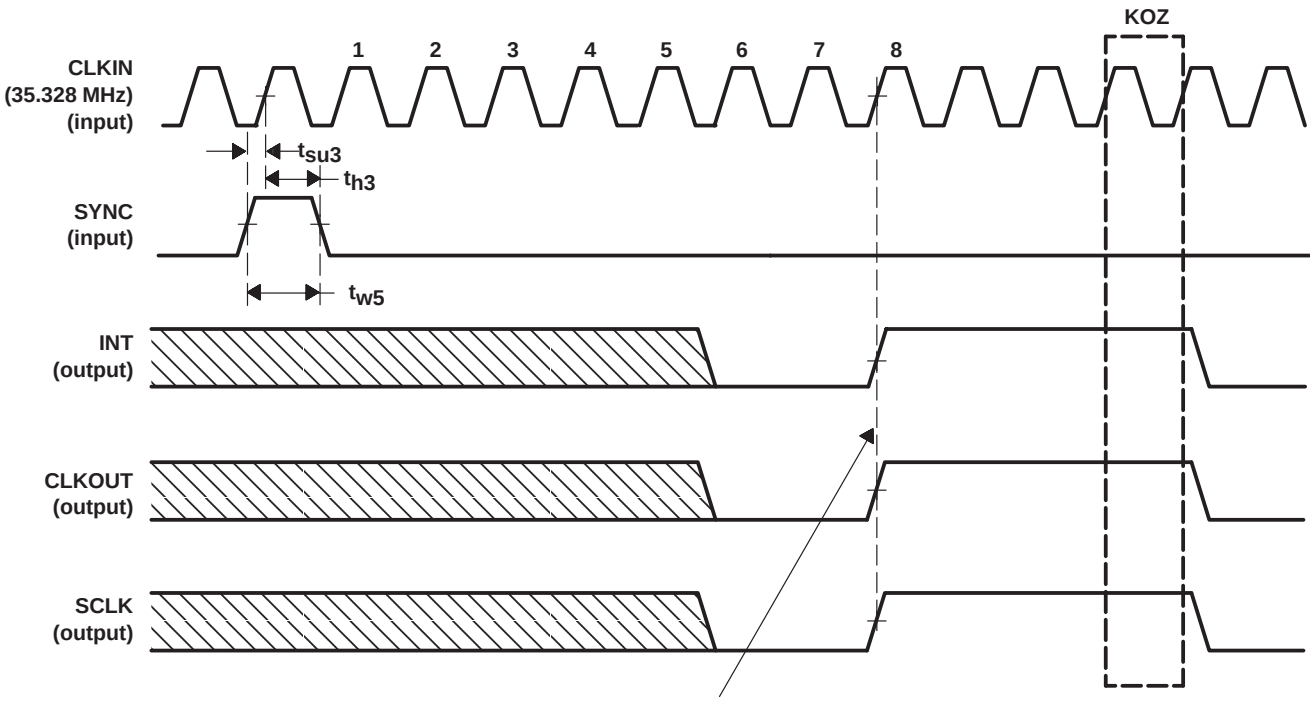
NOTES: A. $\overline{CS}$ AND $\overline{OE}$ may fall/rise together or be skewed from each other. It does not matter which falls/rises first. However, t_{d4} is referenced from whichever falls last, and t_{d5} is referenced from whichever rises first. $\overline{CS}$ can be connected to low if the parallel bus is not shared.

B. $\overline{CS}$ and $\overline{WETX}$/$\overline{WEEC}$ may fall together or be skewed from each other. The rising edges of $\overline{WETX}$ and $\overline{WEEC}$ should occur prior to the rising edge of $\overline{CS}$.

C. The minimum update rate for TX and EC channel is 276 kHz in normal mode, and 552 kHz in oversampling mode. The write operation for TX and EC can occur at any place as long as they do not conflict with each other or the read cycle.

D. If CONFIG2 = 1, the READY signal must be high to read or write the codec.

Figure 2. Parallel Port



Rising edge of INT and CLKOUT occurs on eighth rising edge of CLKIN after SYNC pulse is sampled high.

Figure 3. SYNC Pulse

timing requirements

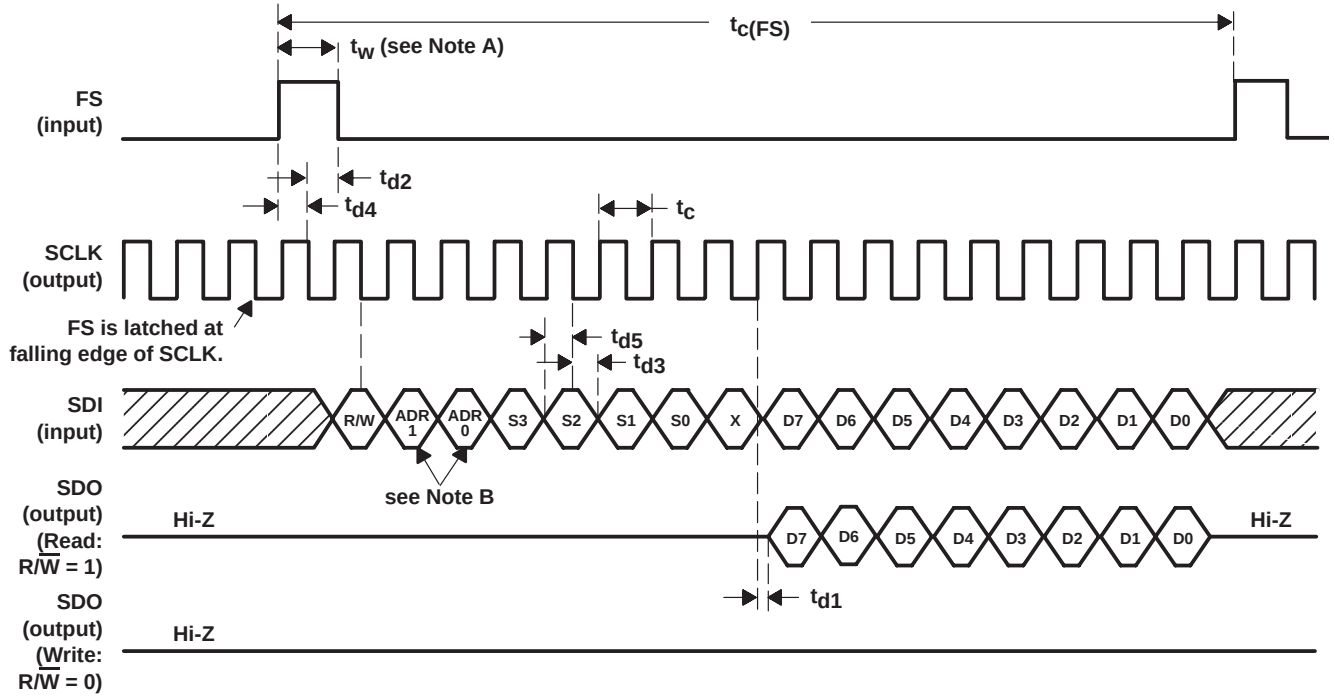
serial port (see Figure 4)

		MIN	NOM	MAX	UNIT
t_W	Pulse duration, FS high		28		ns
$t_{c(FS)}$	Cycle time, FS	18			SCLK cycles

switching characteristics over recommended operating conditions

serial port (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
t_c	Cycle time, SCLK		8		CLKIN cycles
t_{d1}	Delay time, SCLK↑ to SDO valid			15	ns
t_{d2}	Delay time, SCLK↓ to FS↓	5			ns
t_{d3}	Delay time, SCLK↓ to SDI invalid	5			ns
t_{d4}	Delay time, FS↑ to SCLK↓	20			ns
t_{d5}	Delay time, SDI valid to SCLK↓	20			ns

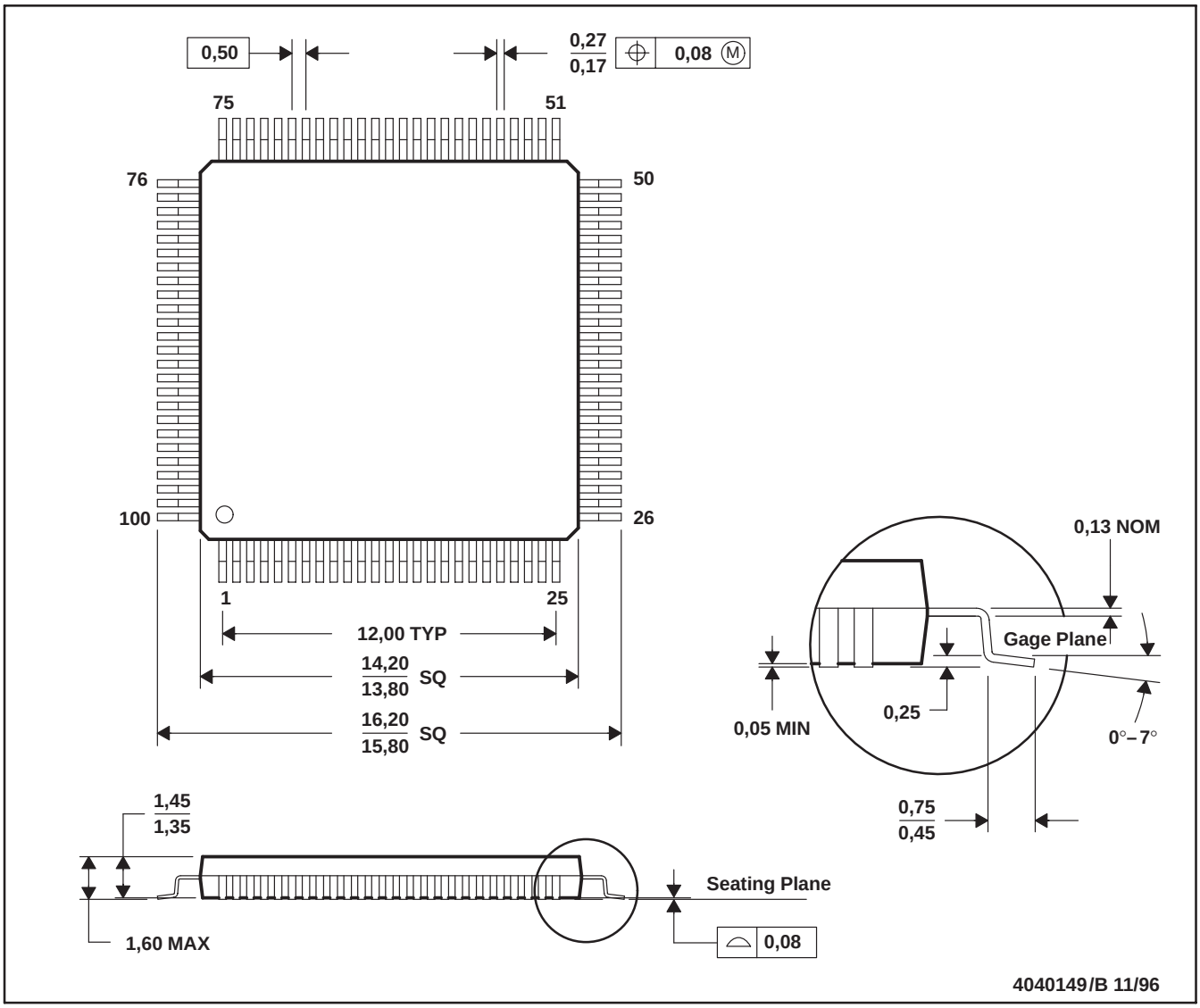


NOTES: A. A width of one SCLK cycle time is recommended for t_W.
B. ADR0 and ADR1 are the hardware-configurable values of ADR0 and ADR1 input terminals.
C. Data on SDI is latched at the falling edge of SCLK.
D. Data is sent from SDO at the rising edge of SCLK.

Figure 4. Serial Port

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

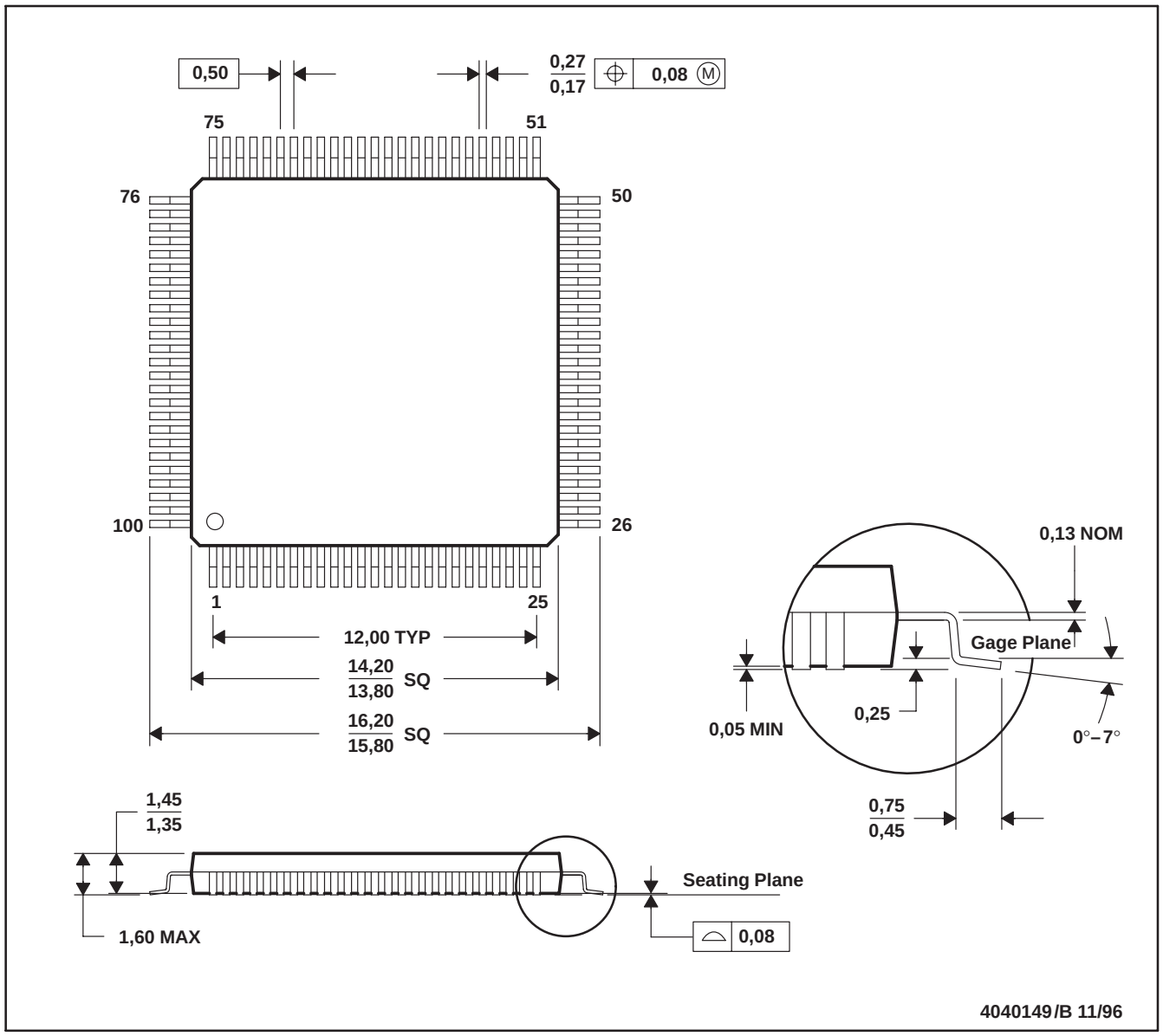
thermal resistance (R_θ) characteristics

NO			°C/W	AIR FLOW (LFPM)†
1	$R_{\theta JC}$	Junction-to-case	5.4	N/A
2	$R_{\theta JA}$	Junction-to-free air	30.4	0
3			24.2	150
4			22.3	250
5			20.0	500

† LFPM = Linear feet per minute

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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