Migrating from TMSVC5409 to TMS320VC5409A

Tai Nguyen *Digital Signal Processing Solutions*

ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5409 to the TMS320VC5409A. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets, 5409 (SPRS082), 5409A (SPRS139), the *TMS320C54x DSP CPU and Peripherals, Reference Set, Volume 1* (SPRS131) and the *TMS320C54x DSP Enhanced Peripherals, Reference Set, Volume 5* (SPRU302).

Migration issues from the 5409 to 5409A are indicated with the following symbols:

S means software modification is required

H means hardware modification is required

D means the 5409 and 5409A are different (usually due to added features on the 5409A) but no modification is necessary for migration (i.e. different but compatible).

These symbols are included at the beginning of each section.

Revision History:

Revision	Date	Description
1.0	06/19/00	Original

Contents

1 Package and Pinout Compatibility

The 5409A is available in two package types:

- 144-pin PGE thin quad flat pack (LQFP)
- 144-pin GGU ball grid array MicroStar BGA

Both these package types are pin compatible (same footprint and pinout) with the 5409.

2 Power Supply [H]

The 5409 CVdd operates at 1.8V and DVdd operates at 3.3V while the 5409A CVdd operates at 1.5V and DVdd operates at 3.3V.

The power-up/power-down sequence on 5409A is not different from that of 5409. Both supplies may be powered up/down simultaneously. If it is impossible to power-up/down the CVdd and DVdd simultaneously, CVdd must be powered up first, DVdd second. For power-down, DVdd must be powered down first, CVdd second.

3 Clock Mode Settings at Reset [H]

The PLL programming and operation of the 5409A PLL is similar to the 5409 but the clock mode settings at device reset is different. Refer to 5409 (SPRS082) and 5409A (SPRS140) data sheets for more details. Note that the 5409A does not support the clock mode of internal oscillator with external crystal.

4 Multi-channel Buffered Serial Port (McBSP) [H/S]

The 5409A McBSP slightly differs from the 5409. The 5409A McBSP has been enhanced:

- To allow all 128 channels of a 128-channel bit stream can be enabled simultaneously
- To enable the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator

Three control bits and twelve registers have been added to enable the 128 channel selection. Refer to the 5409A data sheet (SPRS140) for more details.

5 Host Port Interface (HPI)

The 5409A HPI is similar to the 5409. In addition of capability to interface to an 8-bit host, the 5409A HPI has been enhanced so it can be interfaced to a 16-bit host processor.

The 5409A HPI memory map and type is the same as the 5409.

6 DMA External and Extended Memory Transfer [D]

The 5409A DMA has external memory access that is implemented slightly different from the 5409. The 5409A DMA has been enhanced to provide a better throughput when accessing to extended external program, data and IO memory. Refer to the 5409A data sheet (SPRS140) for more details.

7 DMA Auto-initialization [H/S]

The 5409A has been enhanced to expand the global reload register set. Each DMA channel now has its own global reload register set. For example the DMA channel 1 has DMGSA1, DMGDA1, DMGCR1 and DMGFR1 registers as its global reload registers. Refer to the 5409A data sheet (SPRS140) for more details.

8 Bank Switching Control Register [S]

The Bank Switching Control Register (BSCR) on the 5409 and 5409A are different. The bit map of the BSCRs for both devices are shown below.

5409 BSCR (0x29)

15–12	11	10–3	2	1	0
BNKCMP	PS-DS	Resv	HBH	BH	EXIO

5409A BSCR (0x29)

15	14–13	12	11–3	2	1	0
CONSEC	DIVFCT	IACKOFF	Resv	HBH	BH	Resv

The CONSEC field of the 5409A BSCR is replaced functionally with the BNKCMP and PS-DS fields of the 5409 BSCR. The 5409A has a different external parallel interface from the 5409. The signals are identical but the timing waveform of signals is different. Refer to the 5409A data sheet (SPRS140) for more detail.

9 External Parallel Interface [D]

Although the signals on the 5409A external parallel interface are identical to the 5409, the timing of the 5409A external parallel interface signals are different from the 5409. The 5409A supports additional leading and trailing cycles on external accesses. External access now takes a different amount of time than before. This difference should be considered if the application to be migrated is highly bandwidth-limited based on the operation of the external parallel interface. Otherwise the 5409A interface is compatible.

10 CLKOUT Division [H/S]

On the 5409, CLKOUT always represents the CPU clock. On the 5409A, the DIVFCT field in the BSCR controls whether the CLKOUT represents the CPU clock divided by 1, 2, 3 or 4.

11 Memory Map [D]

The memory map and memory types of the 5409A is identical to the 5409, i.e. four blocks of 8K dual-access RAM (DARAM).

12 Boot-loader/ROM Contents [D]

The boot-loader options available on the 5409A are identical to the 5409. Note that some of the ROM contents are reserved on the 5409. Refer to the 5409A date sheet (SPRS140) for more details.

13 Data Security [D]

The ROM security of the 5409A functions similarly to the 5409 with the following exception:

- 5409 allows only HPI writes (no read) to entire 32K on chip RAM
- 5409A allows both HPI read and write to only 8K on chip RAM (4000h–5FFFh)

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265