

TLV2401, TLV2402, TLV2404

FAMILY OF 880-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS WITH REVERSE BATTERY PROTECTION

SLOS244B – FEBRUARY 2000 – REVISED NOVEMBER 2000

- Micro-Power Operation . . . $< 1 \mu\text{A}/\text{Channel}$
- Input Common-Mode Range Exceeds the Rails . . . -0.1 V to $V_{\text{CC}} + 5 \text{ V}$
- Reverse Battery Protection Up To 18 V
- Rail-to-Rail Input/Output
- Gain Bandwidth Product . . . 5.5 kHz
- Supply Voltage Range . . . 2.5 V to 16 V
- Specified Temperature Range
 - $T_A = 0^\circ\text{C}$ to 70°C . . . Commercial Grade
 - $T_A = -40^\circ\text{C}$ to 125°C . . . Industrial Grade
- Ultrasmall Packaging
 - 5-Pin SOT-23 (TLV2401)
 - 8-Pin MSOP (TLV2402)
- Universal OpAmp EVM (Refer to the EVM Selection Guide SLOU060)

description

The TLV240x family of single-supply operational amplifiers has the lowest supply current available today at only 880 nA per channel. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega- Ω resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 390 μV , CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers available today including TI's MSP430.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in TSSOP.

Operational Amplifier



SUPPLY CURRENT
vs
SUPPLY VOLTAGE



SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS[†]

DEVICE	V_{CC} (V)	V_{IO} (mV)	BW (MHz)	SLEW RATE (V/ μs)	I_{CC}/ch (μA)	RAIL-TO-RAIL
TLV240x [‡]	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

[†] All specifications are typical values measured at 5 V.

[‡] This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLV2401 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SOT-23† (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	1500 µV	TLV2401CD	TLV2401CDBV	VAWC	—
–40°C to 125°C		TLV2401ID	TLV2401IDBV	VAWI	TLV2401IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2401CDR).

TLV2402 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP† (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	1500 µV	TLV2402CD	TLV2402CDGK	xxTIAIX	—
–40°C to 125°C		TLV2402ID	TLV2402IDGK	xxTIAIY	TLV2402IP

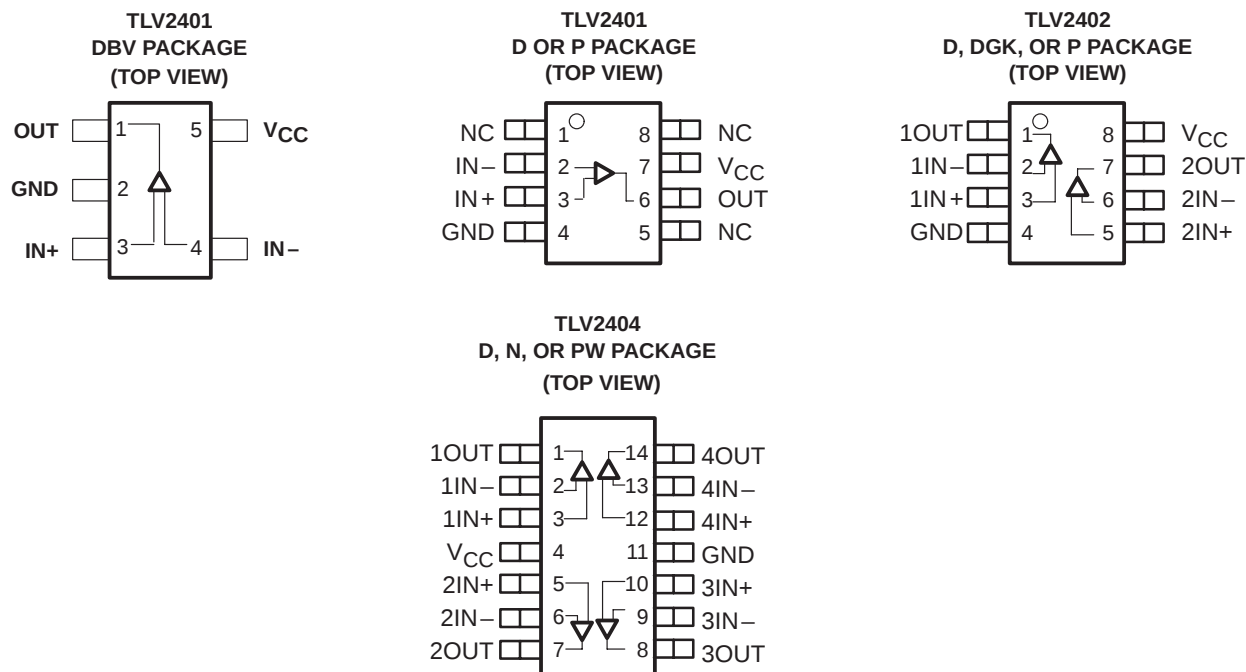
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2402CDR).

TLV2404 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	1500 µV	TLV2404CD	TLV2404CN	TLV2404CPW
–40°C to 125°C		TLV2404ID	TLV2404IN	TLV2404IPW

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2404CDR).

TLV240x PACKAGE PINOUTS



NC – No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	17 V
Differential input voltage range, V_{ID}	± 20 V
Input current range, I_I (any input)	± 10 mA
Output current range, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	16	V
	Split supply	± 1.25	± 8	
Common-mode input voltage range, V_{ICR}		–0.1	$V_{CC}+5$	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _O = V _{CC} /2 V, V _{IC} = V _{CC} /2 V, R _S = 50 Ω		25°C		390	1200	μV
				Full range			1500	
αV _{IO}	Offset voltage draft			25°C		3		μV/°C
CMRR	Common-mode rejection ratio	V _{IC} = 0 to V _{CC} , R _S = 50 Ω	V _{CC} = 2.7 V	25°C		63	120	dB
				Full range			60	
			V _{CC} = 5 V	25°C		70	120	
				Full range			63	
			V _{CC} = 15 V	25°C		80	120	
				Full range			75	
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 2.7 V, V _O (pp) = 1 V, R _L = 500 kΩ	25°C		130	400	V/mV	
			Full range			30		
		V _{CC} = 5 V, V _O (pp) = 3 V, R _L = 500 kΩ	25°C		300	1000		
			Full range			100		
		V _{CC} = 15 V, V _O (pp) = 6 V, R _L = 500 kΩ	25°C		1000	1800		
			Full range			120		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{IO} Input offset current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	25°C		25	250	pA
		Full range			300	
					400	
I_{IB} Input bias current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	25°C		100	300	pA
		Full range			350	
					900	
$r_{i(d)}$ Differential input resistance		25°C		300		M Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 100 \text{ kHz}$	25°C		3		pF

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	V _{IC} = V _{CC} /2, I _{OH} = −2 μA	V _{CC} = 2.7 V	25°C	2.65	2.68		V
				Full range	2.63			
			V _{CC} = 5 V	25°C	4.95	4.98		
				Full range	4.93			
			V _{CC} = 15 V	25°C	14.95	14.98		
				Full range	14.93			
		V _{IC} = V _{CC} /2, I _{OH} = −50 μA	V _{CC} = 2.7 V	25°C	2.62	2.65		
				Full range	2.6			
			V _{CC} = 5 V	25°C	4.92	4.95		
				Full range	4.9			
			V _{CC} = 15 V	25°C	14.92	14.95		
				Full range	14.9			
V _{OL}	Low-level output voltage	V _{IC} = V _{CC} /2, I _{OL} = 2 μA		25°C		90	150	mV
				Full range			180	
		V _{IC} = V _{CC} /2, I _{OL} = 50 μA		25°C		180	230	
				Full range			260	
I _O	Output current	V _O = 0.5 V from rail		25°C		±200		μA

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
I _{CC}	Supply current (per channel)	V _O = V _{CC} /2	V _{CC} = 2.7 V or 5 V	25°C		880	950	nA
				Full range			1290	
			V _{CC} = 15 V	25°C		900	990	
				Full range			1350	
Reverse supply current		V _{CC} = −18 V, V _{IN} = 0 V, V _O = Open circuit		25°C		50		nA
PSRR	Power supply rejection ratio (ΔV _{CC} /ΔV _{IO})	V _{CC} = 2.7 to 5 V, V _{IC} = V _{CC} /2 V, No load,		25°C	100	120		dB
			TLV240xC	Full range		96		dB
					TLV240xI		85	
			V _{CC} = 5 to 15 V, V _{IC} = V _{CC} /2 V, No load		25°C	100	120	
				Full range	100			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.



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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V}$, $R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		2.5		V/ms
ϕM	Phase margin	$R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$		25°C		60°		
	Gain margin					15		dB
t_s	Settling time	$V_{CC} = 2.7 \text{ or } 5 \text{ V}$, $V(\text{STEP})_{PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.1%	25°C		1.84		ms
		$V_{CC} = 15 \text{ V}$, $V(\text{STEP})_{PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.1%			6.1		
		$V_{CC} = 15 \text{ V}$, $V(\text{STEP})_{PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.01%			32		

noise/distortion performance

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	$f = 10 \text{ Hz}$	25°C		800		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$			500		
I_n	Equivalent input noise current	$f = 100 \text{ Hz}$			8		$\text{fA}/\sqrt{\text{Hz}}$

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}	Input Bias Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
I_{IO}	Input Offset Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13, 15
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

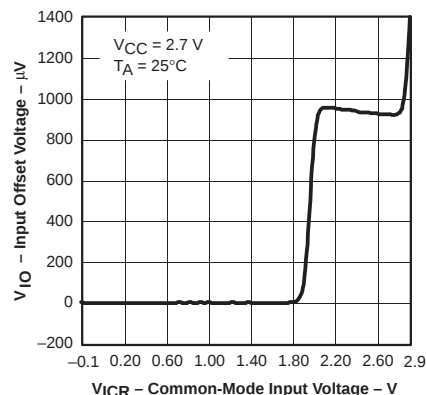


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

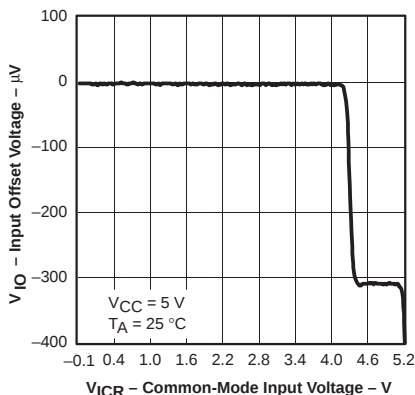


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

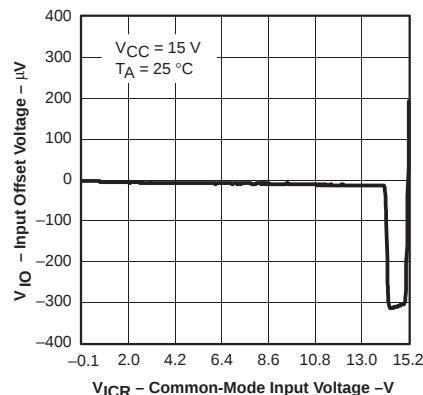


Figure 3

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

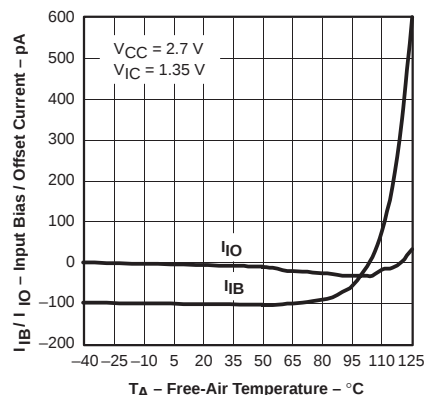


Figure 4

INPUT BIAS / OFFSET CURRENT
vs
COMMON MODE INPUT
VOLTAGE

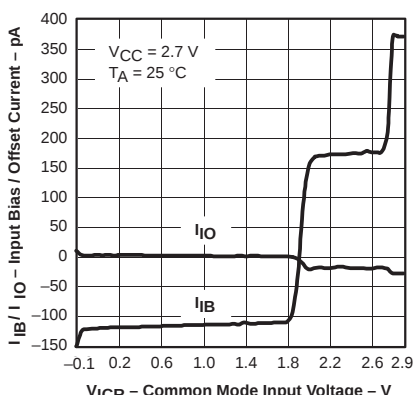


Figure 5

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

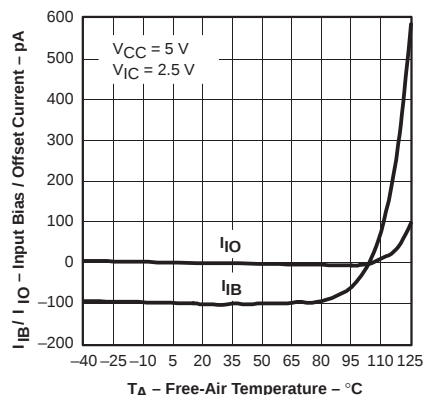


Figure 6

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

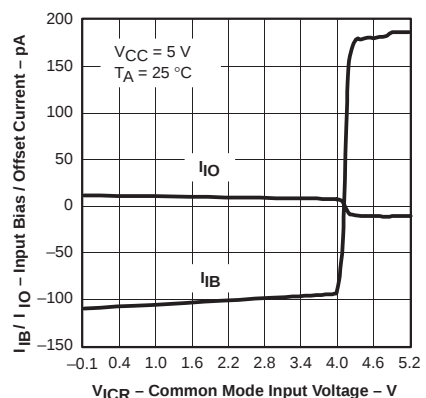


Figure 7

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

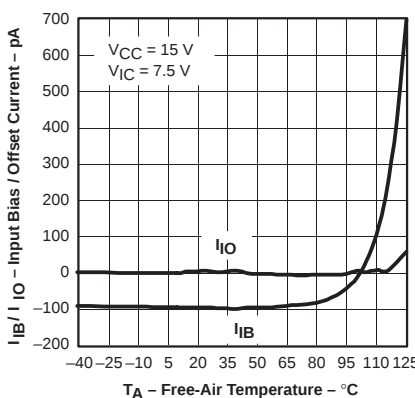


Figure 8

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

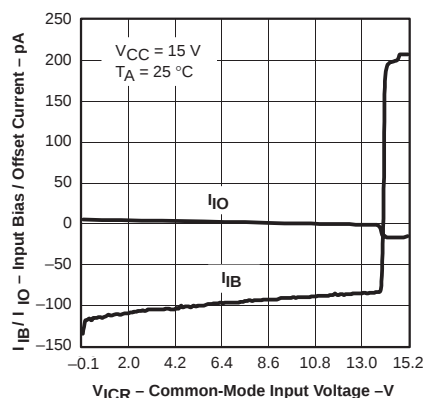


Figure 9



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TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**

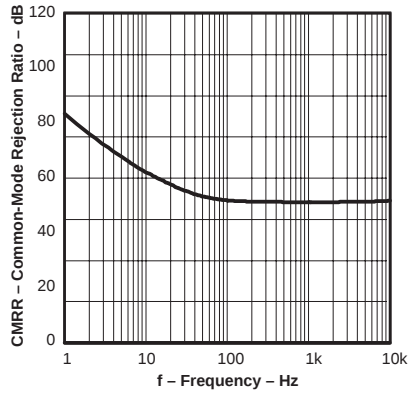


Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

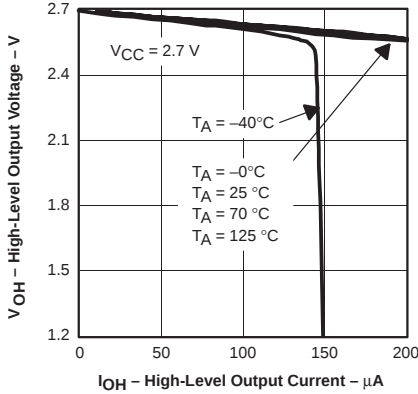


Figure 11

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

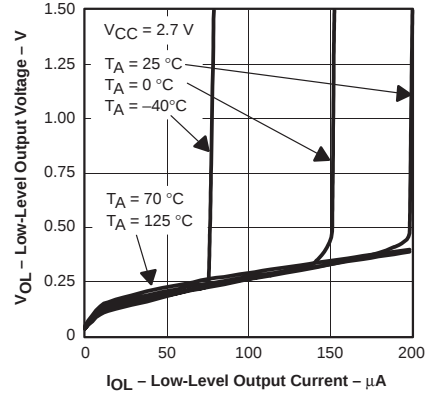


Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

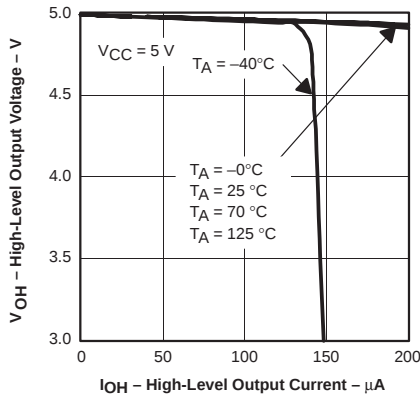


Figure 13

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

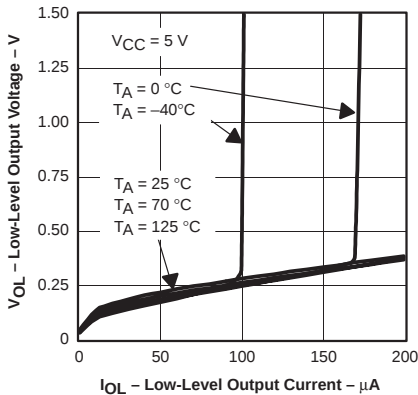


Figure 14

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

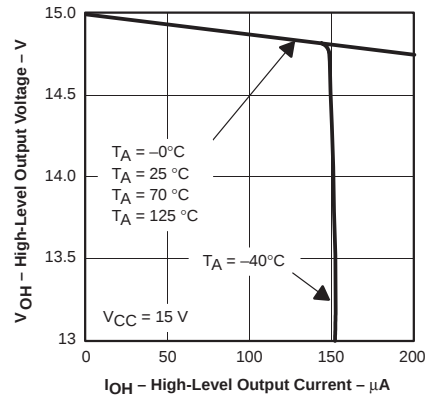


Figure 15

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

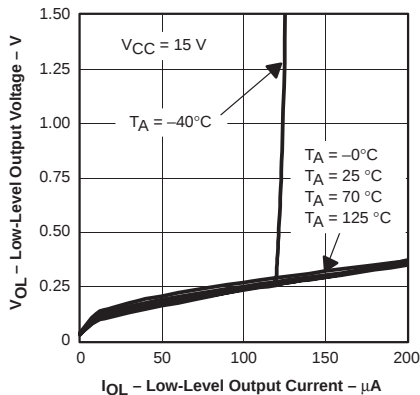


Figure 16

**OUTPUT VOLTAGE
PEAK-TO-PEAK
VS
FREQUENCY**

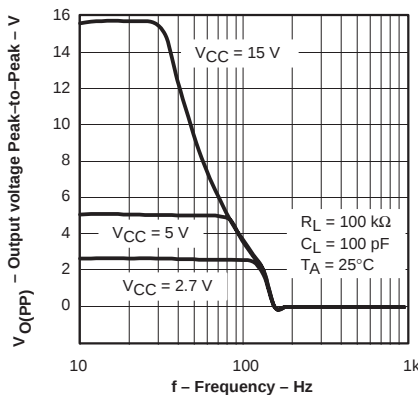


Figure 17

**OUTPUT IMPEDANCE
VS
FREQUENCY**

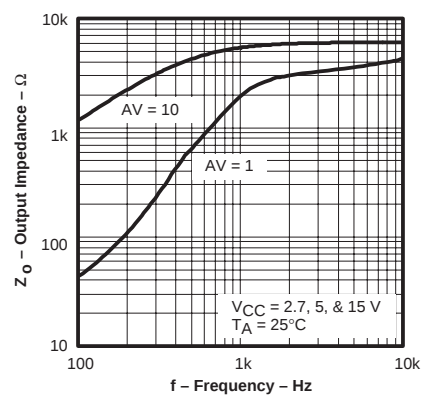


Figure 18

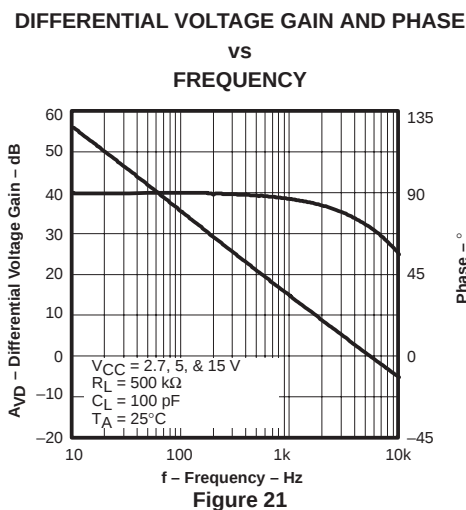
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



Figure 25

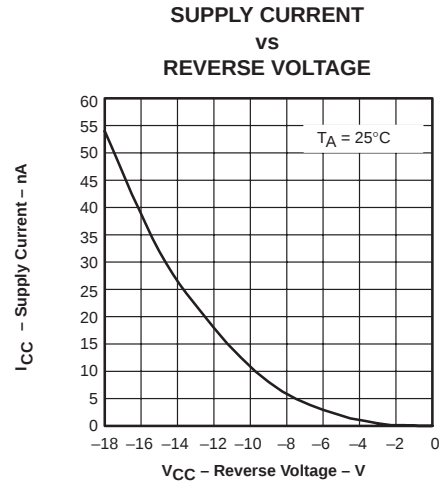


Figure 26

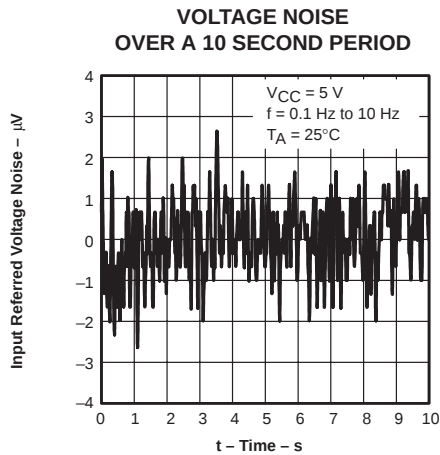


Figure 27

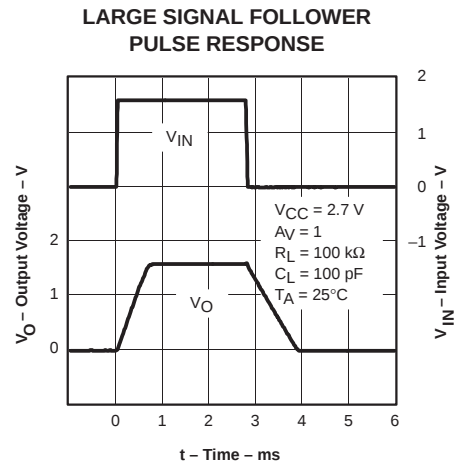


Figure 28

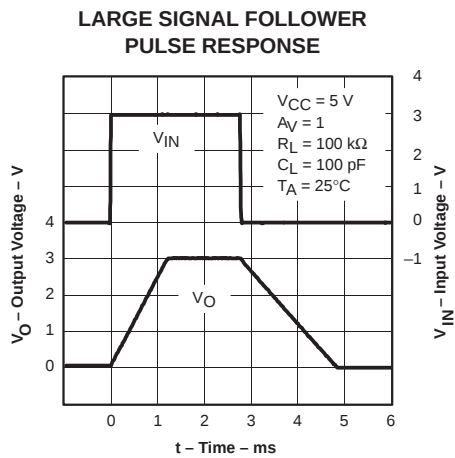


Figure 29

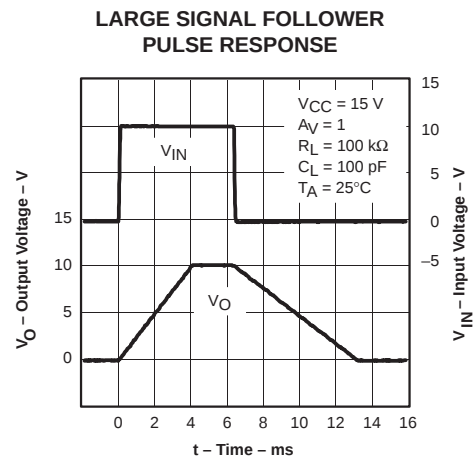


Figure 30

TLV2401, TLV2402, TLV2404

FAMILY OF 880-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS WITH REVERSE BATTERY PROTECTION

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TYPICAL CHARACTERISTICS

**SMALL SIGNAL FOLLOWER
PULSE RESPONSE**



Figure 31

**LARGE SIGNAL INVERTING
PULSE RESPONSE**



Figure 32

**LARGE SIGNAL INVERTING
PULSE RESPONSE**



Figure 33

**LARGE SIGNAL INVERTING
PULSE RESPONSE**

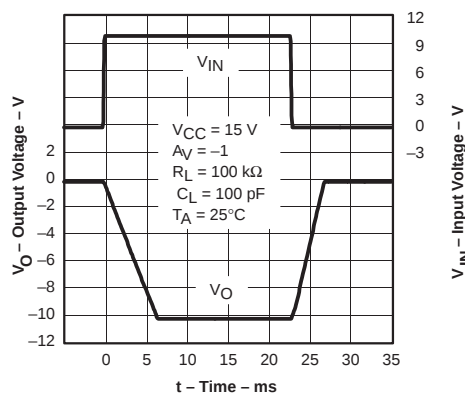


Figure 34

**SMALL SIGNAL INVERTING
PULSE RESPONSE**



Figure 35

**CROSSTALK
vs
FREQUENCY**

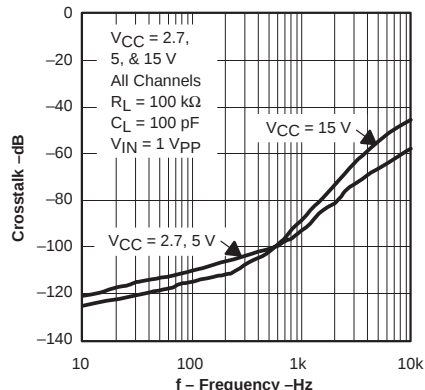


Figure 36

APPLICATION INFORMATION

reverse battery protection

The TLV2401/2/4 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

common-mode input range

The TLV2401/2/4 has rail-to-rail input and outputs. For common-mode inputs from -0.1 V to $V_{CC} - 0.8\text{ V}$ a PNP differential pair will provide the gain.

For inputs between $V_{CC} - 0.8\text{ V}$ and V_{CC} , two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails, because as the inputs go above V_{CC} , the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC} .

The TLV2401/2/4 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

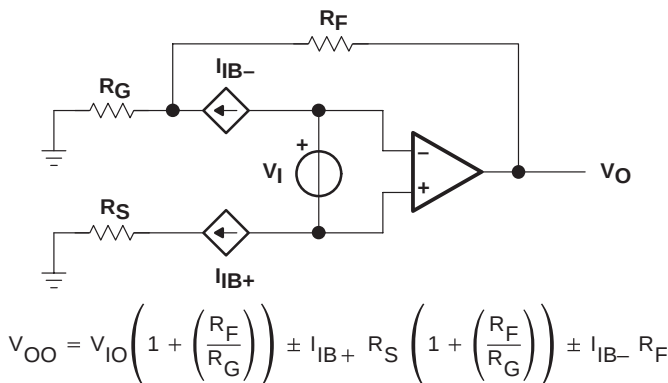


Figure 37. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

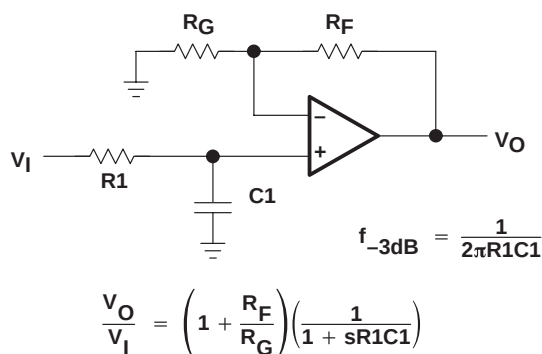


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

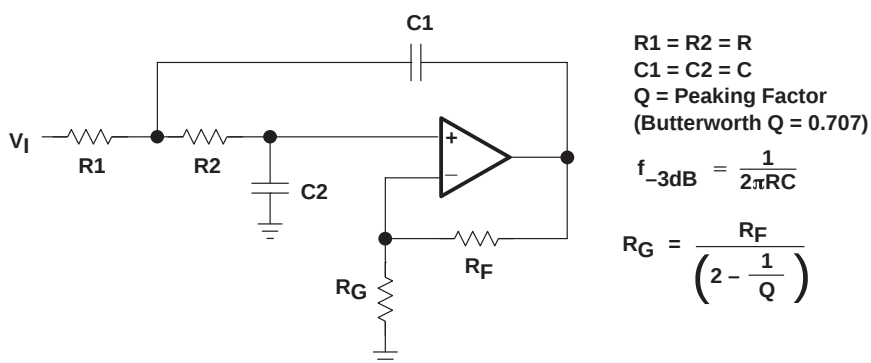


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV240x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

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APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of THS240x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 41 are generated using the TLV240x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

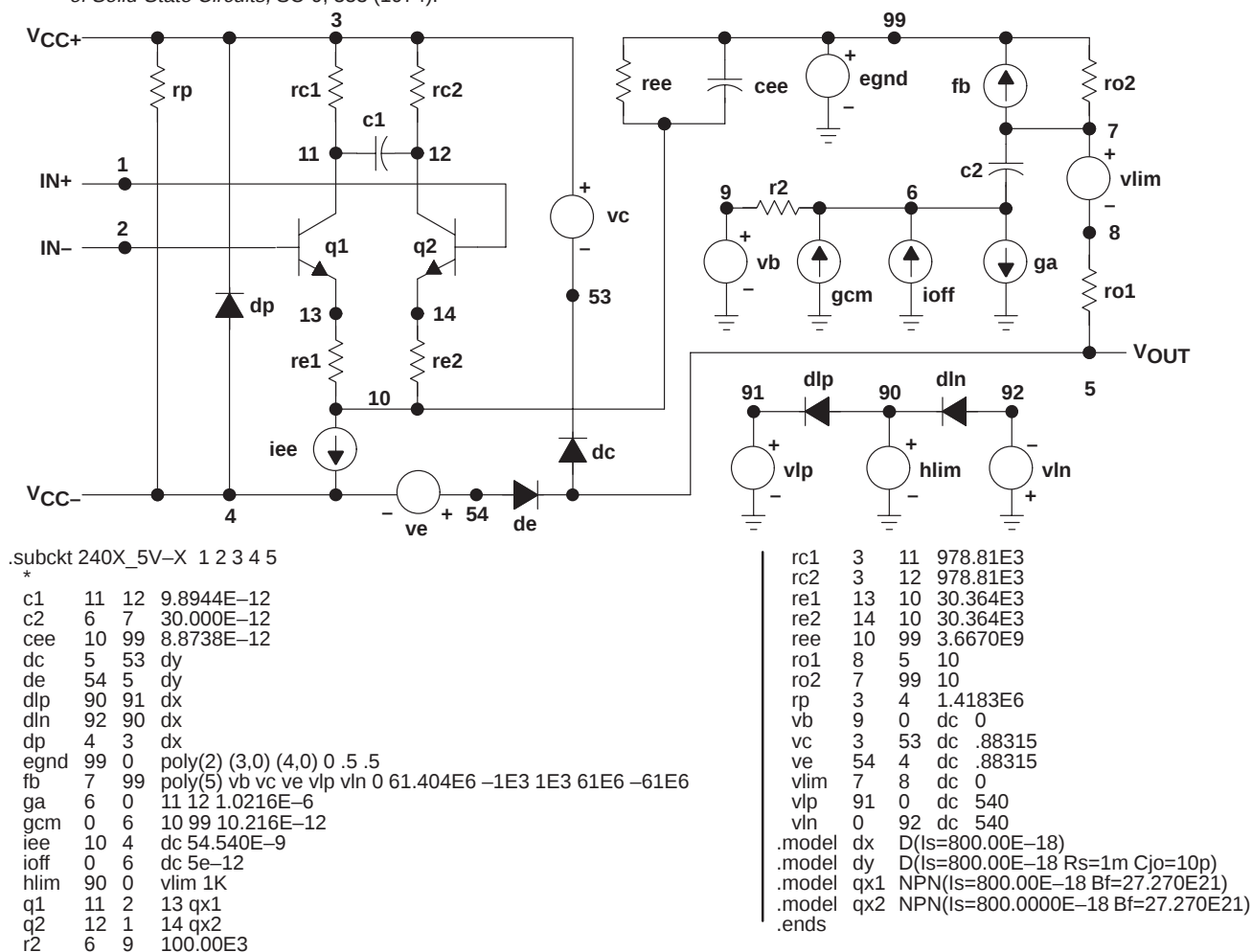


Figure 41. Boyle Macromodels and Subcircuit

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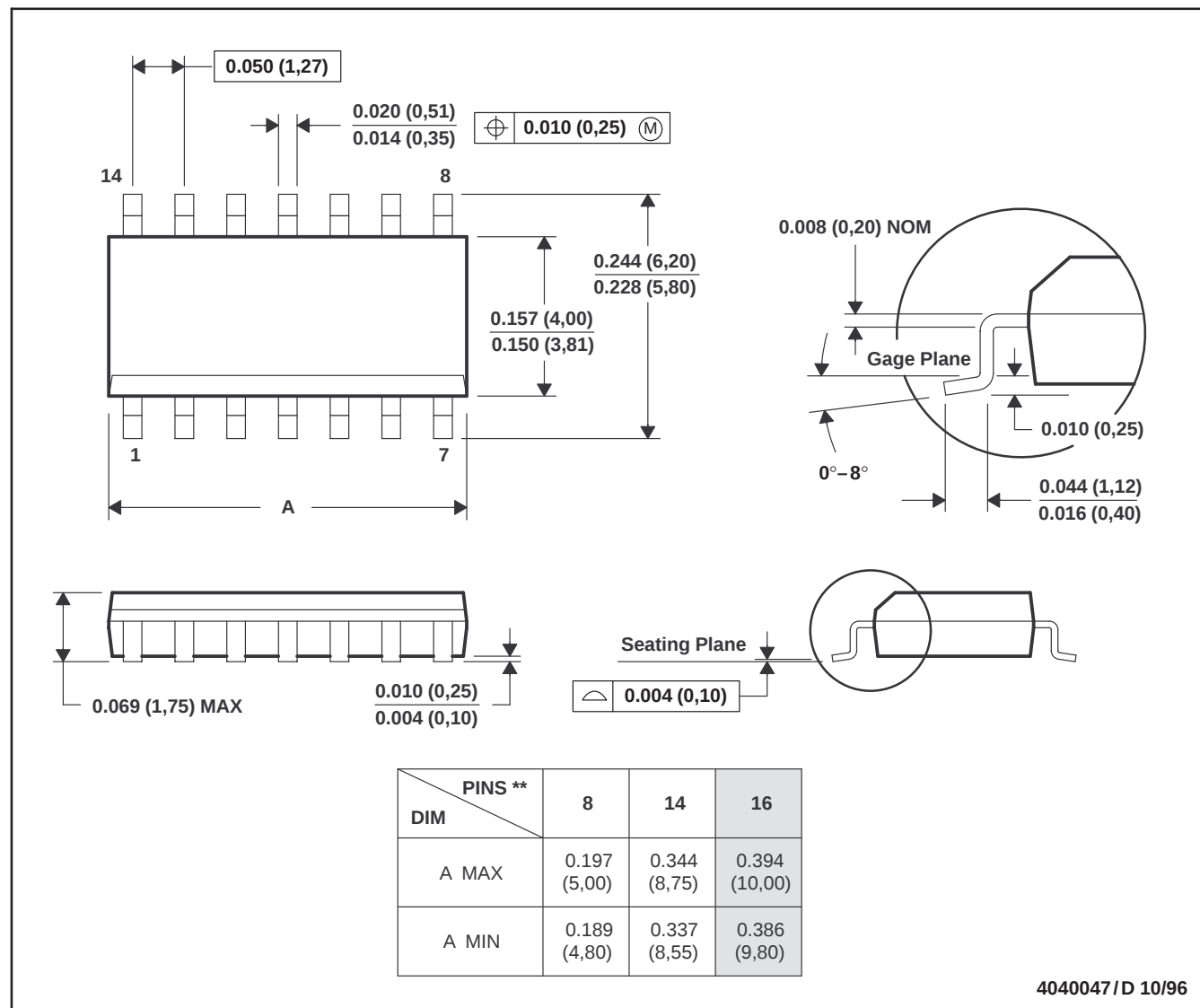
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

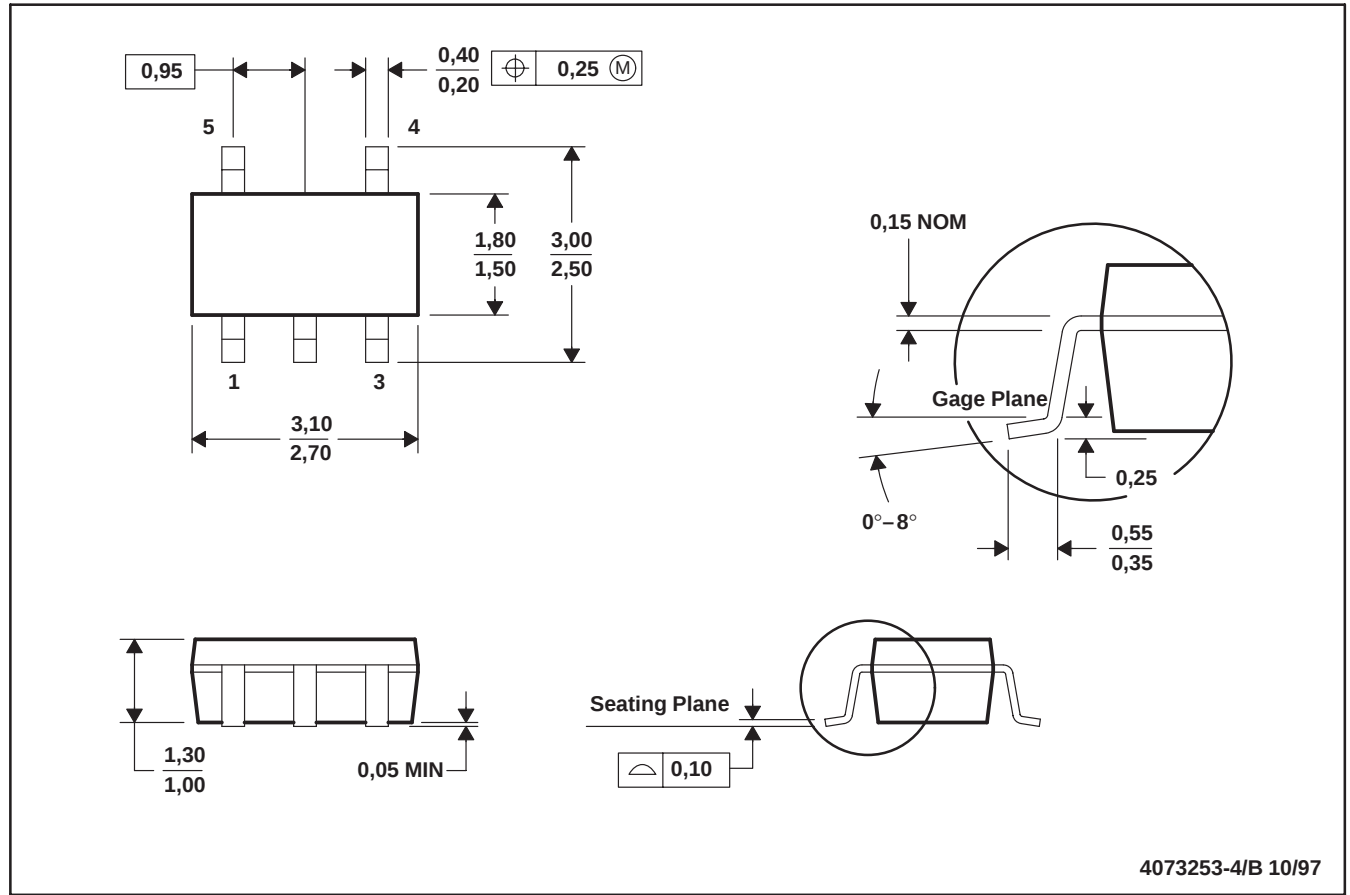


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

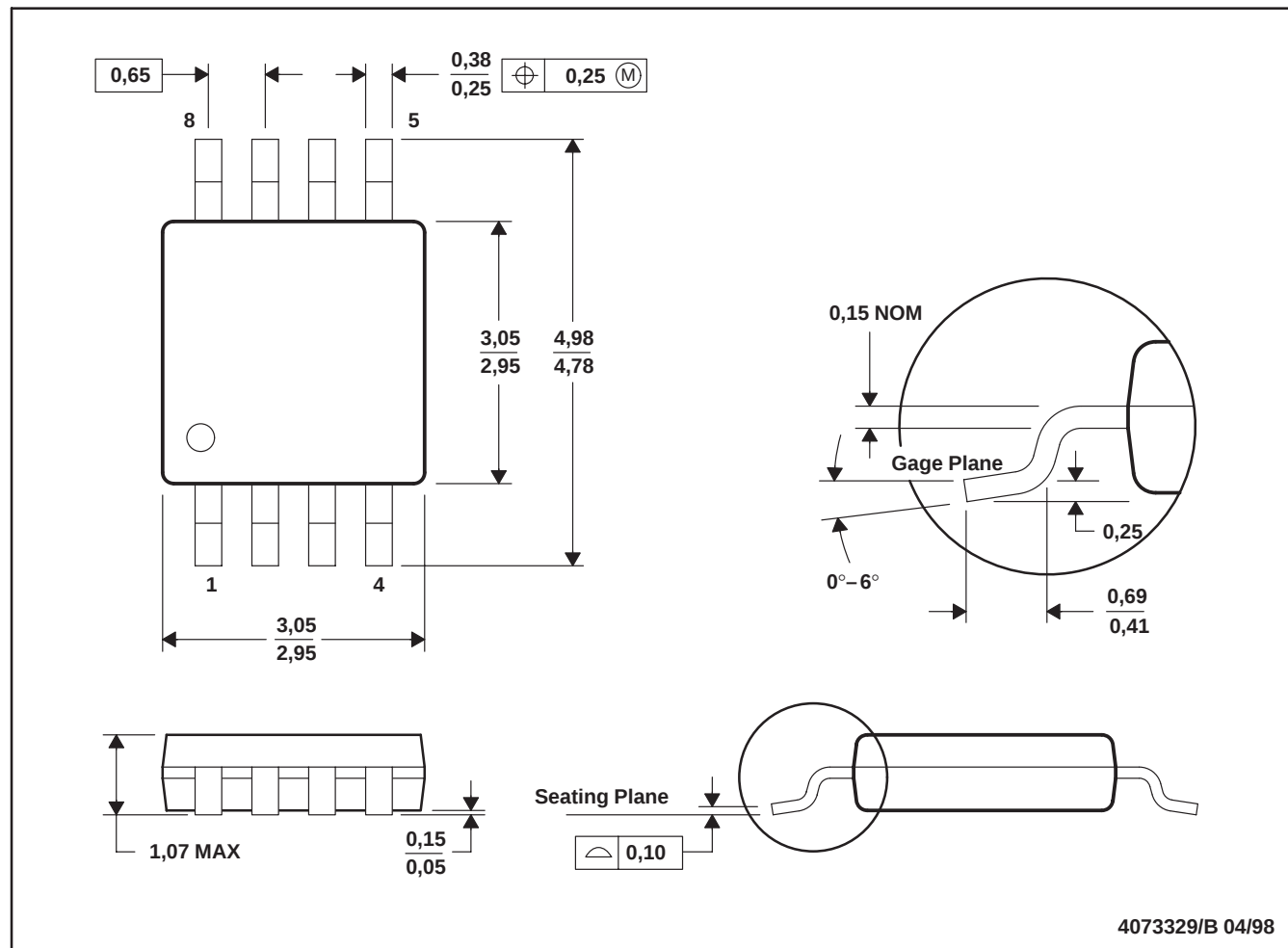
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MECHANICAL INFORMATION

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-187

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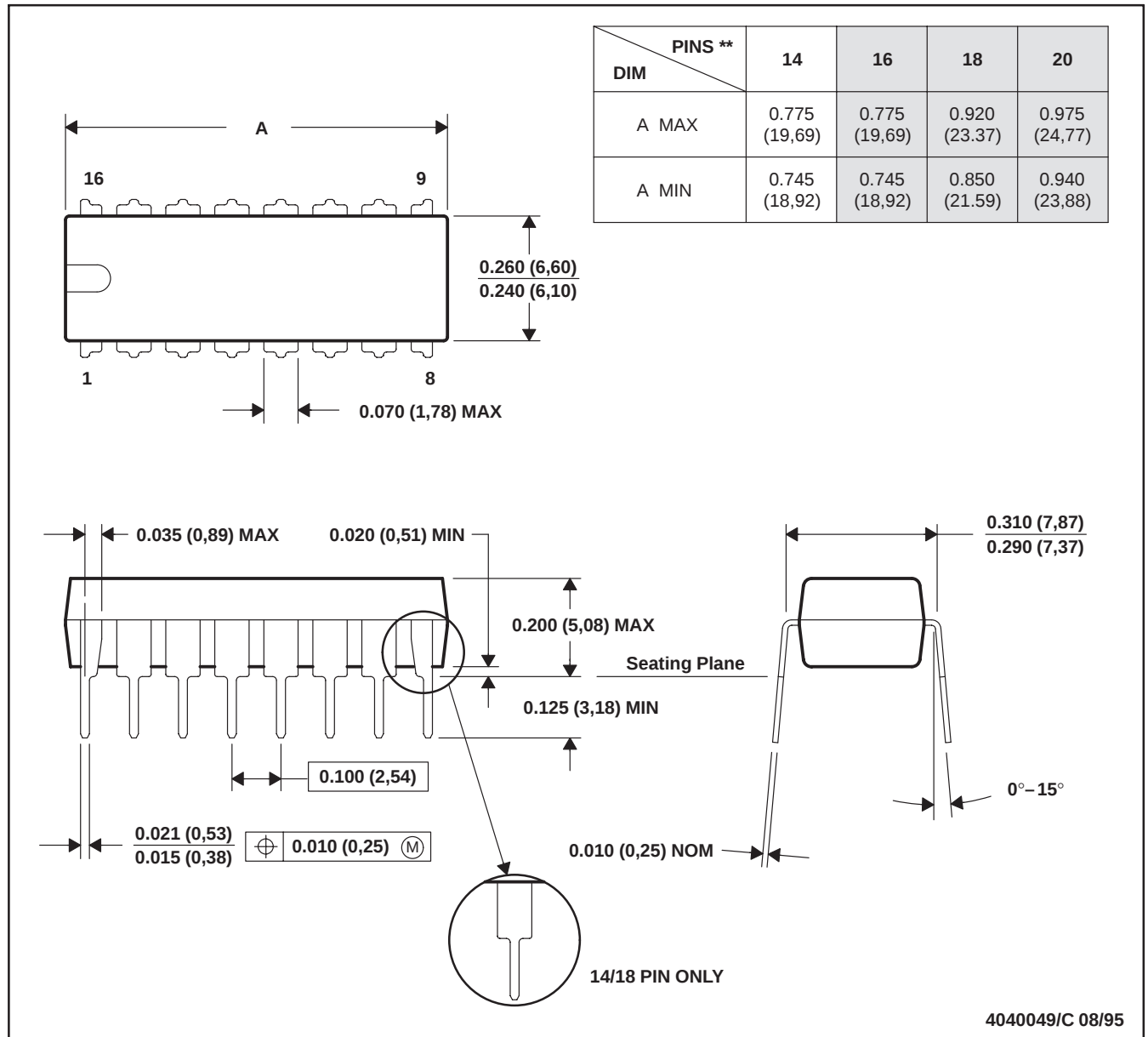
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MECHANICAL INFORMATION

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

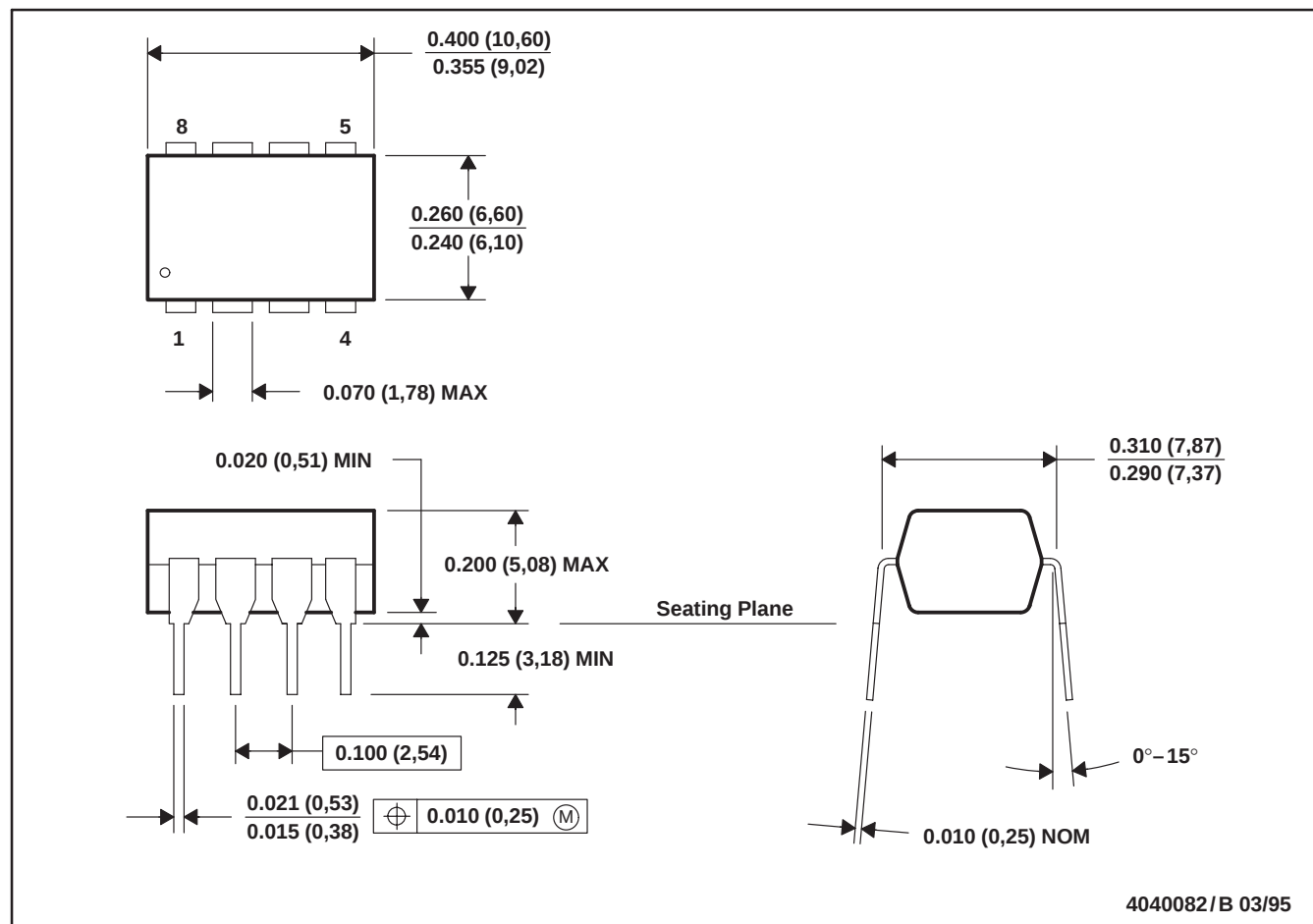
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MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

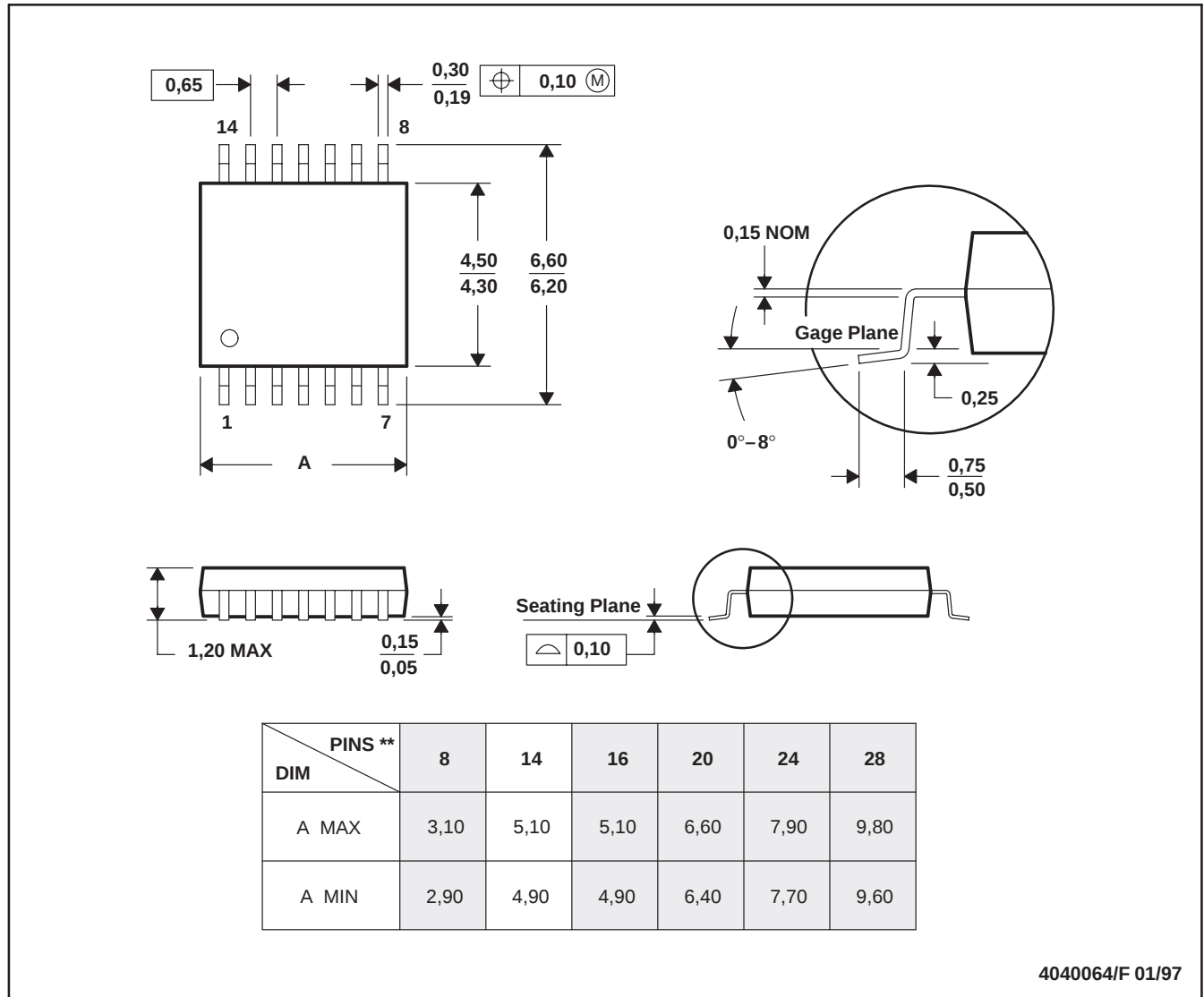
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MECHANICAL INFORMATION

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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