100-W STEREO DIGITAL AMPLIFIER POWER STAGE CONTROLLER

FEATURES

- **Stereo H-Bridge Driver**
- **Efficiency > 95% †**
- **2x100W (RMS) at 6 Ω (BTL) †**
- **4X40W (RMS) at 4 Ω (Single-Ended Output)**
- **THD+N < 0.15% (Typical at 100 W @ 6 Ω, 1 kHz) ‡**
- **Half-Bridge Independent Control for S/E Mode**
- **Glueless Interface to TAS50XX Digital Audio PWM Processors**
- **3.3-V Digital Interface**
- **Overcurrent, Overtemperature, and Undervoltage Protection for External MOSFETs**
- **Low Profile 56-Terminal TSSOP SMD Package**

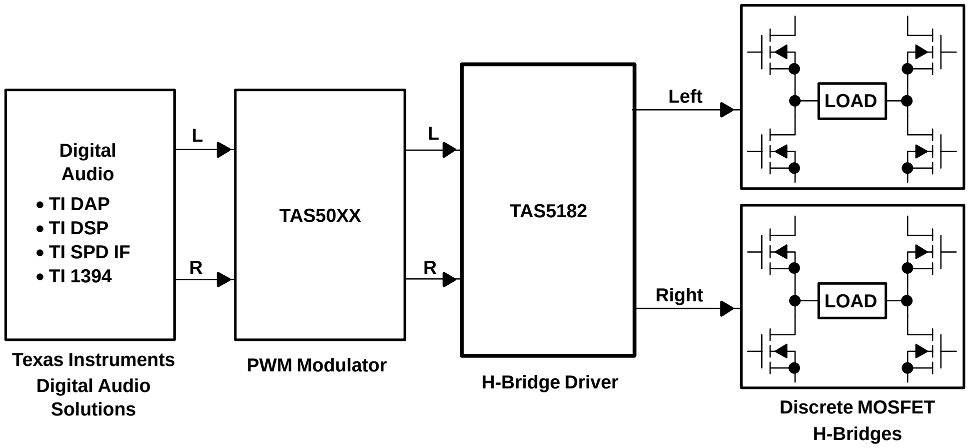
APPLICATIONS

- **AV Receivers**
- **High Power DVD Receivers**
- **Power Amplifiers**
- **Home Theater**
- **Subwoofer Driver**

DESCRIPTION

The TAS5182 device is a high-performance, stereo digital amplifier power stage controller. It is designed to drive two discrete bridge-tied-load (BTL) MOSFET output stages at up to 100 W per channel at 6 Ω. The TAS5182 device, incorporating TI’s Equibit™ technology, is used in conjunction with a digital audio PWM processor (TAS50XX) and two discrete MOSFET H-bridges (4 MOSFETs per H-Bridge) to deliver high-power, true digital audio amplification. The efficiency of this digital amplifier can be greater than 90%, reducing the size of both the power supplies and heat sinks needed. The TAS5182 device accepts a stereo PWM 3.3-V input, and it controls the switching of the discrete H-bridges.

Typical Stereo Audio System Using TAS5182 H-Bridge Driver



Overcurrent, overtemperature, and undervoltage protections are built into the TAS5182 device, safeguarding the H-bridge and speakers against output short-circuit conditions, overtemperature conditions, and other fault conditions that could damage the system.

† When using appropriate MOSFETs.

‡ When using recommended design.

PRODUCT PREVIEW

ORDERING INFORMATION

T_A	PACKAGE
0°C to 70°C	TAS5182DCA

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (T_A) unless otherwise noted(1)

		TAS5182
Supply voltage range	GV_{DD} to GV_{SS}	–0.3 V to 15 V
	DV_{DD} to DV_{SS}	–0.3 V to 3.6 V
AP, AM, BP, BM, CP, CM, DP, DM		–0.3 V to DV_{DD} + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{SHUTDOWN}}$		–0.3 V to DV_{DD} + 0.3 V
BST_A, BST_B, BST_C, BST_D to GV_{SS} for pulse <30 ns		71 V
Switching frequency		1500 kHz
Operating junction temperature range, T_J		150°C
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage range	GV_{DD} to GV_{SS}	7.2	12	15	V
	DV_{DD} to DV_{SS}	3.0	3.3	3.6	V

ELECTRICAL CHARACTERISTICS

T_C = 25°C, DV_{DD} = 3.3 V, GV_{DD} = 12 V, Frequency = 384 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT TEMINALS: AM, AP, BM, BP, CM, CP, DM, DP						
V_{IH}	High input voltage		2			V
V_{IL}	Low input voltage				0.8	V
R_I	Input resistance			50		kΩ
R_{dtp}	Dead time resistor range		0		100	kΩ
INPUT TEMINAL: RESET_X						
V_{IH_RESET}	High input voltage		2			V
V_{IL_RESET}	Low input voltage				0.8	V
GATE DRIVE OUTPUT: GHS_A, GHS_B, GHS_C, GHS_D, GLS_A, GLS_B, GLS_C, GLS_D						
R_{gd}	Gate drive output impedance			3		Ω
I_{oso}	Source current, peak	V_O = 2.0 V		1.2		A
I_{osi}	Sink current, peak	V_O = 2.0 V		1.6		A
BST DIODE						
V_d	Forward current voltage drop	I_d = 100 mA		2		V
SUPPLY CURRENTS						
I_{DVDD}	Operating supply current	No load on gate drive output		3		mA
I_{DVDDQ}	Quiescent supply current	No switching		3		mA
I_{GVDD}	Operating supply current	No load on gate drive output		15		mA
I_{GVDDQ}	Quiescent supply current	No switching		2		mA
VOLTAGE PROTECTION						
$V_{uvp,G}$	Under voltage protection limit, GV_{DD}			7.2		V
CURRENT PROTECTION (VDS SENSING)						
V_{DStrip}	Drain-source voltage protection limit	See *Calculation of Overcurrent Resistor Values*	0.8			V

SWITCHING CHARACTERISTICS

T_C = 25°C, DV_{DD} = 3.3 V, GV_{DD} = 12 V

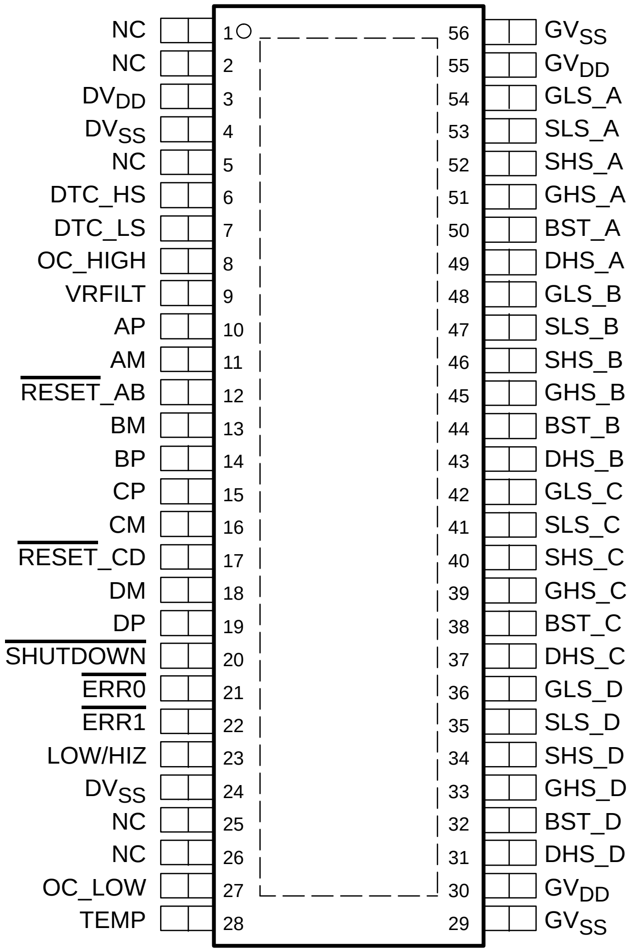
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
TIMING, OUTPUT TERMINALS						
f_{op}	Operating frequency				1500	kHz
$t_{pd,If–O}$	Positive input falling to GHS_x falling	C_L = 1 nF		45		ns
$t_{pd,Ir–O}$	Positive input rising to GLS_x falling	C_L = 1 nF		45		ns
t_{dtp}	Dead time programming range(1)				100	ns
t_{GDr}	Rise time, gate drive output (0.5 to 3.0 V)	C_L = 1 nF		4.5		ns
t_{GDF}	Fall time, gate drive output (9.0 to 3.0 V)	C_L = 1 nF		7		ns
TIMING, PROTECTION, AND CONTROL						
$t_{pd,R–SD}$	Delay, $\overline{\text{RESET}}$ low to $\overline{\text{SHUTDOWN}}$ high			20		ns
$t_{pd,R–LH}$	Delay, $\overline{\text{RESET}}$ low to GDL_x high			45		ns
$t_{pd,R–OP}$	Delay, $\overline{\text{RESET}}$ high to operation state			50		ns
$t_{pd,E–L}$	Delay, error event to all gates low			180		ns
$t_{pd,E–SD}$	Delay, error event to $\overline{\text{SHUTDOWN}}$ low			170		ns

(1) Dead time programming definition: Adjustable delay from AP (BP, CP, or DP) rising edge to GHS_A (GHS_B, GHS_C, or GHS_D) rising edge, and AM (BM, CM, or DM) rising edge to GLS_A (GLS_B, GLS_C, or GLS_D) rising edge.

PRODUCT PREVIEW

PIN ASSIGNMENTS

**DCA PACKAGE
(TOP VIEW)**



NC – No internal connection
Exposed pad size is 106 x 204 mils

Terminal Functions

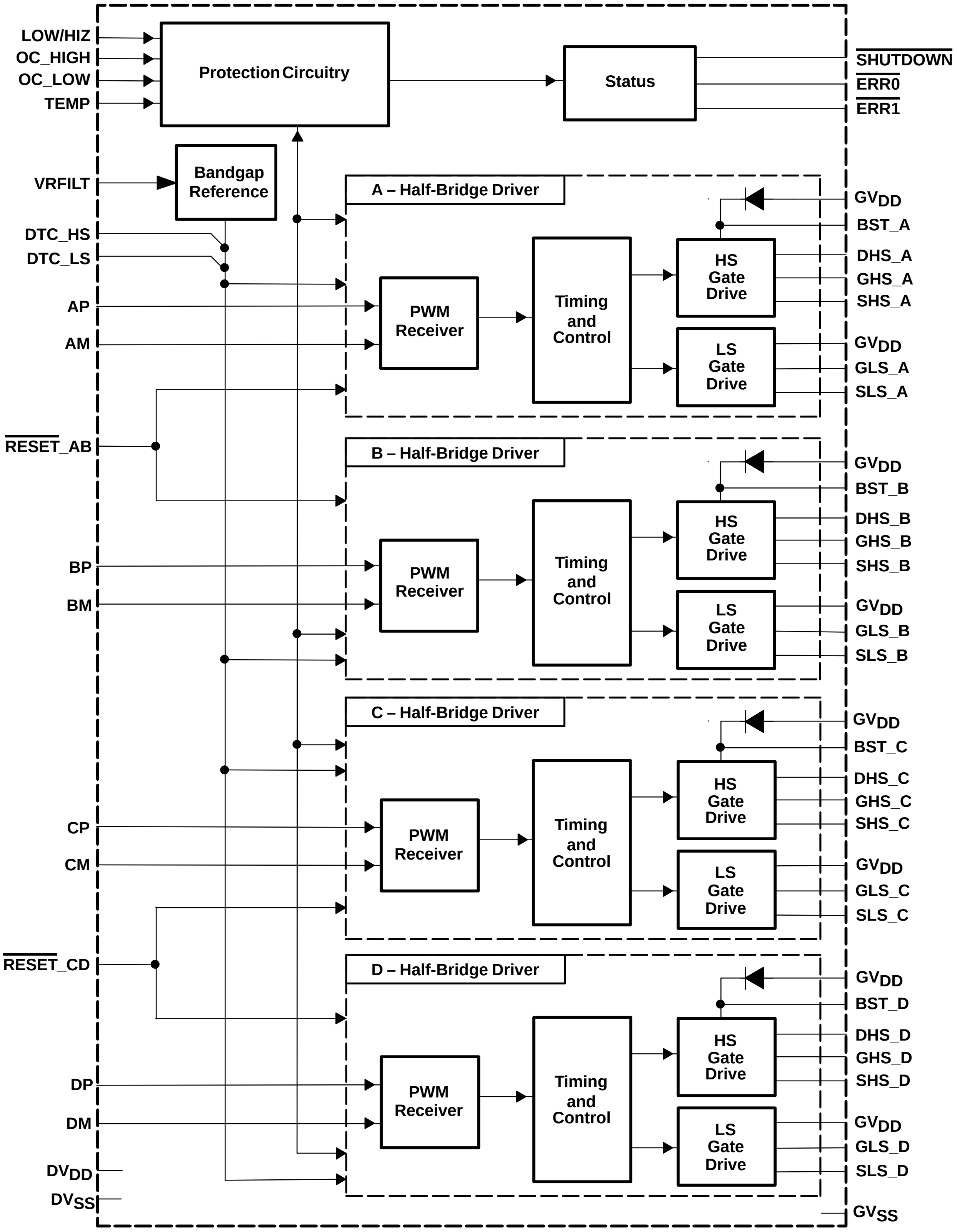
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AM	11	I	PWM input signal (negative), half-bridge A
AP	10	I	PWM input signal (positive), half-bridge A
BM	13	I	PWM input signal (negative), half-bridge B
BP	14	I	PWM input signal (positive), half-bridge B
BST_A	50	I	High-side bootstrap supply (BST), external capacitor to SHS_A required
BST_B	44	I	High-side bootstrap supply (BST), external capacitor to SHS_B required
BST_C	38	I	High-side bootstrap supply (BST), external capacitor to SHS_C required
BST_D	32	I	High-side bootstrap supply (BST), external capacitor to SHS_D required
CM	16	I	PWM input signal (negative), half-bridge C
CP	15	I	PWM input signal (positive), half-bridge C
DM	18	I	PWM input signal (negative), half-bridge D
DP	19	I	PWM input signal (positive), half-bridge D

Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
DHS_A	49	I	High-side drain connection, used for high-side V$_{DS}$ sensing
DHS_B	43	I	High-side drain connection, used for high-side V$_{DS}$ sensing
DHS_C	37	I	High-side drain connection, used for high-side V$_{DS}$ sensing
DHS_D	31	I	High-side drain connection, used for high-side V$_{DS}$ sensing
DTC_HS	6	I	High-side dead-time programming, external resistor to DV$_{SS}$ required
DTC_LS	7	I	Low-side dead-time programming, external resistor to DV$_{SS}$ required
DV$_{DD}$	3	P	Logic supply voltage
DV$_{SS}$	4, 24	P	Digital ground, reference for input signals
$\overline{\text{ERR0}}$	21	O	Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor.
$\overline{\text{ERR1}}$	22	O	Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor.
GHS_A	51	O	Gate drive output for high-side MOSFET, half-bridge A
GHS_B	45	O	Gate drive output for high-side MOSFET, half-bridge B
GHS_C	39	O	Gate drive output for high-side MOSFET, half-bridge C
GHS_D	33	O	Gate drive output for high-side MOSFET, half-bridge D
GLS_A	54	O	Gate drive output for low-side MOSFET, half-bridge A
GLS_B	48	O	Gate drive output for low-side MOSFET, half-bridge B
GLS_C	42	O	Gate drive output for low-side MOSFET, half-bridge C
GLS_D	36	O	Gate drive output for low-side MOSFET, half-bridge D
GV$_{DD}$	30, 55	P	Gate drive voltage supply terminal
GV$_{SS}$	29, 56	P	Gate drive voltage supply ground return
LOW/HIZ	23	I	Logic signal that determines the drive output state during a reset. When $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ is low, LOW/HIZ = 1 indicates that the outputs are low impedance LOW/HIZ = 0 indicates that the outputs are high impedance
NC	1, 2, 5, 25, 26		Not connected. Terminals 1, 2, 5, 25, and 26 may be connected to DV$_{SS}$.
OC_HIGH	8	I	High-side overcurrent trip value programming, external resistors to DV$_{SS}$ and VRFILT are required
OC_LOW	27	I	Low-side overcurrent trip value programming, external resistors to DV$_{SS}$ and VRFILT are required
$\overline{\text{RESET\_AB}}$	12	I	Reset signal half-bridge A and B, active low
$\overline{\text{RESET\_CD}}$	17	I	Reset signal half-bridge C and D, active low
$\overline{\text{SHUTDOWN}}$	20	O	Error/warning report indicator. This output is open drain with internal pull-up resistor.
SHS_A	52	I	High-side source connection, used as BST floating ground (and high-side V$_{DS}$ sensing)
SHS_B	46	I	High-side source connection, used as BST floating ground (and high-side V$_{DS}$ sensing)
SHS_C	40	I	High-side source connection, used as BST floating ground (and high-side V$_{DS}$ sensing)
SHS_D	34	I	High-side source connection, used as BST floating ground (and high-side V$_{DS}$ sensing)
SLS_A	53	I	Source connection low-side MOSFET, ground return terminal, half-bridge A
SLS_B	47	I	Source connection low-side MOSFET, ground return terminal, half-bridge B
SLS_C	41	I	Source connection low-side MOSFET, ground return terminal, half-bridge C
SLS_D	35	I	Source connection low-side MOSFET, ground return terminal, half-bridge D
TEMP	28	I	External temperature sensing connection
VRFILT	9	I	Bandgap reference = 1.8 V. Capacitor must be connected from VRFILT to DV$_{SS}$.

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS

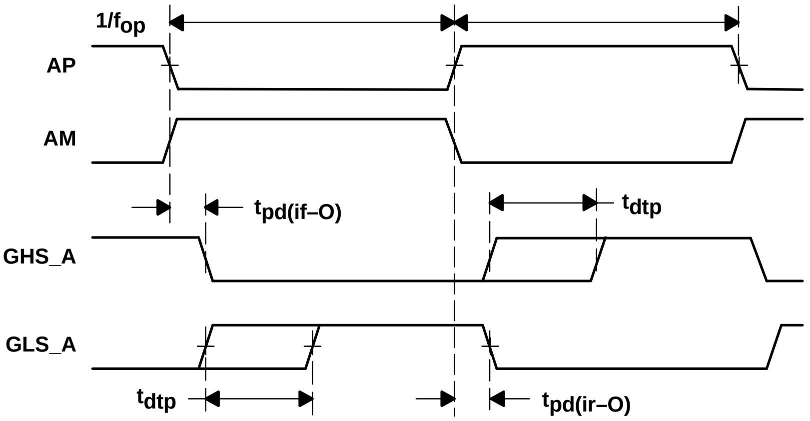


Figure 1. PWM Input to Gate Drive Output Timing (Same for A, B, C, and D Half-Bridge Drivers)

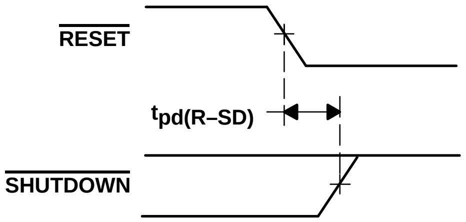


Figure 2. $\overline{\text{RESET}}$ to $\overline{\text{SHUTDOWN}}$ Propagation Delay

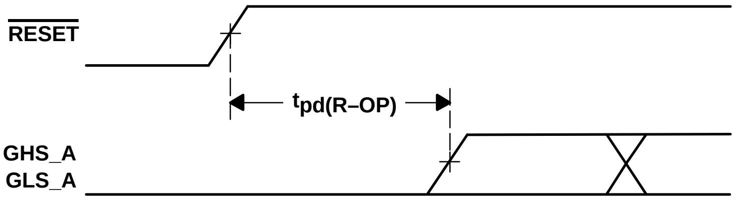
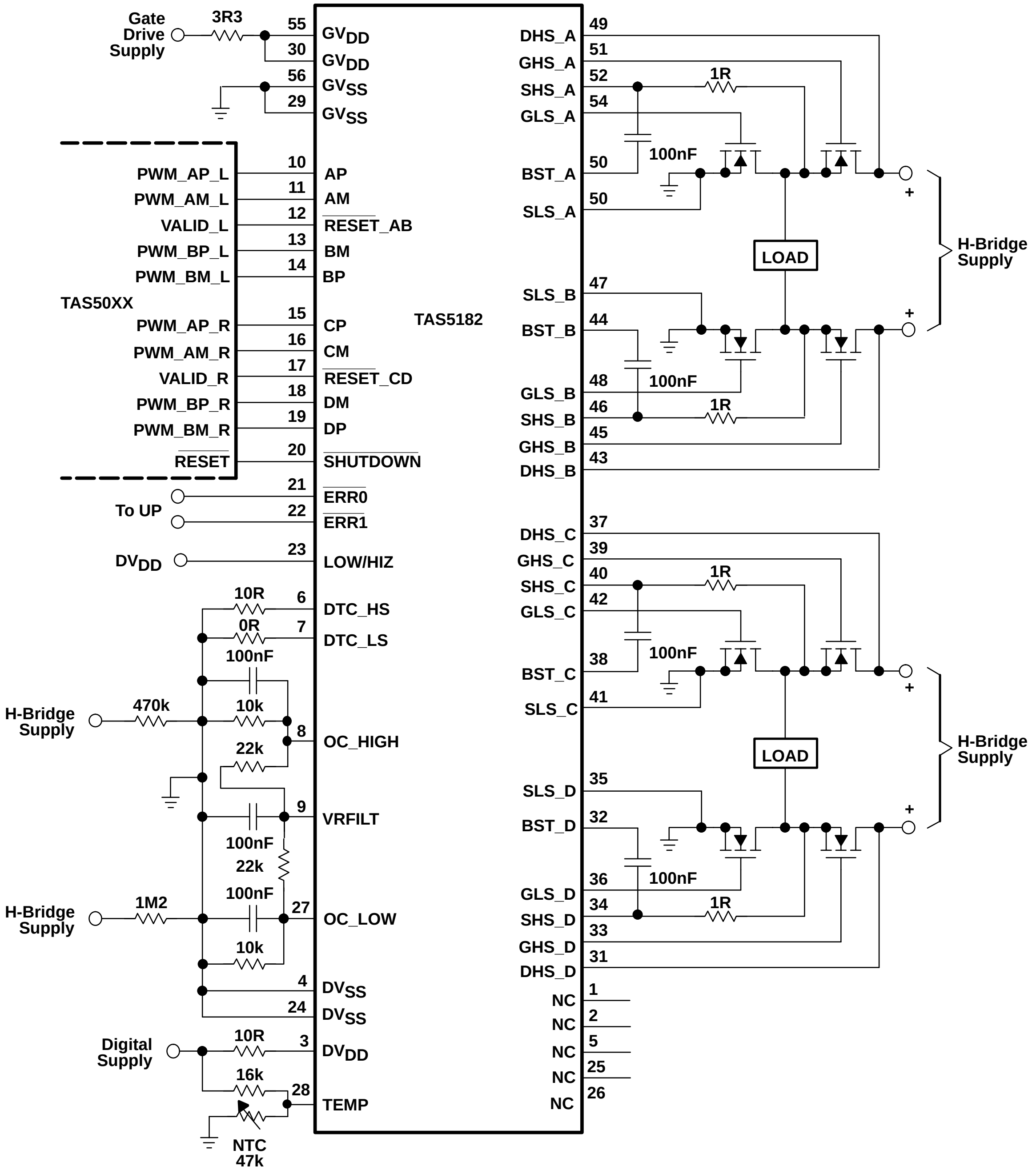


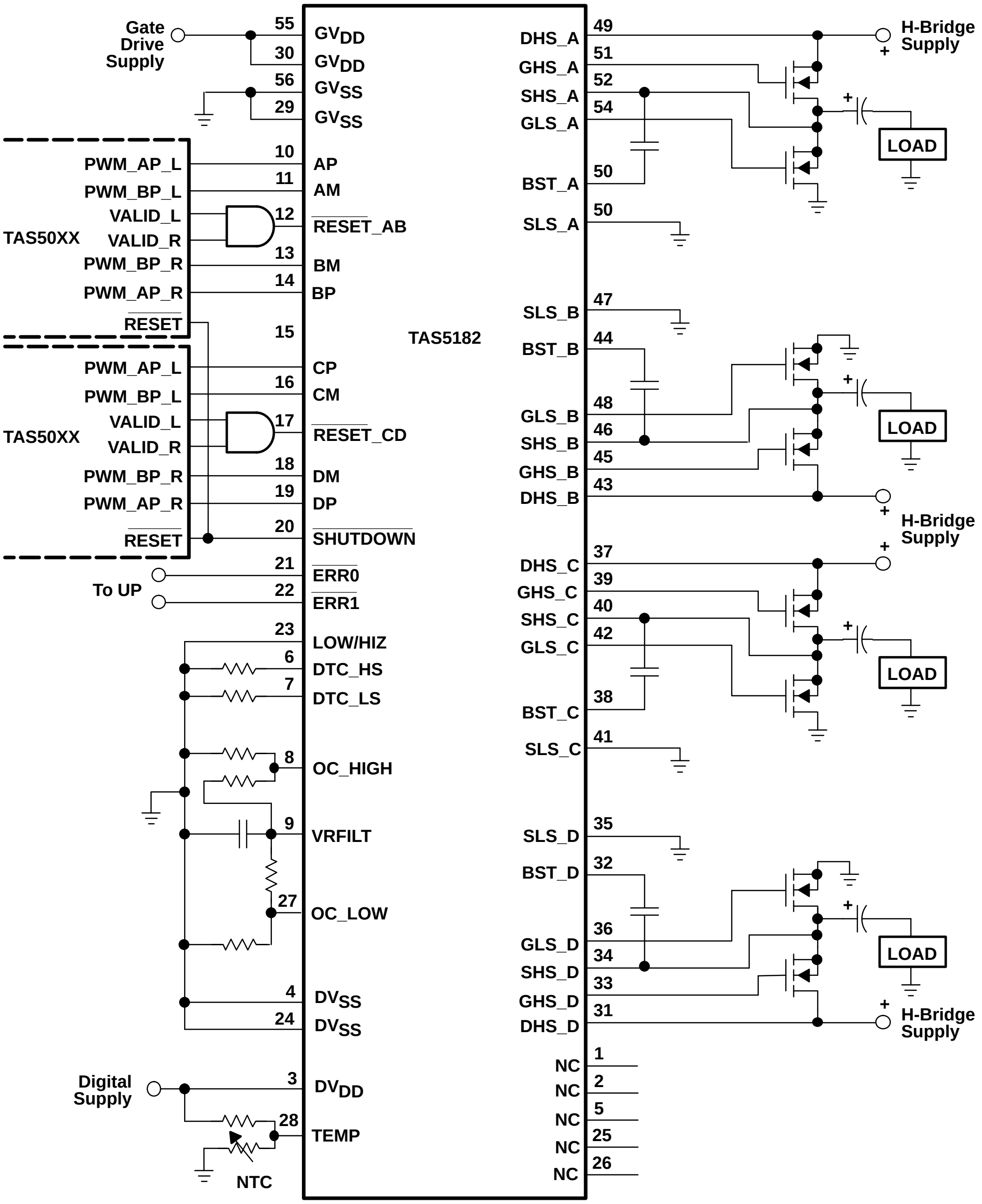
Figure 3. $\overline{\text{RESET}}$ to Gate Drive Output Propagation Delay (Same for Half-Bridge A, B, C, and D)

TYPICAL APPLICATION CONNECTION DIAGRAM (BRIDGE-TIED-LOAD CONFIGURATION)



NOTE: Recommended power MOSFETs
(1) International Rectifier IRFIZ24N (8 places)

TYPICAL APPLICATION CONNECTION DIAGRAM (SINGLE-ENDED CONFIGURATION)



NOTE: Recommended power MOSFETs
(1) International Rectifier IRFIZ24N (8 places)

FUNCTIONAL DESCRIPTION

Power Stage Protection

The TAS5182 device provides overcurrent, overtemperature, and undervoltage protection for the MOSFET power stage.

Overcurrent Protection (OCP)

To protect the power stage from damage due to high currents, a V_{DS} sensing system is implemented in the TAS5182 device. Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated which, when exceeded, triggers the protection latch, causing the $\overline{\text{SHUTDOWN}}$ terminal to go low. This voltage threshold is resistor programmable. See application section *Calculation of Overcurrent Resistor Values* for more details.

Overtemperature Protection (OTP)

The TAS5182 device has a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. See application section *Overtemperature Programming Circuit* for implementation details.

Undervoltage Protection (UVP)

To protect the power output stage during start-up, shutdown, and other possible undervoltage conditions, the TAS5182 device provides power stage undervoltage protection by driving its outputs low whenever GV_{DD} is under 7 V. With the TAS5182 outputs driven low, the MOSFETs go to a high-impedance state.

Control Terminals

The TAS5182 device provides input control terminals to reset each audio channel and also to control the electrical characteristics of the MOSFET output power stage.

Channel Reset

The reset function enables operation after power up, re-enables operation after an error event, and disables the MOSFET output stage switching during power down and mute. The falling edge of $\overline{\text{RESET}}$_AB (left audio channel) or $\overline{\text{RESET}}$_CD (right audio channel) causes the TAS5182 device to reset. Normal operation is resumed when the reset signals go high.

MOSFET Output Reset Control

The LOW/HIZ control terminal selects whether the MOSFET output stage goes into a high-impedance (HI-Z) state or LOW-LOW state when $\overline{\text{RESET}}$_AB or $\overline{\text{RESET}}$_CD is enabled. In the high-impedance state, the low-side and high-side MOSFETs are turned off causing no current flow through the MOSFETs. This effectively disconnects the load from the power supply rail. In the LOW-LOW state, the low-side MOSFETs are turned on, while the high-side MOSFETs are turned off. This causes a low or ground signal to be output to the load.

Status Terminals

The TAS5182 device provides output status terminals to report overcurrent, overtemperature, and undervoltage warnings and errors.

Shutdown Indicator

The $\overline{\text{SHUTDOWN}}$ terminal indicates an error event has occurred such as overcurrent, overtemperature, or undervoltage. The $\overline{\text{SHUTDOWN}}$ terminal is pulled high when $\overline{\text{RESET}}$_AB or $\overline{\text{RESET}}$_CD is asserted. $\overline{\text{ERR0}}$ and $\overline{\text{ERR1}}$ terminals along with the $\overline{\text{SHUTDOWN}}$ terminal indicate the type of warnings and errors. Note that $\overline{\text{SHUTDOWN}}$ is an open-drain signal. See Table 1 for a functional description of these signals.

Table 1. TAS5182 Status Signals

$\overline{\text{ERR0}}$	$\overline{\text{ERR1}}$	$\overline{\text{SHUTDOWN}}$	DESCRIPTION
0	0	0	Multiple errors (TAS5182 gate outputs low, MOSFET outputs HI-Z)
0	0	1	Not valid
0	1	0	Overtemperature error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
0	1	1	Overtemperature warning (normal operation)
1	0	0	Overcurrent error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
1	0	1	Not valid
1	1	0	GV_{DD} undervoltage error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
1	1	1	Normal operation

TAS5182 Power Up and Reset

After power up all gate drive outputs are held low (i.e., the error latch is set). Normal operation can be initiated by toggling $\overline{\text{RESET}}$_AB and/or $\overline{\text{RESET}}$_CD from a low state to a high state. If no errors are present, then the TAS5182 device is ready to accept audio inputs.

TAS5182 Reset and Error Timing

The TAS5182 device provides two output control configurations for reset and error situations. In a BTL system configuraton, the MOSFET outputs must be grounded before resuming normal operation. This enables the bootstrap capacitors to charge. In a single-ended system configuration, the MOSFET outputs must be brought to a high-impedance state before resuming normal operation. This helps reduce pops in the single-ended ac-coupled system.

Reset and Error Timing (BTL System)

When using this device in the BTL configuration, it is advisable to bring the MOSFET outputs to a low-low (ground) state when reset ($\overline{\text{RESET}}$_AB or $\overline{\text{RESET}}$_CD) is asserted. Figure 4 shows the timing that occurs in this configuration. This feature is enabled by connecting the LOW/HIZ terminal to DV_{DD}.

When an error event occurs (see Table 1), and following propagation delay $t_{pd(E–SD)}$, the TAS5182 device pulls the $\overline{\text{SHUTDOWN}}$ signal low. The falling edge of $\overline{\text{SHUTDOWN}}$ forces the MOSFET outputs into a high-impedance state. The $\overline{\text{SHUTDOWN}}$ signal is usually connected to the $\overline{\text{RESET}}$ terminal of the TAS50XX PWM controller. After some delay, the controller then asserts the TAS5182 $\overline{\text{RESET}}$ terminal low. The falling edge of $\overline{\text{RESET}}$ forces the MOSFET ouputs to ground potential (this event also brings the $\overline{\text{SHUTDOWN}}$ signal high). This allows the bootstrap capacitors to charge through the grounded MOSFET outputs. When $\overline{\text{RESET}}$ is pulled high, the system resumes normal operation.

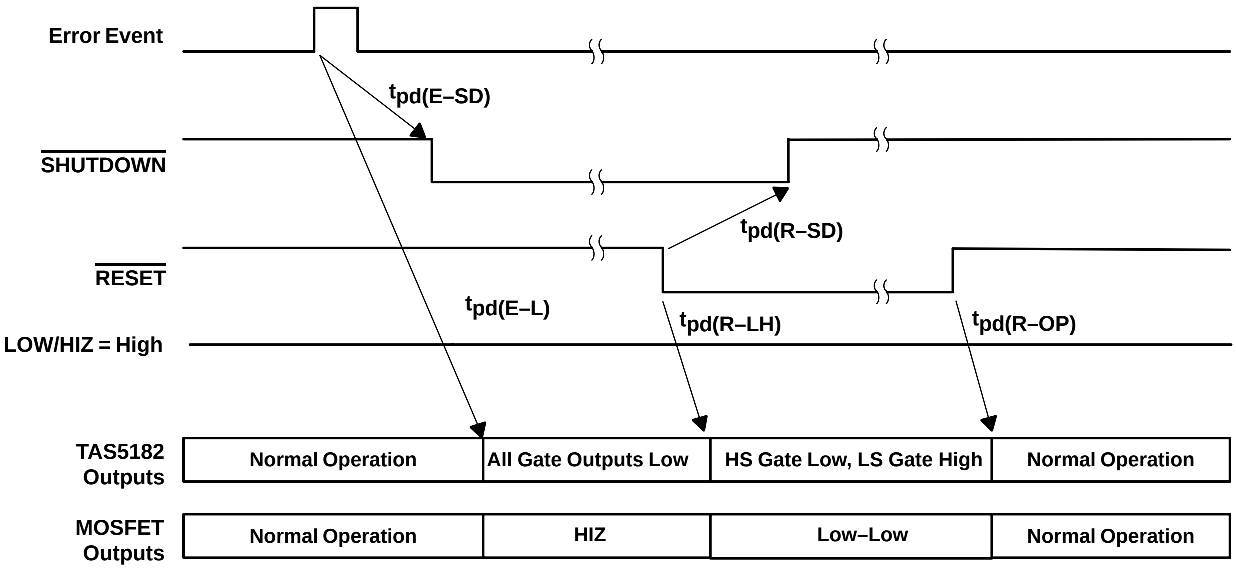


Figure 4. Reset and Error Timing (BTL System)

Reset and Error Timing (Single-Ended System)

When using this device in the single-ended configuration, it is advisable to bring the MOSFET outputs to a high-impedance state when reset ($\overline{\text{RESET}}$_AB or $\overline{\text{RESET}}$_CD) is asserted. Figure 5 shows the timing that occurs in this configuration. This feature is enabled by connecting the LOW/HIZ terminal to DV_{SS}.

When an error event occurs (see Table 1), and following propogation delay *a*, the TAS5182 device pulls the $\overline{\text{SHUTDOWN}}$ signal low. The falling edge of $\overline{\text{SHUTDOWN}}$ forces the MOSFET outputs into a high-impedance state. The $\overline{\text{SHUTDOWN}}$ signal is usually connected to the $\overline{\text{RESET}}$ terminal of the TAS50XX PWM controller. The MOSFET outputs remain in a high-impedance allowing the dc-blocking output capacitors to remain charged thereby reducing the possibility of pops. When $\overline{\text{RESET}}$ is pulled high, the system resumes normal operation.

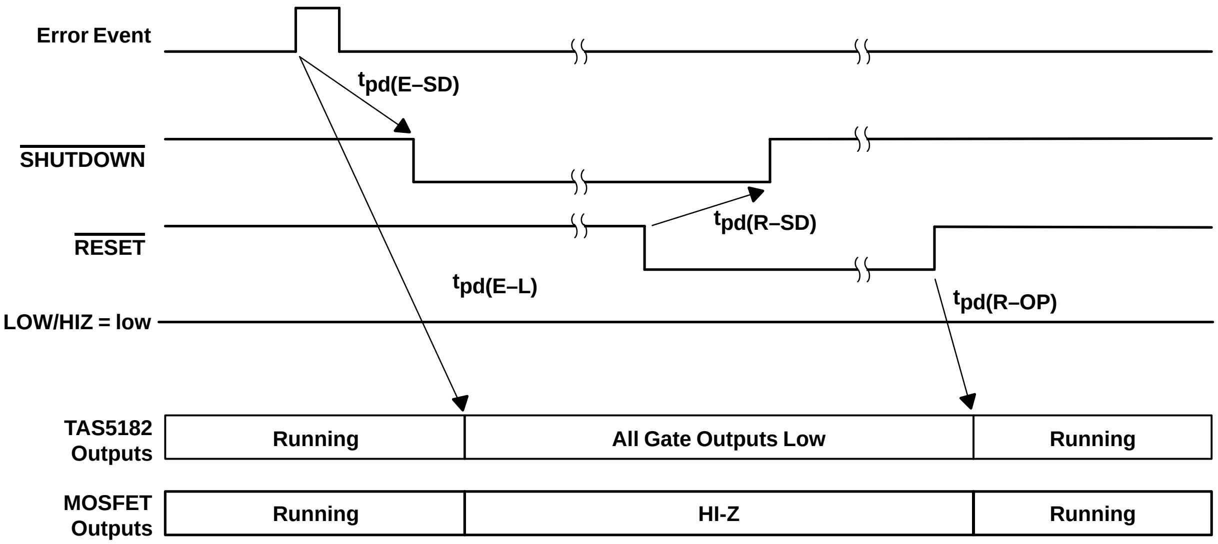


Figure 5. Reset and Error Timing (Single-Ended System)

Calculation of Overcurrent Resistor Values

The output current flows through internal resistance $R_{DS(on)}$ of the external MOSFETs, which creates voltage drop V_{DS}. The overcurrent detector senses this voltage to trigger an error event. To set this overcurrent limit (I_{DS}), equation (1) can be used as an approximation. The exact current limit depends on parasitics from the PCB layout, resistance of the MOSFET at the operation temperature, and the configuration of the H-bridge output stage.

	PROGRAMMING VOLTAGE	OUTPUT INDUCTOR SHUTDOWN CURRENT RANGE(1)
OCL	0.80 V (terminal 27)	–15 to –19 A
OCH	1.14 V (terminal 8)	21 to 25 A

(1) Measured on TI TAS5182 evaluation module (EVM).

Board configuration:

- 1R0 rsisters on SHS and GLS connections
- GV_{DD} = 12 V, PV_{DD} = 40V
- 10BQ030 voltage clamp diodes across TT snubber inductors
- TT snubbers: 4 turns (60 nH), 10 nF, 5R4

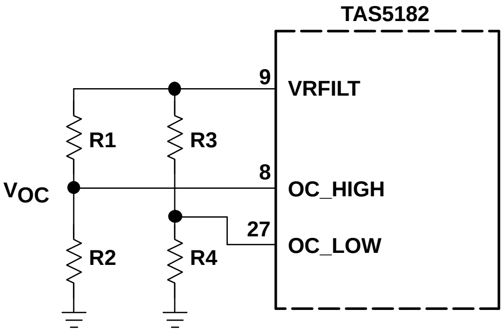


Figure 6. Overcurrent Programming Circuit

Overtemperature Programming Circuit

The TAS5182 device features a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. Figure 7 shows a typical application.

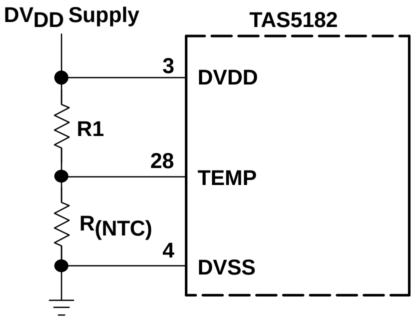


Figure 7. Temperature Sensing Circuit

The temperature protection system has two trigger limits: OT warning and OT error. OT warning occurs when the voltage at the TEMP terminal is approximately 36% of DV_{DD}. OT error occurs when the voltage at the TEMP terminal is approximately 23% of DV_{DD}. OT warning is decoded when $\overline{ERR0}$ = 0, $\overline{ERR1}$ = 1, and $\overline{SHUTDOWN}$ = 1. OT error is decoded when $\overline{ERR0}$ = 0, $\overline{ERR1}$ = 1, and $\overline{SHUTDOWN}$ = 0. The user for a particular application determines the values of R1 and R_{NTC}. Typical values are R1 = 10 kΩ and R_{NTC} = 47 kΩ.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin HTSSOP, but includes a thermal pad (see Figure 8) to provide an effective thermal contact between the IC and the PCB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have two shortcomings: they do not address the low profile requirements (< 2 mm) of many of today's advanced systems, and they do not offer a terminal count high enough to accomodate increasing integration. On the other hand, traditional low-power, surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits

The PowerPAD™ package (thermally enhanced HTSSOP) combines fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PCB. Because of the very small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered to the PCB, good power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved. Refer to Reference 4 for recommended soldering procedure.

THERMAL DATA

PARAMETER		MIN	TYP	MAX	UNIT
Maximum junction temperature, $T_{J(SD)}$		150			°C
Operating temperature, TC	Commercial	0	25	70	°C
	Industrial	–40	25	85	°C
Thermal resistance, θjc	Pad with solder (1)	0.27			°C/W
Thermal resistance, θja		21.17			°C/W
Thermal resistance, θjc	Pad without solder (1)	0.27			°C/W
Thermal resistance, θja		36.42			°C/W

(1) Values taken from Page 31, Table 6, *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002. Refer to pages 32 and 33 for a description of the printed circuit board (PCB) used for these measurements. Note that the PCB used for these measurements is not the recommended PCB for TAS5182 applications but is cited here for reference only.

Power Dissipation

The equation for TAS5182 power dissipation using N external MOSFETs is:

$P_d = V_{gd} * Q_g * f * N$

where:

V_{gd} = GVDD (typically 12V)

Q_g = MOSFET gate charge

f = operating frequency

N = number of external MOSFETs driven (8 for two channel operation)

Example power dissipation calculation:

Given a TAS5182 system with 8 external IRFIZ24N MOSFETs and GVDD = 12 V. The power dissipation is:

$P_d = V_{gd} * Q_g * f * N = 12V * 22.5nC * 384\ kHz * 8 = 0.8\ W$

Note: Lab measurements yield power dissipation of 0.8 W (PVDD = 40 V).

REFERENCES

1. T*AS5000 Digital Audio PWM Process* data manual, TI Literature Number SLAS270
2. *System Design Considerations for True Digital Audio Power Amplifiers,* TI Literature Number SLAA117
3. *Digital Audio Measurements,* TI Literature Number SLAA114
4. *PowerPAD Thermally Enhanced Package,* TI Literature Number SLMA002

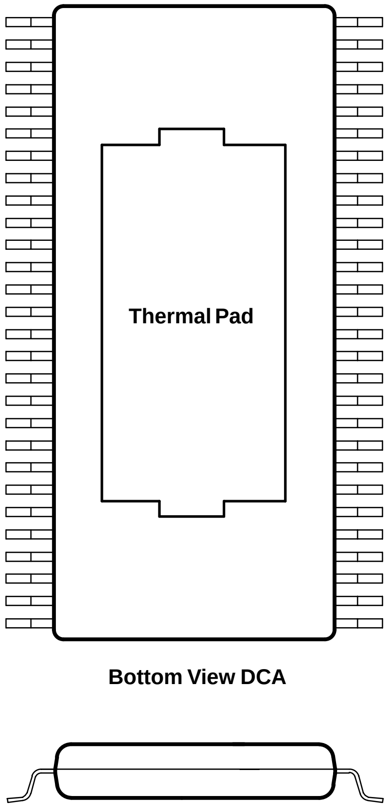
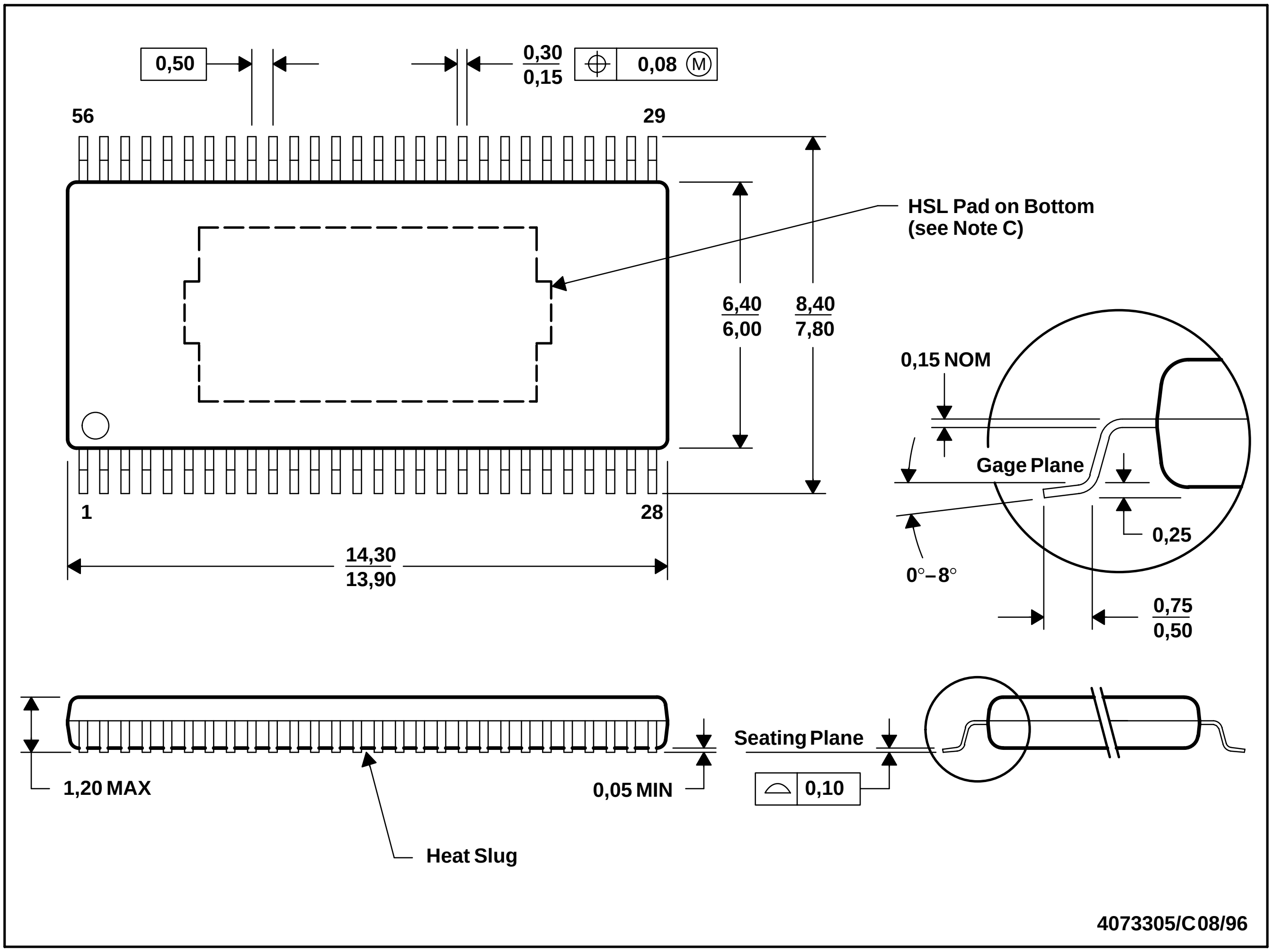


Figure 8. Views of Thermally Enhanced DCA Package

DCA (R-PDSO-G56) **PowerPad™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a exposed heat slug (HSL) on bottom.

PowerPad is a trademark of Texas Instruments Incorporated.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated