

TDAT04622 SONET/SDH 155/622 Mbits/s Data Interface

Features

- Point-to-point path termination device for interface termination.
- Versatile IC supports 155/622 Mbits/s SONET/SDH interface solutions for packet over SONET (POS), asynchronous transfer mode (ATM), or simplified data link (SDL) for data over fiber applications.
- Supports point-to-point and multi-PHY UTOPIA.
- Low-power 3.3 V operation, CMOS technology.
- High-speed I/O is LVPECL. All other logic has 5 V tolerant TTL-level inputs.
- -40 °C to +85 °C temperature range.
- 600 LBGA package.

SONET/SDH Interface

- Termination of quad STS-3/STM-1 or single-channel STS-12/STM-4.
- Supports overhead processing for transport and path overhead bytes.
- Optional insertion and extraction of overhead bytes via serial overhead interface.
- Full path termination and SPE extraction/insertion.
- SONET/SDH compliant condition and alarm reporting.
- Handles all concatenation levels of STS-3c through STS-12c, STM-1 through STM-4.
- Built-in diagnostic loopback modes.
- Compliant with the following Bellcore, ANSI*, and ITU standards:
 - GR-253 CORE: SONET Transport Systems: Common Generic Criteria.

- ITU-T G.707: Network Node Interface for the Synchronous Digital Hierarchy.
- ITU-T G.803: Architecture of Transport Networks Based on the Synchronous Digital Hierarchy.
- T1.105: SONET-Basic Description including Multiplex Structure, Rates and Formats.
- T1.105.02 SONET-Payload Mappings.
- T1.105.03 SONET-Jitter at Network Interfaces.
- T1.105.06 SONET Physical Layer Specifications.
- T1.105.07 SONET-Sub-STS-1 Interface Rates and Formats Specification.
- ITU-T I.432: B-ISDN User-Network Interface-Physical Layer Specification.
- IETF RFC 1619: PPP over SONET/SDH.
- IETF RFC 1661: The Point-to-Point Protocol (PPP).
- IETF RFC 1662: PPP in HDLC-like Framing.

Data Processing

- Provisionable data engine supports payload insertion/extraction and CRC-16/-32 generation/verification for ATM cell or PPP, SDL, or HDLC streams.
- Maintains counts for cell/packet traffic (e.g., total number of cells, number of discarded cells).
- Integrated UTOPIA Level 2- and UTOPIA Level 3-compatible ATM physical layer interface with packet extensions for test and operations.
- Insertion and extraction of up to four separate data channels in STS-3/STM-1, and one data channel in STS-12/STM-4.
- Compliant with 1998: ATM Forum, ITU standards, and IETF standards.

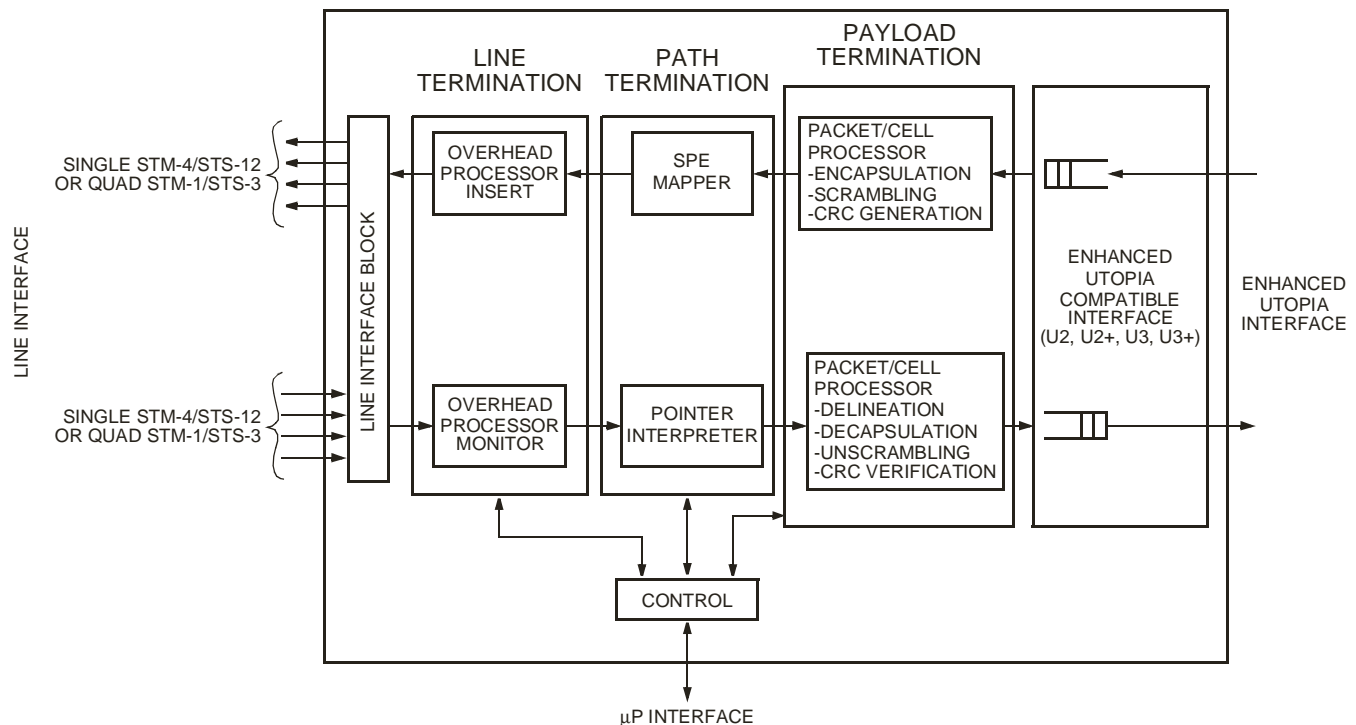
Microprocessor Interface

- 16-bit address and 16-bit data interface with up to 66 MHz read and write access.
- Compatible with most industry-standard processors.

*ANSI is a registered trademark of American National Standards Institute, Inc.

Description

The TDAT04622 SONET/SDH interface device provides a versatile solution for quad STS-3/STM-1 or single STS-12/STM-4 point-to-point datacom/telecom applications. Constructed using Agere Systems' state-of-the-art CMOS technology, this device incorporates integrated SONET/SDH framing, section and line overhead insertion and extraction, path termination, and generation.



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Figure 1. Overview Block Diagram

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