Application Note
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microelectronics group

Lucent Technologies
Bell Labs Innovations

T8502 and T8503 Dual PCM Codecs with Filters

Introduction

Lucent Technologies Microelectronics Group's T8502 and T8503 devices are monolithic, two-channel PCM codecs with filters. These integrated circuits provide the A/D and D/A conversion and the filtering necessary to interface a voice telephone circuit to a time-division multiplexed system using a standard PCM interface. The analog architecture minimizes pinout, allowing the codec to be assembled in a small 20-pin SOJ or SOG package that requires minimal board area. Features include extremely flexible time-slot assignment, delayed (T8502) or nondelayed (T8503) timing mode, pin-selectable μ-law or A-law companding, pin-selectable receive gains, low-power +5 V only operation, automatic powerdown, and automatic adaptation to master clock frequencies of either 2.048 MHz or 4.096 MHz. For added flexibility in interfacing with transmission systems, each channel also provides an uncommitted op amp that can be programmed for transmit gain using external resistors.

These devices are fabricated in Lucent's high-performance analog CMOS technology with double-poly capacitors. Coding and decoding are performed using charge redistribution with successive approximation. Gain, termination impedance, and hybrid balance are set by external components. These codecs are ideal for high-density circuit-board applications where high integration, low crosstalk, and minimal cost are required.

Digital Interface

The digital interfacing to the device consists of the PCM interface block, the internal timing and control block, and the gain control block. See Figure 1 for a functional block diagram of this codec.

PCM Interface

The PCM interface block administers transmit and receive PCM data as well as frame sync controlling.

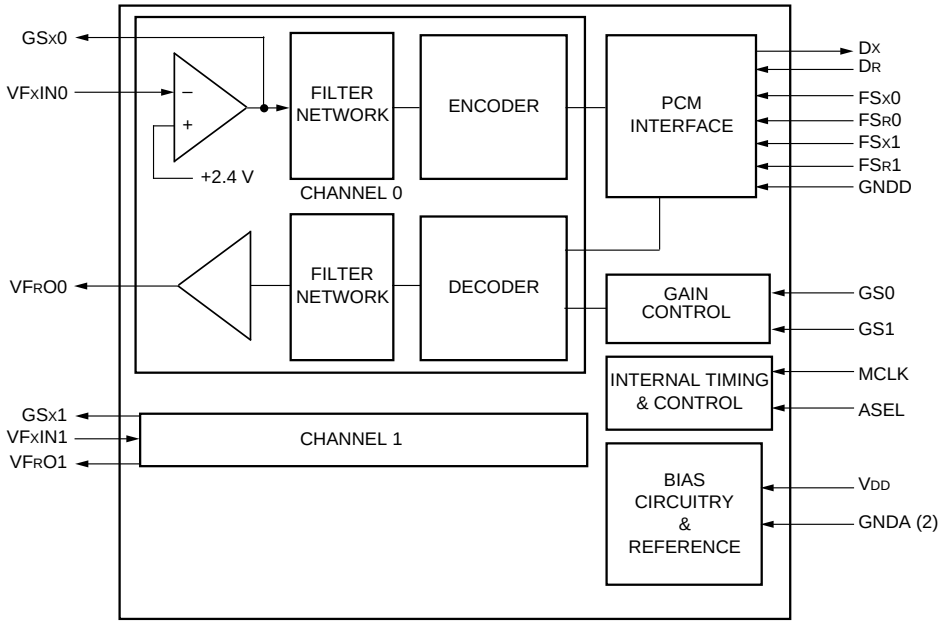

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Figure 1. Functional Block Diagram

Digital Interface (continued)

PCM Data

PCM data occurs once every 125 µs frame period. The frame period is the standard set by doubling the telephone channel bandwidth of 4000 Hz, to provide a minimum sampling rate of 8000 samples per second (Nyquist criterion). The codecs provide fixed data rate timing. Data clocks at the master clock rate (MCLK). In a frame period, there are 32 data time slots when a 2.048 MHz MCLK rate is used and 64 data time slots when a 4.096 MHz MCLK rate is used. Each time slot contains eight clock cycles. Data is transmitted and received serially with the first bit (bit 1) defined as the MSB and the last bit (bit 8) as the LSB. The T8502 provides only one half bit of data for the LSB in order to eliminate bus contention between adjacent time slots. Bit 1 is the sign bit, bits 2 through 4 are the chord bits, and bits 5 through 8 are the steps in the chord.

D_X remains in a high-impedance state when not transmitting data. This allows the codec to operate with a single transmit port and also allows use with other codecs on a shared PCM bus. Since D_X and D_R are CMOS nodes, these buses can be tied to a known state through a pull-up resistor (approximately 100 kΩ), if desired. Data is transmitted from the codec through D_X and received to the codec through D_R. D_R remains inactive until data is to be received. For analog loopback, D_X and D_R can be shorted together. If using this feature, transmit and receive data must be aligned. Data alignment and time-slot assignment are discussed next.

Frame Synchronization

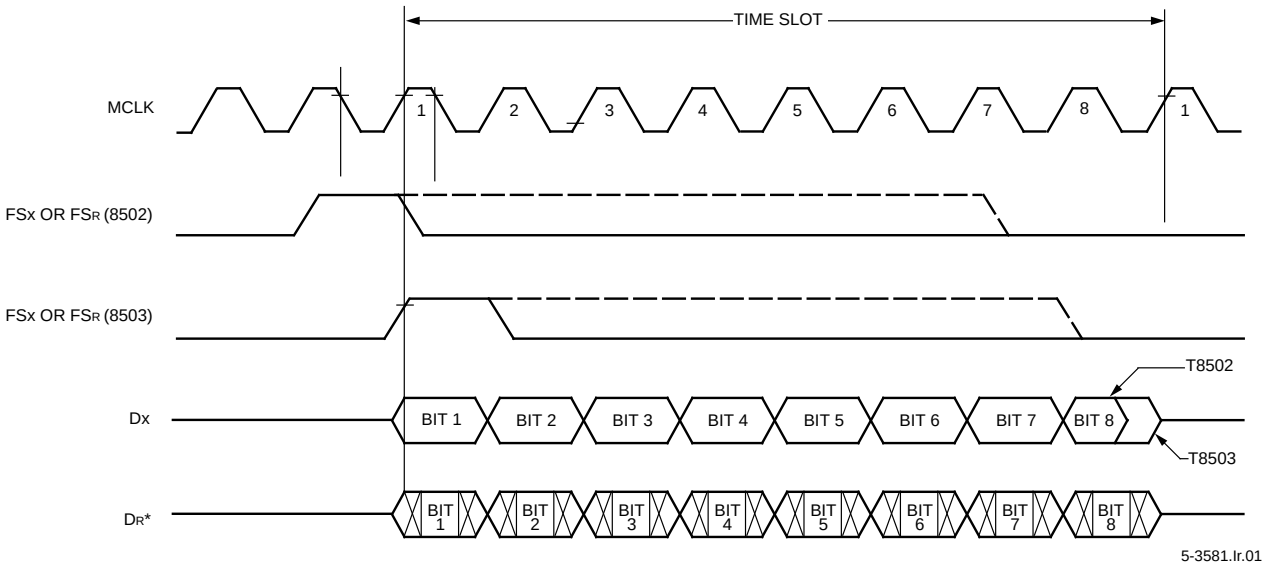
Each device has four frame sync (FS_X and FS_R) inputs, one pair for each channel. During a single 125 µs frame, each frame sync input is supplied a single pulse. Frame syncs can be applied anytime after the initial powerup of the device and after MCLK is applied. The timing of the respective frame sync pulse indicates the beginning of the time slot during which data for that channel is clocked in or out of the device. FS_X and FS_R must be high for a minimum of one master clock cycle. They can be operated independently, or they can be tied together on a given channel for coincident transmit and receive data transfer. During a frame, channel 0 and 1 transmit frame sync pulses must be separated from each other by one or more time slots. Likewise, channel 0 and 1 receive frame sync pulses must be separated from each other by one or more time slots, unless both channels are to receive the same PCM signal. In that case, the receive frame sync pulses can be tied together. In practice, both FS_X and FS_R should be provided to ensure proper data transfer operation. For transmitting data only, however, providing FS_X alone will suffice. For receiving data only, both FS_X and FS_R strobes are required.

With the T8502, FS is latched by a negative-going MCLK edge. With regard to FS, the byte boundary occurs on the first positive-going MCLK edge after FS is detected. FS must occur at one of the byte boundaries; that is, at time slot 0 or multiples of eight clock cycles thereafter (time slot 1, 2, 3, etc.). Data is valid one MCLK cycle after FS is detected. This is referred to as delayed timing mode. The MSB of data is latched on the first negative-going MCLK edge following the negative-going edge that latches FS.

With the T8503, the byte boundary occurs coincident with the rising edge of FS. Data is valid coincident with FS. This is referred to as nondelayed timing mode. The MSB of data is latched on the same negative-going MCLK edge that latches FS_X. Note, in this mode, the width of data bit 1 will be dependent upon when FS_X goes high. If the rising edge of FS_X lags the rising edge of MCLK, bit 1 will have a shorter width than the other data bits. This could cause data corruption if hold times are violated.

FS_X and FS_R for a given channel can occur only one time per frame. The falling edge of FS has no relevance; therefore, the width of FS is not critical. The digital interface will operate satisfactorily as long as FS goes to low at least one clock cycle prior to it going high again.

Digital Interface (continued)



* DR Xed areas refer to DON'T CARE states.

Figure 2. Digital Interface Timing

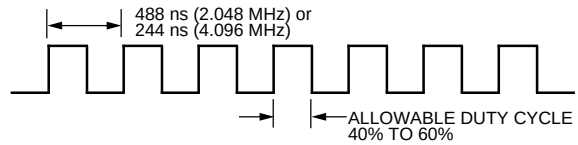
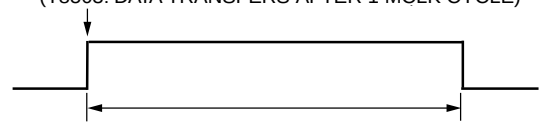
MCLK	MASTER CLOCK REQUIRED FOR OVERALL OPERATION. WITH ONLY MCLK APPLIED, CODEC WILL ASSUME STANDBY MODE.	
FSX0, FSR0, FSX1, FSR1	FRAME SYNC ASSIGNS TIME SLOT. REQUIRED FOR PER-CHANNEL OPERATION. WITH MCLK AND ALL FSs APPLIED, CODEC ASSUMES POWERUP MODE. ABSENCE FOR FOUR FRAMES PLACES CODEC IN STANDBY OR PARTIAL STANDBY MODE.	INITIATES DATA TRANSFER (T8502: DATA TRANSFERS IMMEDIATELY) (T8503: DATA TRANSFERS AFTER 1 MCLK CYCLE)  ALLOWABLE WIDTH: MCLK = 2.048 MHz 488 ns TO 124.5 µs (1 MCLK TO 255 MCLKs) MCLK = 4.096 MHz 244 ns TO 124.75 µs (1 MCLK TO 255 MCLKs)

Figure 3. User-Supplied Timing Pulses—Definition and Relevance

Digital Interface (continued)

Internal Timing and Control

Master Clock

The T8502 and T8503 are configured to operate at MCLK rates of 2.048 MHz or 4.096 MHz. Internal circuitry determines the master-clock frequency during a built-in powerup reset interval. MCLK can be applied anytime after the initial powerup of the device. The MCLK is used by various internal circuits including the filters. For instance, operating at higher than specified MCLK rates will affect the device's filter characteristics by shifting the filter poles to higher frequencies. Lower than specified MCLK rates should not be used because there will be an inadequate number of pulses to perform normal codec operations. MCLK duty cycle should be maintained between 40% to 60%.

A-Law/μ-Law Select

The ASEL pin provides pin-strap programmability of the companding operation. Logic low selects μ-law coding, and logic high selects alternate bit inversion A-law coding. Companding selection can be changed in real time. ASEL is monitored every 125 μs, so a change in logic level will change the companding state on the next frame sync pulse. A pull-down device is included within the codec, thereby defaulting the part to μ-law companding.

Powerdown Control

The dual codec exhibits three power dissipation modes: powerup, partial standby, and standby. Operation in the standby modes reduces power consumption and heat dissipation when device operation is not required. The device is at full powerup when MCLK and both FSx pulses are present. Under full powerup, the codec typically dissipates 80 mW (maximum 105 mW). Absence of an FSx pulse institutes a powerdown of that given channel. When FSx is absent for four frames (500 μs), the channel it is associated with will go into standby mode. With one channel powered down (partial standby), power dissipation is reduced by 30 mW (maximum 37 mW) from the full powerup mode. If both FSx pulses are absent, the codec will go into standby mode and the entire part will typically dissipate 15 mW (maximum 42 mW).

Standby mode is not guaranteed if MCLK is lost. Standby is achieved by removing the FSx pulse for at least 500 μs with MCLK active, after which MCLK can be removed.

Standby mode keeps the internal reference voltages active. This ensures a fast, quiet powerup when FSx is reapplied.

Analog Interface

See Figure 1 for a functional block diagram of this codec.

Bias Circuit and Reference

The codec requires only a 5 V supply to operate. This eliminates the necessity of a –5 V supply and bypass capacitor for codec use. It also changes the signal reference from 0 V, like codecs with –5 V supplies use, to 2.4 V. This 2.4 V is internally generated by a precision band-gap voltage reference. This voltage reference requires no additional external components. A single band-gap voltage reference is used throughout the codec circuitry in order to provide very accurate gains and a wide dynamic range. This voltage reference is heavily buffered using unity gain op amps. The reference is used as the input to the noninverting node of the transmit uncommitted op amp and the reference output of the receive op amp. Each channel is provided with its own individually buffered transmit and receive voltage references in order to minimize interchannel and intrachannel crosstalk.

Transmit Operation (A-D)

The transmit path consists of an input op amp, bandpass filtering, and an encoder.

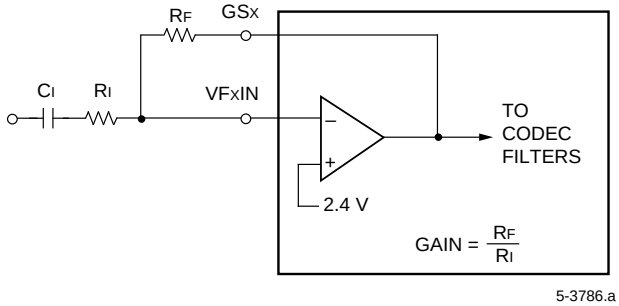


Figure 4. Typical Analog Input Section

Analog Interface (continued)

The dual codec supplies one uncommitted op amp per channel. A schematic of an input circuit is shown in Figure 4. Inverting input (VFxIN) and output leads (GSx) are user accessible. The band-gap voltage reference is applied to the noninverting input.

Passband gain is set by simply dividing the op amp's feedback resistor (R_F) by the op amp's input resistor (R_I). For best transmission performance, gain values should range from 0 dB to 20 dB (gain between 1 to 10).

Feedback resistance values should range from 10 kΩ to 200 kΩ, and capacitance from GSx to ground should be kept less than 50 pF. A low-value picofarad capacitor can be used across the feedback resistor to increase stability or to reduce the gain of injected high-frequency noise. Maintaining these values will minimize crosstalk while still providing acceptable loading on GSx. An encoder milliwatt is defined as 0.775 Vrms on this part. This convenient value (1 mW into 600 Ω is 0.775 Vrms) referenced to 2.4 V still allows acceptable headroom for the maximum signal transmission, which is 3 dBm0 (3.145 Vp-p max, A-law; 3.169 Vp-p max, μ-law). The minimum transmission signal level is determined by the signal-to-noise ratio. The codecs are measured at –50 dBm0 signal levels in production test and pass ITU-T quantization distortion plus noise specifications.

If phase inversion of the analog signal is required for transhybrid balance considerations, then an external op amp must be employed. Many Lucent SLICs include a spare op amp that can be used to supply the necessary phase inversion.

VFxIN must be capacitively coupled to its signal source since the codec analog inputs are referenced to internal 2.4 V. Filtering within the codec forms the frequency spectrum shaping, but the input capacitor selection can impact on the low-frequency pole. Additional low-frequency loss contributed by the input network can be calculated using the following equation:

$$\text{loss} = 20 \log_{10} \frac{2\pi f_{in} R_I C_I}{\sqrt{1 + (2\pi f_{in} R_I C_I)^2}}$$

Where f_{in} is the low-frequency of interest (e.g., 300 Hz), and R_I and C_I are the input resistor and input capacitor, respectively (see Figure 4). For an input resistor of 50 kΩ and an input capacitor of 0.1 μF, the additional loss provided by the input network at 300 Hz would be –0.05 dB.

For SLIC use, the ac impedance of the transmit and receive coupling capacitors becomes a factor in the effective transhybrid balance. Coupling capacitor values should be selected according to component selection criteria defined by the SLIC.

The output of the op amp feeds the bandpass filter network. Transmit filtering consists of an antialiasing filter followed by a fifth-order elliptic low-pass filter and a third-order high-pass filter. The filters are all switched capacitor filters. The antialiasing filter prevents high frequencies from folding over and distorting the encoding process. The high-pass filter effectively attenuates low-frequency noise like ac and ringing signals, yet typically provides only –0.5 dB of attenuation at 200 Hz (see Transmit Filter Characteristics in the data sheet). The passband frequencies adhere to ITU-T G.712 requirements. Passband frequencies are then encoded via quantization. The analog signal is sampled and converted to a digital PCM representation using charge redistribution with successive approximation. Companding is user selectable as either A-law or μ-law. The encoded signal is now presented to the PCM interface block.

If one transmit channel is not to be used, tie GSx to VFxIN and omit R_I and C_I.

Receive Operation (D-A)

The decoder converts the digital PCM stream to an analog signal using charge redistribution and sample and hold capacitors. The reconstructed analog signal passes through a fifth-order elliptic low-pass filter compliant with ITU-T G.712 and Lucent PUB43801 D3/D4 requirements. The filtered analog signal is now provided to the output amplifier.

The output amplifier provides a single-ended output, capable of driving a load of 2000 Ω or greater and a capacitance of up to 100 pF. The output signal is referenced to its channel's analog ground. Like the analog input, common-mode reference is a dc 2.4 V. Receive gain of the codec is selectable. With the gain selection pin (GS0 or GS1) tied high or left floating, the receive path gain is set at 0 dB. When the pin is tied low, the receive path gain is attenuated by 3.5 dB. Receive gain can be further attenuated external to the output op amp by simply employing a resistive voltage divider.

A decoder milliwatt with a PCM input of 0 dBm0 is 0.775 Vrms. Maximum signal level output is 3 dBm0 (3.145 Vp-p max, A-law; 3.169 Vp-p max, μ-law).

For determining a proper value of capacitive coupling, follow the same procedure as with the transmit coupling capacitor using the input resistance of the SLIC as R_I.

To minimize power dissipation, let an unused receive output float.

Board Layout and Decoupling

Concentrating four analog-to-digital conversions in a board area of 0.18 in.^{2} places extra burden on the board layout. The integration of two codecs into a 20-pin package places highly sensitive analog nodes and noisy digital circuits in close proximity. The high dynamic range of the codec, which allows low noise transmission of very small signal levels with minimal crosstalk, could be jeopardized if proper grounding and decoupling techniques are not observed and parasitic coupling is not minimized.

A common layout methodology for line card design is to use the codec's analog ground pins for the reference point for all analog circuitry. The codec has two analog ground pins (GNDA). These should all be tied together at the device. Analog grounds from other circuitry, like SLICs, should also be tied to this common reference point.

The codec also has one digital ground pin (GNDD). There are two methods on how to deal with digital ground. Both of these would be classified as parallel or star single-point ground connection schemes. The preferred method is to tie GNDD and GNDA together as part of one large, low-impedance ground plane. This is commonly used in multilayer boards where a separate ground layer can be used. Another method is to route a separate digital ground to GNDD. This method is common on two-layer boards where PWB real estate is limited.

The codec has one V_{DD} pin. V_{DD} serves both analog and digital circuits. It is important to place a 0.1 µF ceramic capacitor on this pin to GNDD.

V_{DD} is the demarcation point for analog and digital circuitry. Digital circuits are grouped together in one area of the package. Runners for analog and digital circuitry should diverge from this point. Not following this practice could result in harmonic frequencies from carrier modulation or digital transitions coupling into VFxIN and the passband frequencies.

Special consideration is required with regard to layout of analog input leads to output leads. Interchannel and intrachannel crosstalk into VFxIN can be significantly affected by parasitic capacitance feeds from GSx and VF_RO. PWB layouts should be arranged to keep these parasitics low. The T8502/8503 Evaluation Board can be used as a guide for correct layout technique. The evaluation board achieves interchannel crosstalk values of < –80 dB.

For general board layout, other general rules of digitally controlled, audio frequency circuits apply. Digital circuitry should be placed as close to the edge connector as possible. Clock leads should be kept as short as possible. And a large bulk storage capacitor of about 47 µF, in parallel with the 0.1 µF ceramics, should be placed at distribution points located near the connector.

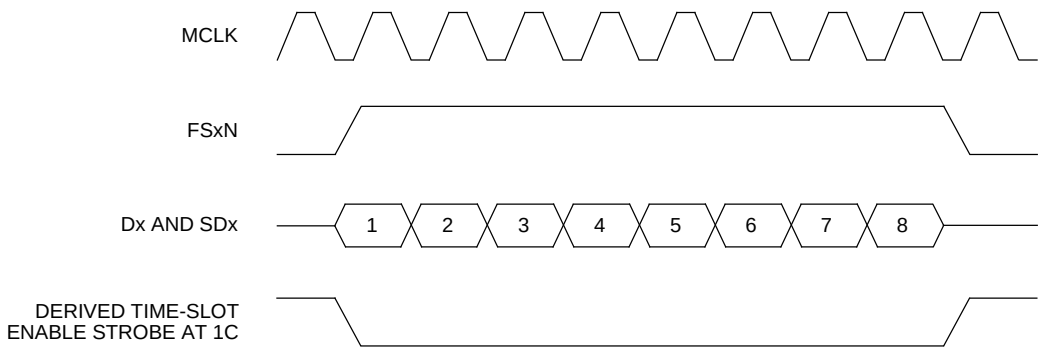
Applications

Time-Slot Enable Strobe

Some codecs provide a time-slot enable strobe. This strobe is useful in enabling external 3-state buffers that could be required to drive heavily loaded bus lines. This strobe provides an active-low pulse that envelops an 8-bit transmit PCM time slot. The dual codec does not provide a time-slot enable output. A time-slot enable pulse can be derived, however, from the T8503 FS_X pulse. The T8503 operates in nondelayed timing mode. The rising edge of frame sync envelops the first bit of the time slot. Frame sync pulses can be set anywhere from one clock pulse wide to 255 or 511 clock pulses wide (2.048 MHz and 4.096 MHz operation, respectively). To generate a time-slot enable pulse, the frame sync pulse should be set eight clock pulses wide. Inverting the frame sync pulse generates an 8-bit wide active-low pulse that can be used for time-slot enable (see Figure 5).

To create a time-slot enable for the T8502, insert a D-type flip-flop clocked by MCLK at node 1C in Figure 5.

Applications (continued)



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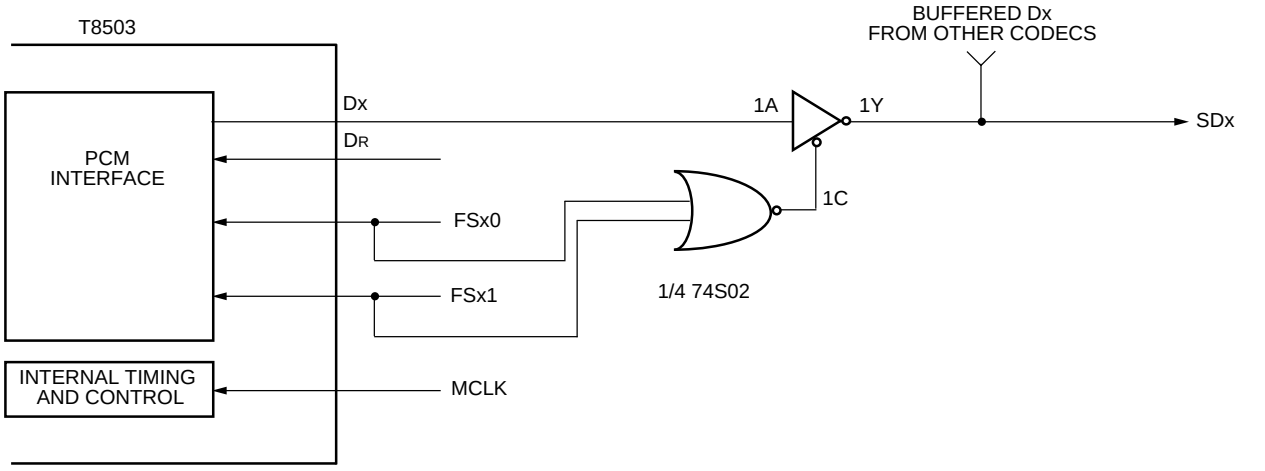

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Figure 5. Time-Slot Enable Strobe Timing Diagram and Circuit

Applications (continued)

SLIC Interface

Interfacing a codec to a SLIC is discussed in detail in application materials relating to the SLIC. Lucent provides application material and software to assist in the design of this interface. A basic interface circuit for 600 Ω resistive termination is shown in Figure 6. RG sets the transmit gain for the SLIC. RT2 and RX set the transmit gain of the codec. The value of RHB1 needs to be appropriately selected according to loop gains to set the hybrid balance. RRCV and RGP (with RT1 in parallel) provide attenuation of the codec receive signal. Receive gain of the codec is set at 0 dB. RT1 (with RRCV and RGP in parallel) sets up the termination impedance. CB1 and CB2 provide dc blocking of the codec reference level and ac signal coupling. Their ac impedance also needs to be considered in hybrid balance calculations.

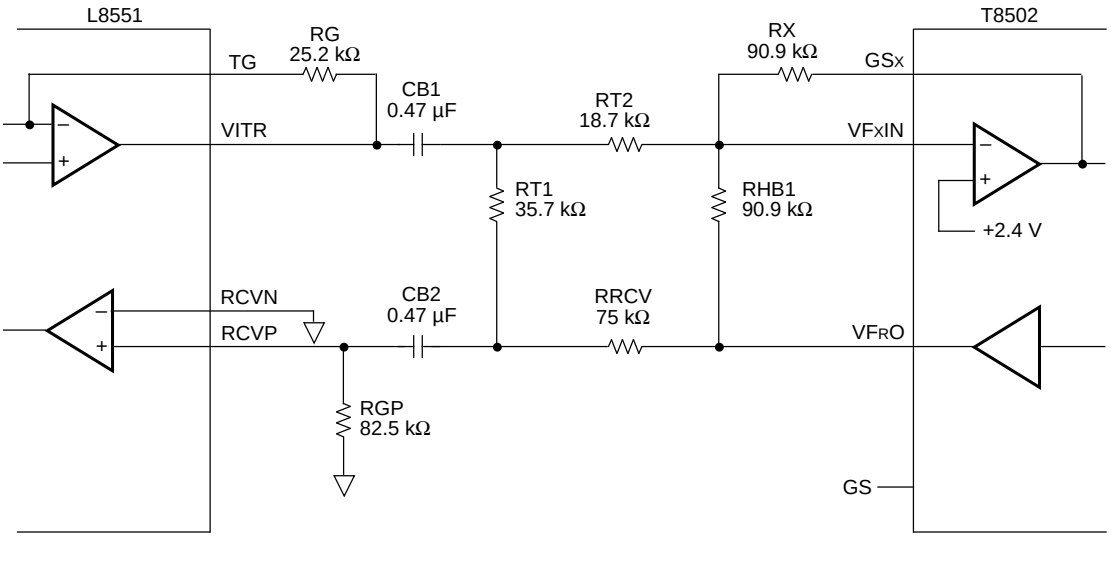

Figure 6. SLIC Interface (600 Ω Resistive)

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