- **Dot and N-Line Inversion Available**
- **Six-Bit (64 Gray-Scale) Digital Driver**
- **Mini-LVDS Level Input (Five Pairs of Serial Data Inputs)**
- **480 Output Ports (for UXGA Format)**
- **V_{DD} for Logic Port: 2.7 V to 3.6 V**
- **V_{DD} for LCD Driving Port: 8 V to 13.5 V**

description

TMS57535A is a six bit (64 gray-scale) source driver for TFT liquid-crystal display (LCD) with 480 output ports to deal with UXGA format.

Reduction in the number of input ports and electromagnetic interference (EMI) is expected with the introduction of mini-LVDS (low voltage differential signaling) interface at the input ports.

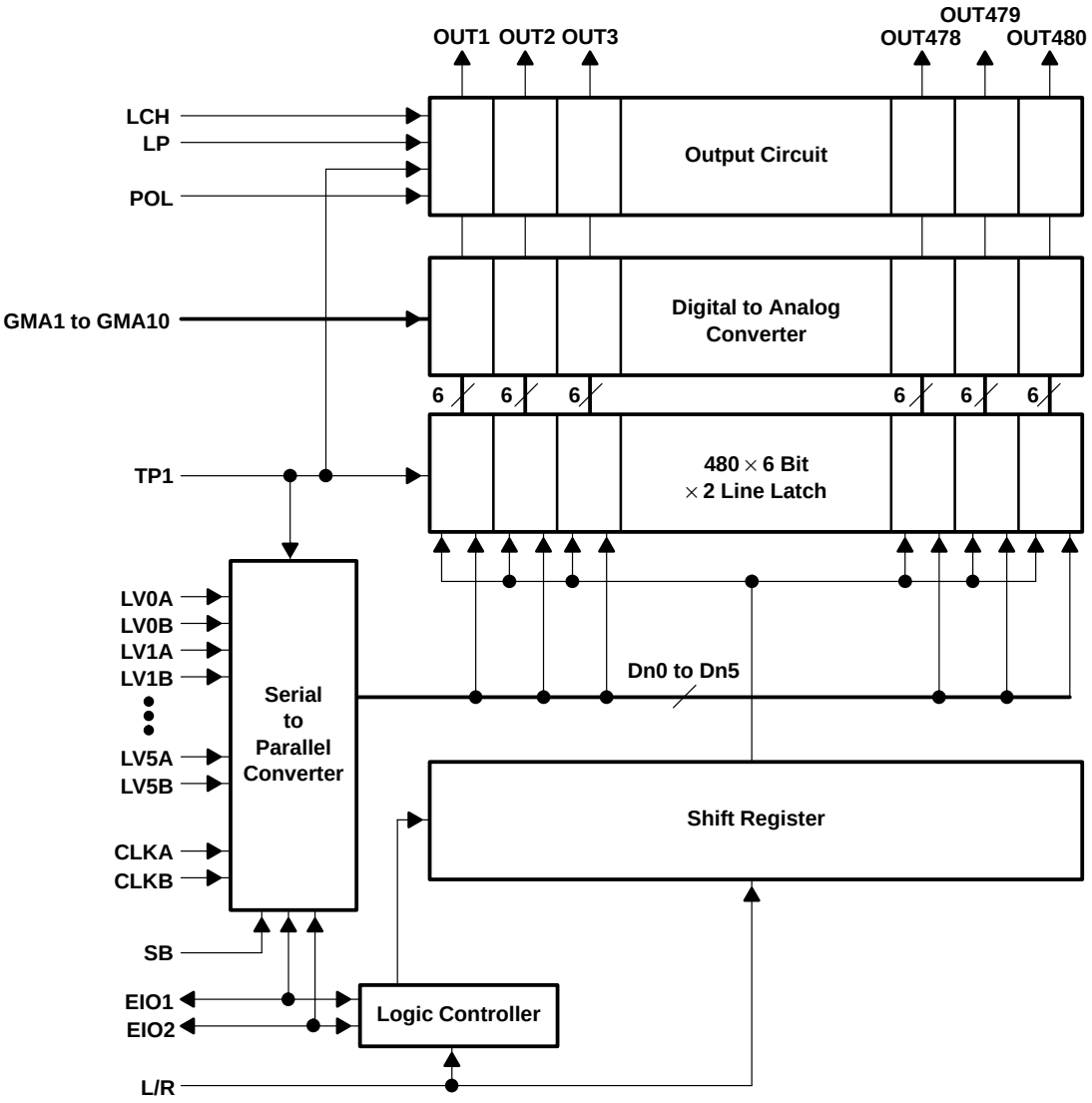
PACKAGE INFORMATION

The TCP's external shape is customized. To order the required shape, contact a TI sales representative.

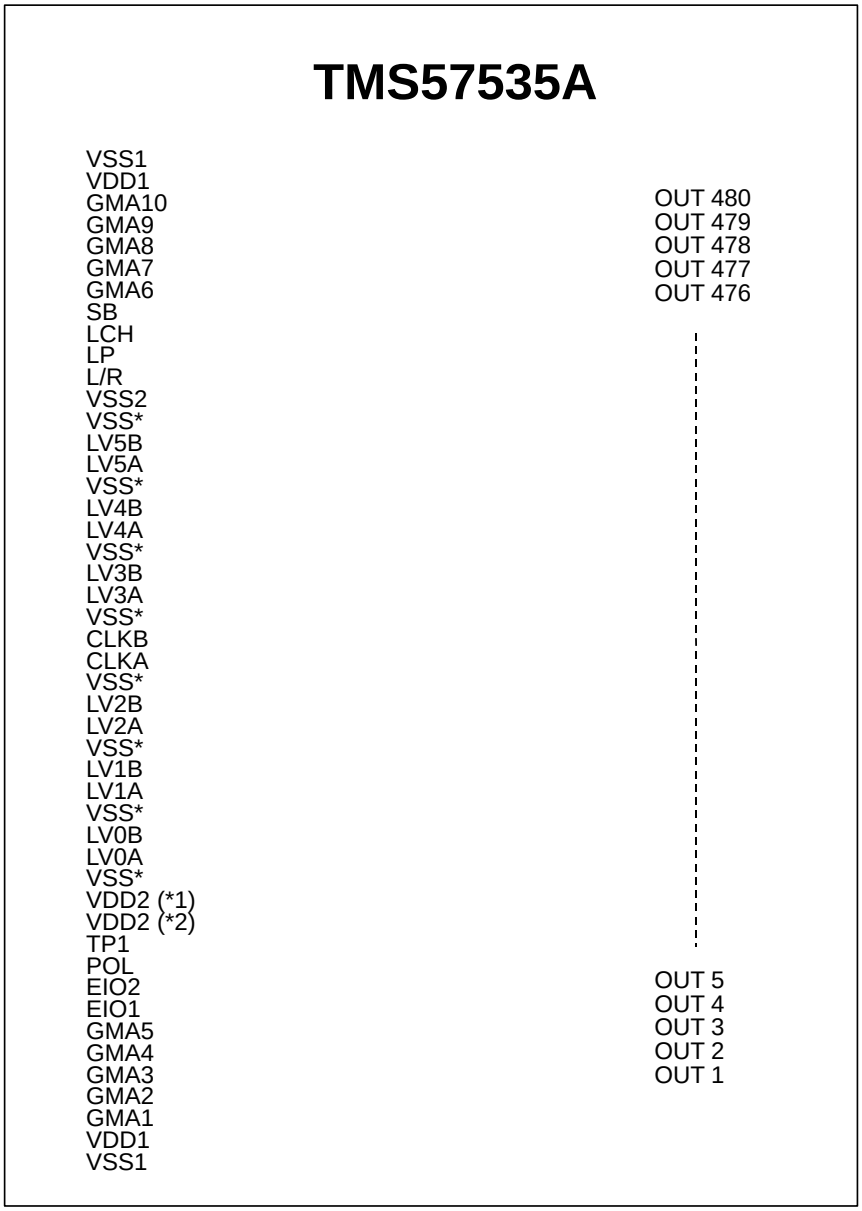
PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



TCP pin assignments



NOTE: Pattern side up and no dimension specification for the TCP

PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
CLKA, CLKB	I	Clock (mini-LVDS). Shift clock (refer to Table 1)
LV0A, B–LV5A, B	I	Display data (mini-LVDS). Displays data with gray-scale data (6-bit) and control signal (RST=reset) (refer to Table 1)
L/R	I	Shift direction. Controls the direction of loaded data at the shift register (refer to Table 2)
EIO1, EIO2	I/O	Start pulse. Input/Output definition of address shift register (refer to Table 2)
TP1	I	Input mode and output timing control. Changes the input mode, latches the registered data, and transfers to the DAC at the rising edge. Voltage to LCD pixel is output at falling edge.
POL	I	Polarity control. Controls the polarity of the output. Defined by the POL signal at TP1 as H (refer to Table 3)
LCH	I	Drivability control. LCH = H: Higher drivability for heavy load LCH = L; Normal drivability
LP	I	Low power mode selection. Decreases the charge/discharge current to output load. LP=H: low power mode. Refer to the application notes.
SB	I	Bus-line set-back. Changes the data order of mini-LVDS input (see Table 1)
OUT1–OUT480	O	Output. Supplies voltage to each LCD pixel.
VDD1, VSS1	I	Power supply (output circuits). Power supply for output (driving) circuits
VDD2(*1) VDD2(*2) VSS2 VSS*	I	Power supply (control=logic circuits). VDD2(*1) is for mini-LVDS receiver and VDD2(*2) is for other logic circuits. Supplies stable voltage to VDD2(*1). VDD2(*1) and VDD2(*2) must be at the same electric potential. Possible to wire the V_{SS} potential between each mini-LVDS signal line from VSS* terminal, though no wiring, no relation to function itself.
GMA1–GMA10	I	γ-corrected power supplies. Receives the external γ-corrected power supplies by using operational amplifiers. Maintain the recommended operating conditions.

Table 1. Function Table (Bus-Line Set-Back)

PIN NAME	SB=L	SB=H
LV0A	DUMMY	LV4–
LV0B	DUMMY	LV4+
LV1A	LV0+	LV3–
LV1B	LV0–	LV3+
LV2A	LV1+	LV2–
LV2B	LV1–	LV2+
CLKA	CLK+	CLK–
CLKB	CLK–	CLK+
LV3A	LV2+	LV1–
LV3B	LV2–	LV1+
LV4A	LV3+	LV0–
LV4B	LV3–	LV0+
LV5A	LV4+	DUMMY
LV5B	LV4–	DUMMY

Suffix + indicates positive potential and – indicates negative potential at each differential signal input pair.

Table 2. Function Table (L/R and EIOn)

L/R	EIO1	EIO2	Shift Direction
H	Right shift: in	Right shift: out	OUT1 → OUT480
L	Left shift: out	Left shift: in	OUT480 → OUT1

Table 3. Function Table (POL and Reference GAMMA)

POL	ODD-NUMBERED OUTPUT	EVEN-NUMBERED OUTPUT
H	GMA6 to GMA10	GMA1 to GMA5
L	GMA1 to GMA5	GMA6 to GMA10

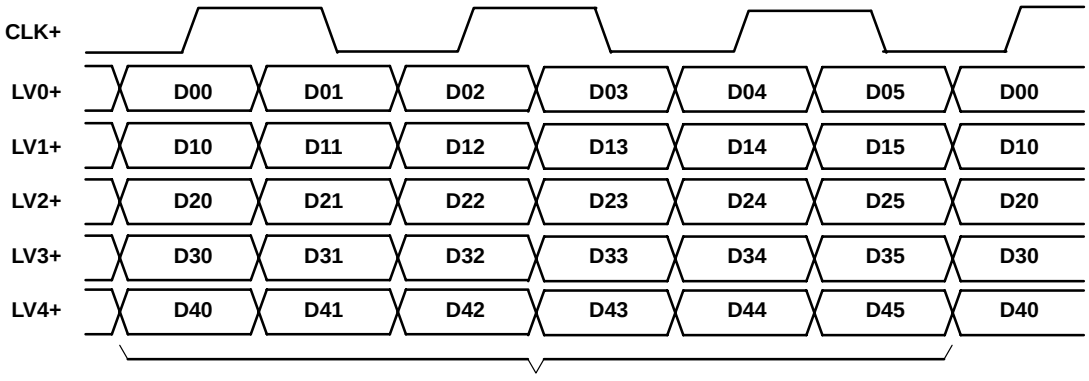
detailed description

data mapping

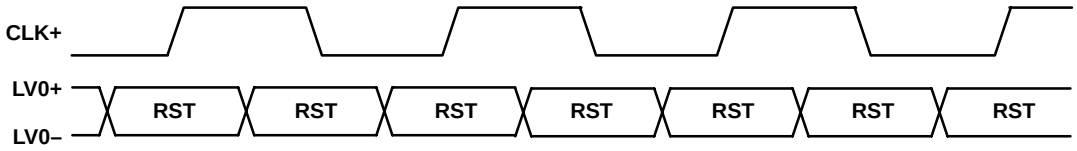
Display and control data (RST) are input to LV0+,– to LV4+,–.

Data mapping is changed in response to the mode; the mode is changed by TP1.

<Data Input Mode>



< Control Signal Input Mode >



There is no assignment from LV1+,– to LV4+,–. Therefore, they are don't care.

Output timing and polarity are controlled by TP1 and POL signals. Refer to the Terminal Function table and Table 3.

composition of display data

MSB					LSB	
Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	N = 0 to 4

relation between display data and output number

OUTPUT	OUT1	OUT2	OUT3		OUT478	OUT479	OUT480
Display data	D00 to D05	D10 to D15	D20 to D25	– – – – – – –	D20 to D25	D30 to D35	D40 to D45

This relationship is irrespective of L/R condition.

PRODUCT PREVIEW

detailed description (continued)

cascade

Multiple chips can be used in a cascade connection.

- Input EIO pad at lead (head) chip is fixed to H.
- Input EIO after secondary chips are connected to output EIO of lead chip.

Receiving the display data

- The lead (head) chip is set to *control signal input mode* (also called *control mode*), and the receivers at LV0+,– and CLK+,– on all chips are activated by the rising edge of TP1.
- Input the reset (RST) signal to LV0+,– as L. This RST must be maintained over 200 ns after rising of TP1.
- Input RST as H to LV0+,–. The duration of H must be over 50 ns and at least three CLK cycles.
- Input the RST as L to LV0+,–; then change to the *data input mode* function. Input TP1 again when a second RST is necessary.
- Data sampling starts at the rising edge of CLK after reading of RST=L.
- The internal counter starts counting the data cycle for EIO signal generation at the same time data sampling starts.
- When data sampling is finished, the receivers turn off.
- After the receivers turn off, keep the timing for at least five more CLK cycles until TP1 is applied.
- Figure 1 shows the rough timing chart from application of TP1 to the start of data sampling.

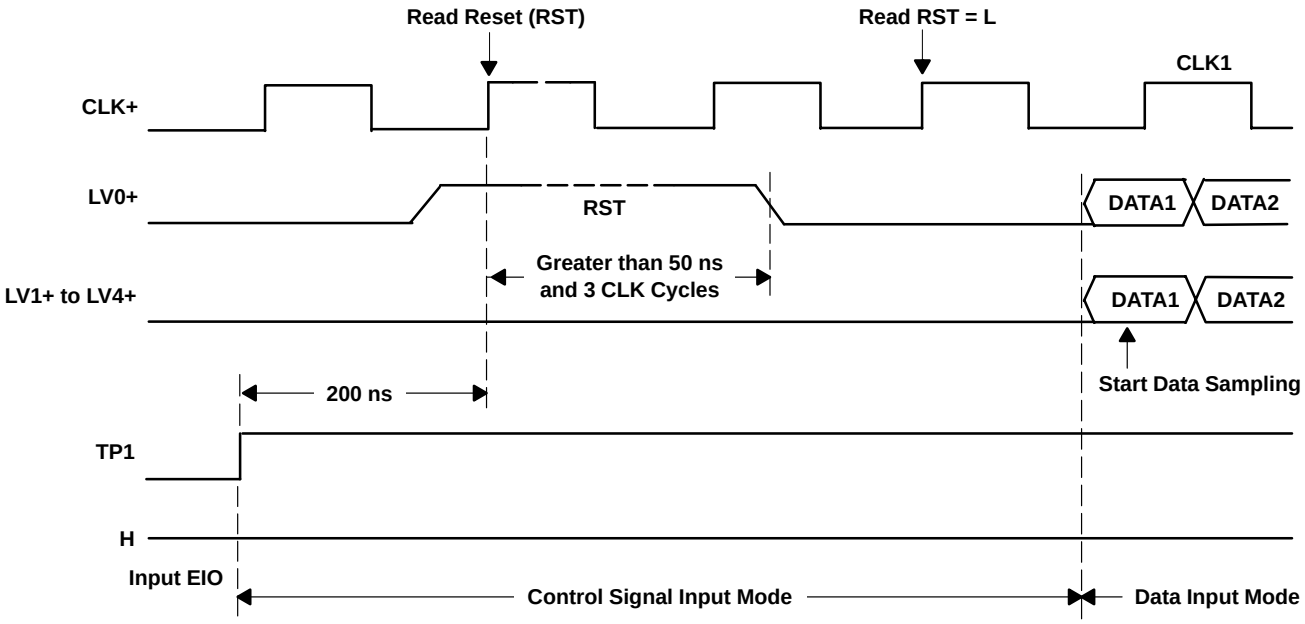


Figure 1. Timing From Start to Sampling (Reference)

detailed description (continued)

relation between input data and output voltage

The digital-to-analog converter (D/A) consists of resistors connected in a ladder configuration. Figure 2 shows an outline of the relation between input data and γ-corrected voltages.

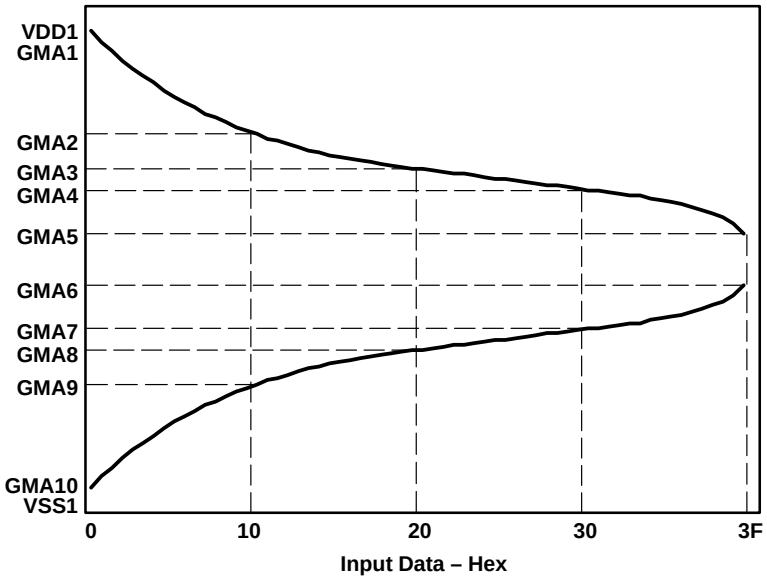


Figure 2. γ-Corrected Power Supplies

ladder resistors

Resistors are connected to each terminal of the power supplies for γ-corrected supplies, and the resistance ratio is given in Table 4.

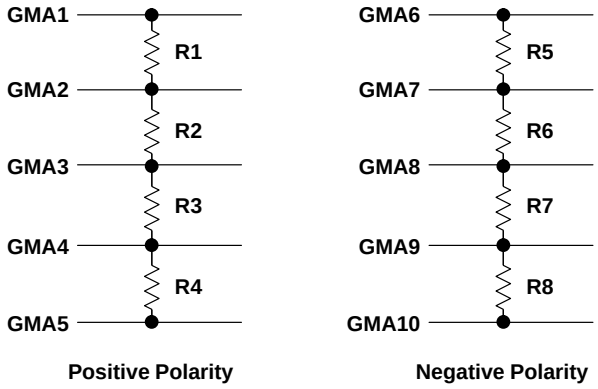


Figure 3. Ladder Resistors Connection

Table 4. Resistor Ratio

RESISTOR	RATIO
R1, R8	161
R2, R7	55
R3, R6	32
R4, R5	69

PRODUCT PREVIEW

detailed description (continued)

relation between input data and output voltage

Table 5. Positive Polarity

DATA (HEX)	OUTPUT VOLTAGE	DATA (HEX)	OUTPUT VOLTAGE
00	GMA1	20	GMA3
01	GMA2+(GMA1–GMA2)X 145/161	21	GMA4+(GMA3–GMA4)X 30/32
02	GMA2+(GMA1–GMA2)X 130/161	22	GMA4+(GMA3–GMA4)X 28/32
03	GMA2+(GMA1–GMA2)X 116/161	23	GMA4+(GMA3–GMA4)X 26/32
04	GMA2+(GMA1–GMA2)X 103/161	24	GMA4+(GMA3–GMA4)X 24/32
05	GMA2+(GMA1–GMA2)X 91/161	25	GMA4+(GMA3–GMA4)X 22/32
06	GMA2+(GMA1–GMA2)X 80/161	26	GMA4+(GMA3–GMA4)X 20/32
07	GMA2+(GMA1–GMA2)X 69/161	27	GMA4+(GMA3–GMA4)X 18/32
08	GMA2+(GMA1–GMA2)X 59/161	28	GMA4+(GMA3–GMA4)X 16/32
09	GMA2+(GMA1–GMA2)X 49/161	29	GMA4+(GMA3–GMA4)X 14/32
0A	GMA2+(GMA1–GMA2)X 41/161	2A	GMA4+(GMA3–GMA4)X 12/32
0B	GMA2+(GMA1–GMA2)X 33/161	2B	GMA4+(GMA3–GMA4)X 10/32
0C	GMA2+(GMA1–GMA2)X 26/161	2C	GMA4+(GMA3–GMA4)X 8/32
0D	GMA2+(GMA1–GMA2)X 19/161	2D	GMA4+(GMA3–GMA4)X 6/32
0E	GMA2+(GMA1–GMA2)X 12/161	2E	GMA4+(GMA3–GMA4)X 4/32
0F	GMA2+(GMA1–GMA2)X 6/161	2F	GMA4+(GMA3–GMA4)X 2/32
10	GMA2	30	GMA4
11	GMA3+(GMA2–GMA3)X 49/55	31	GMA5+(GMA4–GMA5)X 67/69
12	GMA3+(GMA2–GMA3)X 44/55	32	GMA5+(GMA4–GMA5)X 65/69
13	GMA3+(GMA2–GMA3)X 39/55	33	GMA5+(GMA4–GMA5)X 63/69
14	GMA3+(GMA2–GMA3)X 34/55	34	GMA5+(GMA4–GMA5)X 61/69
15	GMA3+(GMA2–GMA3)X 30/55	35	GMA5+(GMA4–GMA5)X 59/69
16	GMA3+(GMA2–GMA3)X 26/55	36	GMA5+(GMA4–GMA5)X 56/69
17	GMA3+(GMA2–GMA3)X 22/55	37	GMA5+(GMA4–GMA5)X 53/69
18	GMA3+(GMA2–GMA3)X 19/55	38	GMA5+(GMA4–GMA5)X 50/69
19	GMA3+(GMA2–GMA3)X 16/55	39	GMA5+(GMA4–GMA5)X 46/69
1A	GMA3+(GMA2–GMA3)X 13/55	3A	GMA5+(GMA4–GMA5)X 42/69
1B	GMA3+(GMA2–GMA3)X 10/55	3B	GMA5+(GMA4–GMA5)X 37/69
1C	GMA3+(GMA2–GMA3)X 8/55	3C	GMA5+(GMA4–GMA5)X 32/69
1D	GMA3+(GMA2–GMA3)X 6/55	3D	GMA5+(GMA4–GMA5)X 26/69
1E	GMA3+(GMA2–GMA3)X 4/55	3E	GMA5+(GMA4–GMA5)X 16/69
1F	GMA3+(GMA2–GMA3)X 2/55	3F	GMA5

NOTE: GMA5 and GMA6 are not connected in the chip.

relation between input data and output voltage (continued)

Table 6. Negative Polarity

DATA (HEX)	OUTPUT VOLTAGE	DATA (HEX)	OUTPUT VOLTAGE
00	GMA10	20	GMA8
01	GMA10+(GMA9–GMA10)X 16/161	21	GMA8+(GMA7–GMA8)X 2/32
02	GMA10+(GMA9–GMA10)X 31/161	22	GMA8+(GMA7–GMA8)X 4/32
03	GMA10+(GMA9–GMA10)X 45/161	23	GMA8+(GMA7–GMA8)X 6/32
04	GMA10+(GMA9–GMA10)X 58/161	24	GMA8+(GMA7–GMA8)X 8/32
05	GMA10+(GMA9–GMA10)X 70/161	25	GMA8+(GMA7–GMA8)X 10/32
06	GMA10+(GMA9–GMA10)X 81/161	26	GMA8+(GMA7–GMA8)X 12/32
07	GMA10+(GMA9–GMA10)X 92/161	27	GMA8+(GMA7–GMA8)X 14/32
08	GMA10+(GMA9–GMA10)X 102/161	28	GMA8+(GMA7–GMA8)X 16/32
09	GMA10+(GMA9–GMA10)X 112/161	29	GMA8+(GMA7–GMA8)X 18/32
0A	GMA10+(GMA9–GMA10)X 120/161	2A	GMA8+(GMA7–GMA8)X 20/32
OB	GMA10+(GMA9–GMA10)X 128/161	2B	GMA8+(GMA7–GMA8)X 22/32
OC	GMA10+(GMA9–GMA10)X 135/161	2C	GMA8+(GMA7–GMA8)X 24/32
OD	GMA10+(GMA9–GMA10)X 142/161	2D	GMA8+(GMA7–GMA8)X 26/32
OE	GMA10+(GMA9–GMA10)X 149/161	2E	GMA8+(GMA7–GMA8)X 28/32
OF	GMA10+(GMA9–GMA10)X 155/161	2F	GMA8+(GMA7–GMA8)X 30/32
10	GMA9	30	GMA7
11	GMA9+(GMA8–GMA9)X 6/55	31	GMA7+(GMA6–GMA7)X 2/69
12	GMA9+(GMA8–GMA9)X 11/55	32	GMA7+(GMA6–GMA7)X 4/69
13	GMA9+(GMA8–GMA9)X 16/55	33	GMA7+(GMA6–GMA7)X 6/69
14	GMA9+(GMA8–GMA9)X 21/55	34	GMA7+(GMA6–GMA7)X 8/69
15	GMA9+(GMA8–GMA9)X 25/55	35	GMA7+(GMA6–GMA7)X 10/69
16	GMA9+(GMA8–GMA9)X 29/55	36	GMA7+(GMA6–GMA7)X 13/69
17	GMA9+(GMA8–GMA9)X 33/55	37	GMA7+(GMA6–GMA7)X 16/69
18	GMA9+(GMA8–GMA9)X 36/55	38	GMA7+(GMA6–GMA7)X 19/69
19	GMA9+(GMA8–GMA9)X 39/55	39	GMA7+(GMA6–GMA7)X 23/69
1A	GMA9+(GMA8–GMA9)X 42/55	3A	GMA7+(GMA6–GMA7)X 27/69
1B	GMA9+(GMA8–GMA9)X 45/55	3B	GMA7+(GMA6–GMA7)X 32/69
1C	GMA9+(GMA8–GMA9)X 47/55	3C	GMA7+(GMA6–GMA7)X 37/69
1D	GMA9+(GMA8–GMA9)X 49/55	3D	GMA7+(GMA6–GMA7)X 43/69
1E	GMA9+(GMA8–GMA9)X 51/55	3E	GMA7+(GMA6–GMA7)X 53/69
1F	GMA9+(GMA8–GMA9)X 53/55	3F	GMA6

NOTE: GMA5 and GMA6 are not connected in the chip.

electrical/timing specifications

Basically, the ground-level voltage is $V_{SS1} = V_{SS2} = 0$ V.

Electrical and timing characteristics are assured under the recommended operating conditions.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage at logic port, V_{DD2} . . . . . –0.5 V to 5 V
Supply voltage at driver port, V_{DD1} . . . . . –0.5 V to 14.0 V
Input voltage: GMA1 to GMA10 . . . . . –0.5 V to V_{DD1} + 0.5 V
Except GMA . . . . . –0.5 V to V_{DD2} + 0.5 V
Output voltage: EIO1, EIO2 . . . . . –0.5 V to V_{DD2} + 0.5 V
OUT1 to OUT480 . . . . . –0.5 V to V_{DD1} + 0.5 V
Storage temperature, T_{stg} . . . . . –55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- Keep the order of the V_{DD2} input port except GMA, V_{DD1}, and GMA1 to GMA10 when turning on the device, and reverse the order when turning it off.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DD1}	8		13.5	V
	V_{DD2}	2.7	3	3.6	
γ-corrected supply voltage	GMA1 to GMA5	$1/2V_{DD1}$		V_{DD1}–0.2	V
	GMA6 to GMA10	V_{SS1}+0.2		$1/2V_{DD1}$	
Clock frequency, CLK			146	152	MHz
Load capacitance, driver output (C_L), OUT1 to OUT480				125	pF
Operating free-air temperature range, T_A		–10		75	°C
Input capacitance, C_I	EIO1, EIO2		10		pF
	Except EIO and GMAn		5		

NOTE: Relation of γ-corrected input voltage
V_{DD1}>GMA1, GMAn ≤ GMAn+1 (n=1 to 9), GMA10>V_{SS1}

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electrical characteristics

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH1}	High-level input voltage	EIO1, EIO2, L/R, TP1, LCH LP, SB, POL		0.7×V_{DD2}		V_{DD2}	V
V_{IL1}	Low-level input voltage	EIO1, EIO2, L/R, TP1, LCH LP, SB, POL		0		0.25×V_{DD2}	V
$I_{I(lkg)}$	Input leakage current	EIO1, EIO2, L/R, TP1, LCH LP, SB, POL, CLKA,B, LV0A,B to LV5A,B		–1		1	µA
V_I	Mini-LVDS input voltage (center)	CLKA,B, LV0A.B to LV5A,B		0.3+(V_{ID}/2)		(V_{DD2}–1.2)–V_{ID}/2	V
V_{ID}	Mini-LVDS differential voltage (amplitude: peak to peak)	CLKA,B, LV0A,B to LV5A,B		0.2		0.6	V
$I_{O(chg)}$	Output current	OUT1 to OUT480	VX = V_{DD1}–0.2 V_O = V_X–1.0		TBD		µA
$I_{O(dis)}$			V_X = V_{SS}+0.2 V_O = V_X+1.0		TBD		µA
δV_O	Output swing difference deviation	OUT1 to OUT480	See Note 1		±10		mV
$\delta V_{O(avg)}$	Averaged output voltage deviation	OUT1 to OUT480	See Note 2		±10		mV
R_{GMA}	Ladder resistance	GMA1–GMA5 GMA6–GMA10			15850		Ω
V_O	Output voltage range	OUT1 to OUT480		V_{SS1}+0.2		V_{DD1}–0.2	V
$I_{D(dp)}$	Driver port dynamic current consumption	V_{DD1}–V_{SS1}	Black raster, V_{DD1} = 13.5 V, TP1 = 10 µs No load		TBD		mA
$I_{S(dp)}$	Driver port static current consumption	V_{DD1}–V_{SS1}	Black raster, V_{DD1} = 13.5 V, No load		TBD		mA
$I_{D(lp)}$	Logic port dynamic current consumption	V_{DD2}–V_{SS2}	TP1 = 10 µs, f_{CLK} = 110 MHz, Checkered		TBD		mA
$I_{S(lp)}$	Logic port static current consumption	V_{DD2}–V_{SS2}	No clock, no input		TBD		mA

NOTES: 1. Amplitude offset when all ports output the same data
2. Deviation in averaged amplitude offset between chips
3. Input the same value to all pairs of mini-LVDS inputs and mini-LVDS differential voltage ports.

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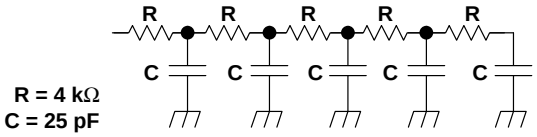
timing requirements

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Clock pulse cycle		6.5	6.8		ns
t_2	Clock pulse high period		2.5			ns
t_3	Clock pulse low period		2.5			ns
t_4	Data setup time		1.25			ns
t_5	Data hold time		1.25			ns
t_6	EIO setup time		–1			ns
t_8	EIO signal delay time	Load = 25 pF		16	TBD	ns
t_9	CLK, LV0 to LV5 rising time				0.5	ns
t_{10}	CLK, LV0 to LV5 falling time				0.5	ns
t_{15}	Driver output delay time (see Note 4)	Target voltage ±0.1 V_{DD1}			4	µs
t_{16}		6-bit accuracy			8	
t_{20}	Reset (RST) high period		50 ns over 3 CLK cycles			
t_{25}	TP1 high period		0.2			µs
t_{28}	POL setup time		–5			ns
t_{29}	POL hold time		6.0			ns
t_{30}	Receiver off to TP1 timing		5			CLK cycles
t_{31}	TP1 to reset input time		200			ns
t_{32}	Reset low to TP1 rising time		0			ns

NOTE 4: Output load condition:



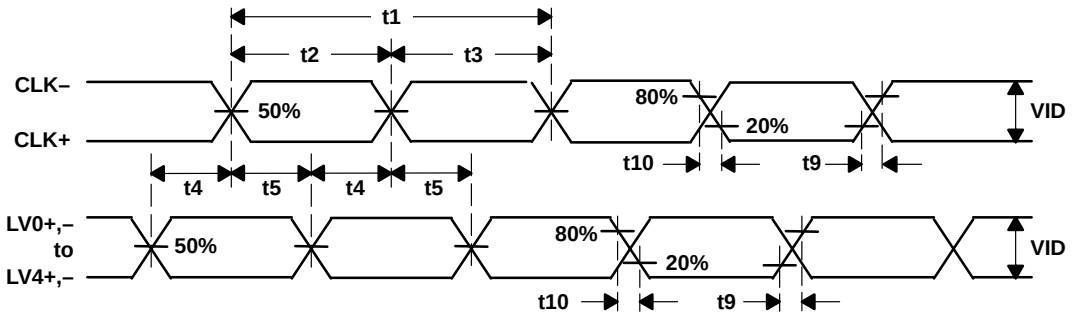
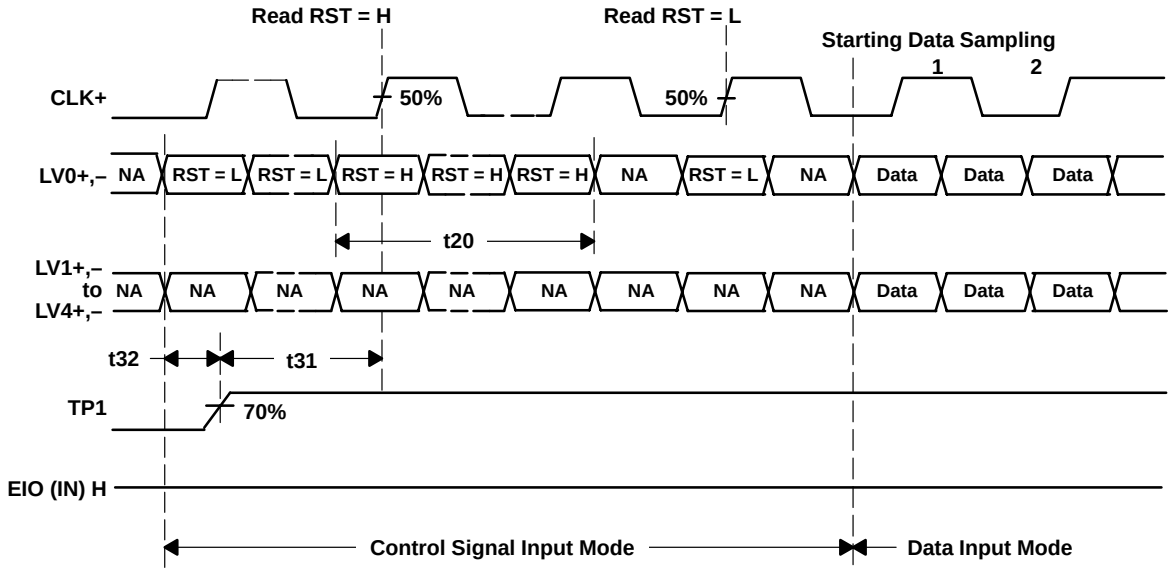


Figure 4. Data Read Timing



NOTE: No assigned data for NA

Figure 5. Input Data Timing (Lead Chip)

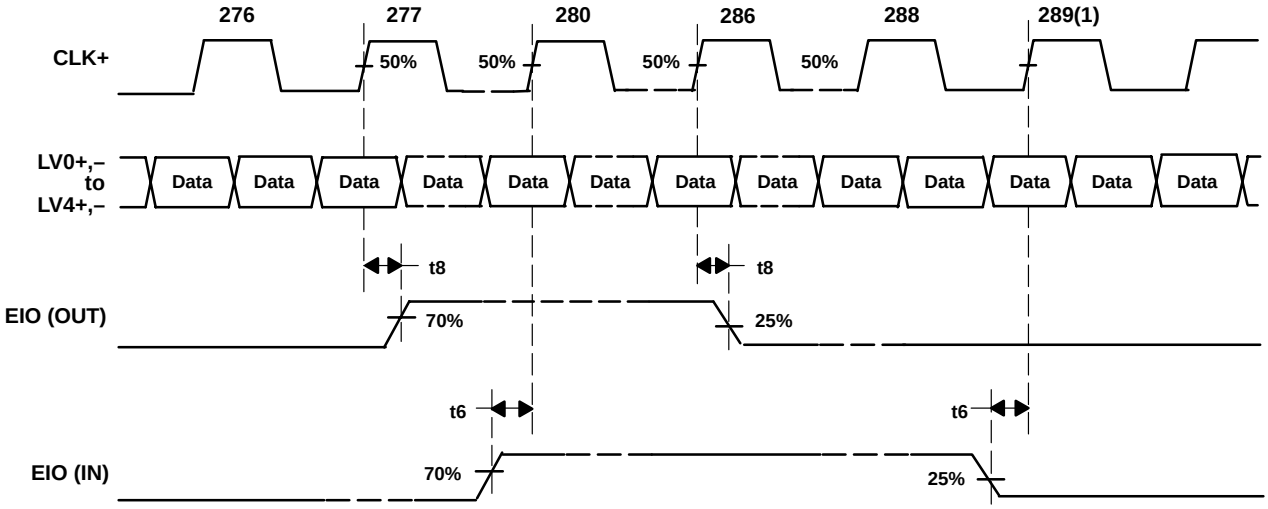
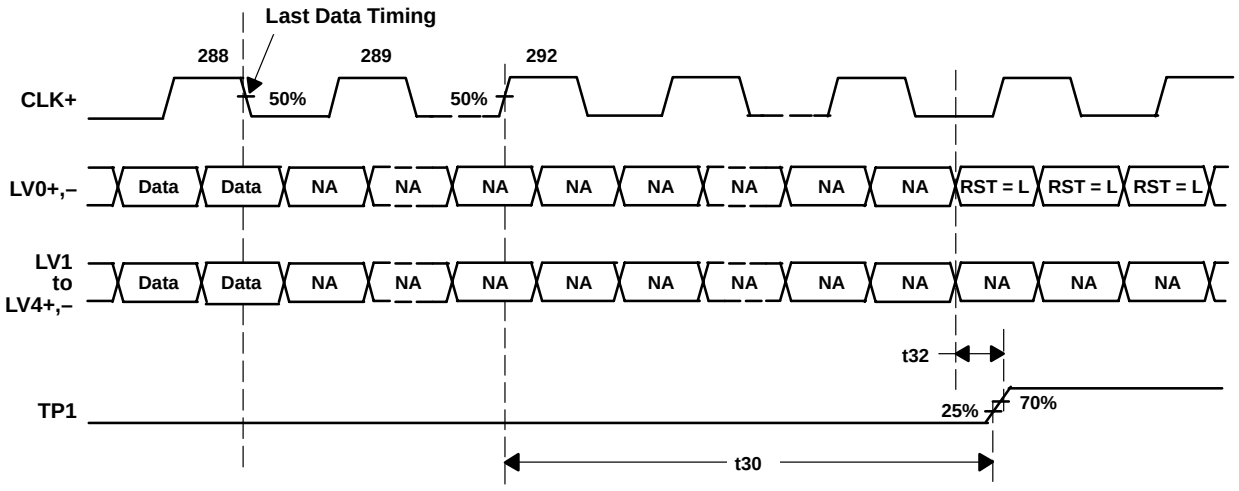


Figure 6. Input Data Timing (Cascade Port)

PRODUCT PREVIEW



NOTE: No assigned data for NA

Figure 7. Last Data Sampling to TP1 Timing

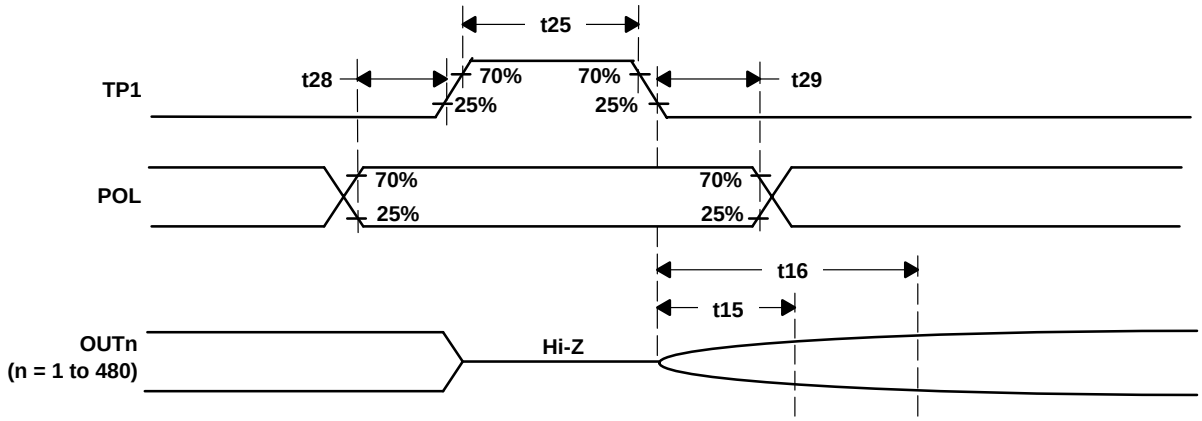


Figure 8. Output Timing

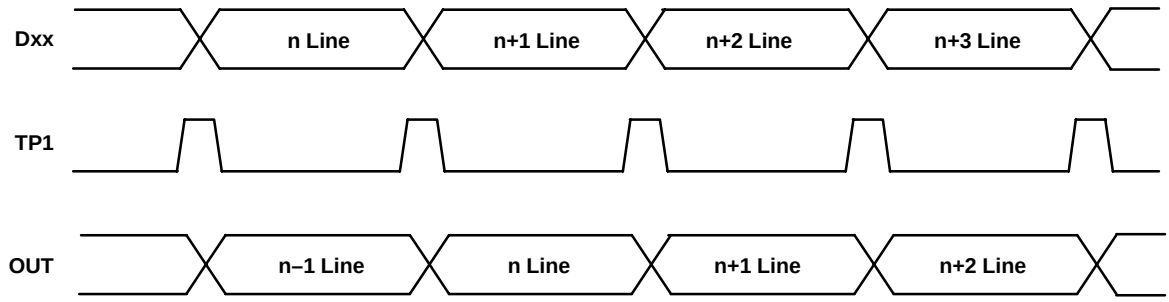


Figure 9. Relation Between Input and Output Data

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265