Application Note
February 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

Programming the *Ambassador*™ T8100, T8100A, T8102, and T8105 Registers

Introduction

This application note explains in detail how to program the *Ambassador* family of time-slot interchangers. The programming is straightforward once the reader understands the usage of the registers.

Holding Registers

There are four holding registers that are used to program the chip(s):

1. Time-slot holding register
2. Control/stream holding register
3. Tag holding register
4. Subrate/tag MSbit (for T8100A, T8102, and T8105 only)

As the name implies, these registers hold data which will be used to set/get CAM or RAM contents. Many instructions require that these registers be set up before a command is issued. When the command has executed, the holding registers still contain the original data written to them.

AMR and IDR Registers

These two registers are used together. First, a command to be performed is loaded into the AMR register. Second, the same value is loaded into the IDR register. After writing the IDR, the chip internally recognizes this read or write and executes the command.

Memory

The T8100, T8100A, T8102, and T8105 chips have memory that is designated for a particular function. For the H-bus, there are three CAMs. These are the even, odd, and local CAMs. As the name implies, the EVEN CAM is for even-numbered streams. The ODD CAM is for odd-numbered streams. The LOCAL CAM is for both even- and odd-numbered streams, when the source/destination is from/to the local bus. When programming the stream information for H-bus transfers, it is important to note that if the stream is even-numbered, then the EVEN CAM must be used. The odd-numbered streams use the ODD CAM. Using the commands MKCx, BKCx, or FENx with EVEN streams to the ODD CAM (or ODD streams to the EVEN CAM) will produce erroneous results. For EVEN CAMs, the 5-bit stream information is truncated to 4 MSbits (LSB is lost), so if stream 31 is loaded into the EVEN CAM, it will be truncated to stream 30. For the LOCAL CAM, the 5-bit stream information is truncated to 4 LSbits (MSB is lost), since only 4 bits are needed to define 16 streams.

Reading the CAMs

If subrate is disabled when reading back the data from the CAMs using RDCE, RDCO, or RDCL, the IDR register has to be read three times to get the time slot, the control/stream, and the tag. If three consecutive reads are not performed, then the next time an RDCD, RDCO, or RDCL is issued, the IDR will return the 8-bit data from where it left off. For example, issue RDCE. Read IDR once for time-slot value. Issue another RDCE. Reading the IDR will return the control/stream and not the time-slot value. To preserve alignment, perform three consecutive reads whether the information is used or not. Also, the time-slot field only occupies the lower 7 bits (6—0). The eighth bit (bit 7) is the valid bit. If there is a connection, this bit will be a one (1). If there is no connection, this bit will be a zero (0). This bit is always returned along with the 7-bit time-slot value.

Using a Command

When programming the devices, the following considerations must be addressed:

1. Is subrate switching enabled?
2. Is this a 256 or 512 device?

Use the following three rules to help evaluate the considerations described above:

1. For the T8100A, if subrate is disabled, then the fourth holding register in not used. Reading and writing uses the IDR only three times.
2. For the T8100A, if subrate is enabled, then the fourth holding register is used. Reading and writing uses the IDR four times.
3. If this is a 512 device, T8102 or T8105, and subrate is enabled or disabled, all four holding registers are used. This is because the fourth holding register holds the most significant bit of the tag field. Nine bits give 512 locations.

Command Usage

This section explains, step by step, the usage of each command. To perform a command, program the registers according to the steps listed. The syntax of the command varies whether one is programming the T8100 or the T8100A, T8102, and T8105.

```
/*************************************************************************/
/*                                                                       */
/*      T8100                                                            */
/*      T8100A with SUBRATE DISABLED                                     */
/*                                                                       */
/*************************************************************************/

COMMAND:  MKCx (E, O, L)  - for T8100 (or T8100A with subrate DISABLED)
     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xB2 (point to tag field)
     write IDR <= tag value
     write AMR <= 0xE0, 0xE1 or 0xE3 (CAM command for MKCE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM write)

Note: SYSERR is returned if you try to write to a FULL cam
/*=======================================================================*/


COMMAND:  BKCx (E, O, L) - for T8100 (or T8100A with subrate DISABLED)
     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xE4, 0xE5 or 0xE7 (CAM command for BKCE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM break)

Note: SYSERR is returned if the timeslot/stream is not found in the CAM
/*=======================================================================*/

COMMAND:  CLL (E,O,L) - for T8100 (or T8100A with subrate DISABLED)
     write LAR <= 0x00, ... or 0xFF  (physical address)
     write AMR <= 0xE8, 0xE9 or 0xEB (CAM command for CLLE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM clear)

/*=======================================================================*/

COMMAND:  RDC (E,O,L) - for T8100 (or T8100A with subrate DISABLED)

     write LAR <= 0x00, ... or 0xFF  (physical address)
     write AMR <= 0xEC, 0xED or 0xEF (CAM command for RDCE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM read)
     read IDR (returns TIMESLOT value)
     read IDR (returns CTRL/STREAM value)
     read IDR (returns TAG value)
/*=======================================================================*/
```

Command Usage (continued)

```
COMMAND:  FENx (E, O, L) - for T8100 (or T8100A with subrate DISABLED)
     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xF0, 0xF1 or 0xF3 (CAM command for FENE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM find)
     read IDR (returns MATCH ADDRESS, 8 bits for 256 locations)

     Note: SYSERR is returned if the timeslot/stream is not found in the CAM
/*=========================================================================*/

COMMAND:  (E, O, L) RSC, RCH, and CI -  for T8100 (or T8100A with subrate DISABLED)

     write AMR <= 0xF8, 0xF9, 0xFB, 0xFC, or 0xFF (CAM command for RSC, RCH, CI)
     write IDR <= same value as AMR above (this triggers the actual CAM clear)
/*=========================================================================*/


/*************************************************************************/
/*                                                                       */
/*      T8100A, or                                                       */
/*      T8102,  or                                                       */
/*      T8105   with SUBRATE ENABLED                                     */
/*                                                                       */
/*************************************************************************/

COMMAND:  MKCx (E, O, L) - for T8105 (or T8102, or T8100A with SUBRATE ENABLED)

     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xB2 (point to tag LSByte field)
     write IDR <= tag LSByte value
     write AMR <= 0xB3 (point to subrate control/tag Msbit field)
     write IDR <= subrate control/tag MSbit value
     write AMR <= 0xE0, 0xE1 or 0xE3 (CAM command for MKCE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM write)
/*=========================================================================*/

COMMAND:  BKCx (E, O, L) - for T8105 (or T8102, or T8100A with SUBRATE ENABLED)
                           (same as T8100).
     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xE4, 0xE5 or 0xE7 (CAM command for BKCE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM break)
/*=========================================================================*/
```

Command Usage (continued)

```
COMMAND:  CLL - for T8105 (or T8102, or T8100A with SUBRATE ENABLED) - same as
                 T8100, except AMR bit 5 points to upper/lower CAM range
     write LAR <= 0x00, ... or 0xFF  (physical address 8 LSBits)
     write AMR <= 0xE8, 0xE9 or 0xEB for CLL LOWER range 0-255, OR 0xC8, 0xC9 or
                  0xCB for CLL UPPER range 256-511
     write IDR <= same value as AMR above (this triggers the actual CAM clear)
/*=========================================================================*/

COMMAND:  RDC - for T8105 (or T8102, or T8100A with SUBRATE ENABLED) -
                AMR bit 5 points to upper/lower CAM range, execute 4 IDR READS
                to retrieve 4 bytes

     write LAR <= 0x00, ... or 0xFF  (physical address 8 LSBits)
     write AMR <= 0xEC, 0xED or 0xEF for RDC LOWER range 0-255, OR 0xCC, 0xCD or
                  0xCF for RDC UPPER range 256-511
     write IDR <= same value as AMR above (this triggers the actual CAM read)
     read IDR (returns TIMESLOT value)
     read IDR (returns CTRL/STREAM value)
     read IDR (returns TAG LSByte value)
     read IDR (returns subrate control/tag Msbit value)
/*=========================================================================*/

COMMAND:  FENx (E, O, L) for T8105 (or T8102, or T8100A with SUBRATE ENABLED) -
                         T8100A is identical protocol to T8100 (only 1 IDR read
                         required to retrieve 8 bits) For T8105, T8102, a second
                         IDR read is required to retrieve the 9th address bit
                         for 512 locations

     write AMR <= 0xB0 (point to timeslot field)
     write IDR <= timeslot value
     write AMR <= 0xB1 (point to ctrl/stream field)
     write IDR <= ctrl/stream value
     write AMR <= 0xF0, 0xF1 or 0xF3 (CAM command for FENE,O, or L)
     write IDR <= same value as AMR above (this triggers the actual CAM find)
     read  IDR (returns MATCH ADDRESS value LSByte)
     read  IDR (returns MATCH ADDRESS value MSB) *** this 2nd IDR read only
                required for T8102,T8105
/*=========================================================================*/

COMMANDS:  RSC, RCH and CI - for T8105 (or T8102, or T8100A with SUBRATE
                             ENABLED)- same as T8100
     write AMR <= 0xF8, 0xF9, 0xFB, 0xFC, or 0xFF (CAM command for RSC, RCH, CI)
     write IDR <= same value as  AMR above (this triggers the actual CAM clear)
/*=========================================================================*/
```

Command Usage (continued)

```
/*************************************************************************/
/*    Reading and Writing the Local Connection Memory                    */
/*                                                                       */
/*    Remarks: The command byte is divided into two parts:               */
/*             Bits 7-4 is equal to 4 or 5 depending whether it's the    */
/*             time-slot or the ctrl/stream field respectively. Bits 3-0 is  */
/*             any number from 0 to F (hex) and represents the stream.   */
/*************************************************************************/

COMMAND:    Local Bus, Connection Memory, Time-Slot Field 0x4Z where "Z"
                       is the stream number with a value of 0-F.

READ Format
   write LAR <= time-slot field
   write AMR <= 0x4Z where "Z" = stream value(0-F)
   read  IDR (returns TIMESLOT  value)

WRITE Format
   write LAR <= time-slot field
   write AMR <= 0x4Z where "Z" = stream value(0-F)
   write ID  <= time-slot value  (this triggers the actual write)
/*=======================================================================*/

COMMAND:    Local Bus, Connection Memory, Time-Slot Field 0x5Z where "Z"
                       equals 0-F.

READ Format
   write LAR <= time-slot field
   write AMR <= 0x5Z where "Z" = stream value(0-F)
   read  IDR (returns TIMESLOT  value)

WRITE Format
   write LAR <= time-slot field
   write AMR <= 0x5Z where "Z" = stream value(0-F)
   write ID  <= time-slot value  (this triggers the actual write)
/*=======================================================================*/
```

Command Usage (continued)

```
/*************************************************************************/
/* To reset the Local Connection Memory.                                 */
/*                                                                       */
/* This requires using the diagnostics mode register. There is no single in- */
/* struction to do clear the memory. This sequence of instructions will clear*/
/* all of the control bits plus a few extra of the local connection memory.  */
/*************************************************************************/

SEQUENCE:

    write AMR = 0x00      select control registers
    write LAR = 0x30      select DIAG1 register
    write IDR = 0x0C      Enable memory fill bit, pattern selected is "data
                          locations equal address bits, 9-0”. Bits 15-10 are
                          written with zero’s.
    At this point the T8100A /2/5 is/are executing the instruction. To find when
    the T8100A /2/5 has completed the operation software must poll(read) the
    same register and observe when bit 0 (DMD) is equal to a 1.

    To get out of diagnostics mode:
    write AMR = 0x30      select DIAG1 register
    write IDR = 0x00      end diagnostics mode
```

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February 1999
AP99-021NTNB

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