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Product Brief
June 2001

Excerra-8 TTSI00832 Time-Slot Interchanger (TSI)

Features

- 8K X 8K nonblocking time/space switch fabric.
- Concentration highway interface (CHI) compatible with IOM2, GCI, and SLD, and H.110 interfaces.
- 32 full-duplex, serial TDM highways (CHIs).
- Programmable CHI data rates from 2.048 Mbits/s (32 time slots) to 16.384 Mbits/s (256 time slots) data rates, independently programmable per highway.
- Frame integrity mode to ensure proper operation with wideband data (N x DS0, ISDN H-channels).
- Low latency mode for voice channels.
- Independently programmable bit and byte offsets with 1/4 bit resolution for all highways.
- 16-bit microprocessor interface allows fast access to connection data and device registers.
- Time-slot translation look-up tables allow the user to perform real-time digital transforms on outgoing TDM data.
- *IEEE** 1149.1 boundary scan (JTAG).
- Test-pattern generation and checking for on-line system testing (PRBS, QRSS, or user-defined byte).
- Low-power 1.5 V core power supply with 3.3 V digital I/O compatibility. Maximum power estimated to be 800 mW.
- 208-pin ball grid array (PBGA) package, which is 17 mm square with 1.0 mm ball pitch.
- –40° C to 85° C industrial temperature range.

Applications

- Small and medium TDM switches
- Digital loop carriers
- Digital cross connects
- Remote access concentrators with voice/IP
- Remote access servers
- Multiservice voice/IP gateways
- Multiservice access switching

Description

The TTSI00832 time-slot interchanger (TSI) is a DS0 cross-connect. The TSI receives and transmits TDM traffic via multiple concentration highway interfaces (CHI). Each CHI is independently programmed and the output CHIs support multidriver bussing. The TSI is configured via a 16-bit microprocessor interface. The microprocessor interface can be configured as a 16-bit synchronous host bus. This interface is designed to configure connection data and access device registers. Each CHI has a programmable data rate (up to 16.384 Mbits/s), virtual frame offsets, and individually controlled transmit and receive configurations. The TTSI00832 has internal circuitry to ensure frame integrity. Frame integrity is a requisite feature for applications that switch wideband data (i.e., N x DS0 or ISDN H-channels). Low latency mode is available for voice applications where reduced latency is an advantage.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Overview

The TTSI00832 time-slot interchanger is an 8K X 8K nonblocking time-slot (DS0) switch for use with serial TDM data streams. The TSI comprises several major design elements: receive TDM logic, microprocessor interface, interchange fabric, transmit TDM logic, CHI logic, clock/reset logic, JTAG/UBS logic, and test pattern generation and monitoring (TPG/TPM) logic. Figure 1 represents a high-level block diagram of the TTSI00832.

The TSI switches DS0 data received from two types of TDM links (streams). The CHI is a very flexible link that can be programmed to interface to most serial TDM data links. Each of these CHIs can contain a minimum of 32 time slots at 2.048 Mbits/s to a maximum of 256 time slots at 16.384 Mbits/s. The interchange fabric stores the time-slot data and the switch parameters. The interchange fabric can rearrange time-slot data in time (order within a frame) and space (among data links). The microprocessor interface provides fast access to the device's registers and switching configuration memory. The TSI is configured via microprocessor interface. The microprocessor interface allows fast access to time-slot data and device registers. The microprocessor interface is a 16-bit interface compatible with most synchronous general-purpose processors.

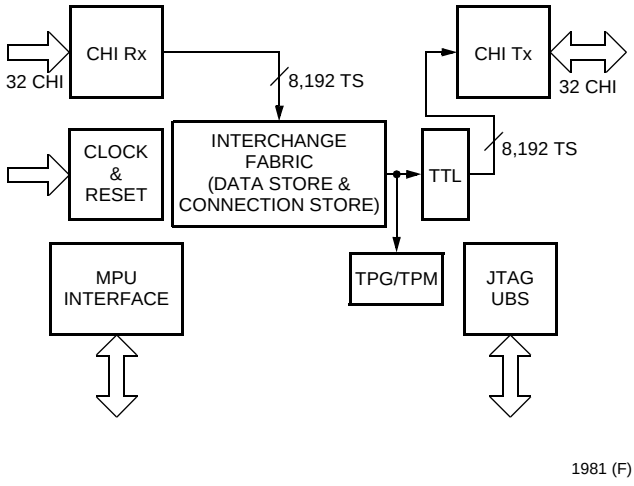

Figure 1. Functional Diagram of Time-Slot Interchanger

Interchange Fabric

The interchange fabric performs the nonblocking switching function, and its core has a memory for the time-slot data and another memory for the switching configuration. The interchange fabric switches any of the 8192 possible incoming time slots to any of the 8192 possible outgoing time slots. The interchange fabric performs this switching function without regard to the physical link from which the time slot was taken, which allows this TSI to be called a time-space switch.

An important feature of the interchange fabric is the ability to select one of two latency modes on a per-time-slot (DS0) basis: frame integrity and low latency. Frame integrity mode ensures proper operation with wideband data by getting all of the time slots in an output frame from the same input frame. Low latency mode minimizes delay for voice applications.

Expansion

To interconnect more DS0 traffic than 8K input and 8K output time slots, which a single TSI allows, a geometric expansion of TSIs will be needed. The best alternative would be to use the TTSI01664 or the TTSI14464 device. Read the *Excerra-144* Product Brief for more details.

Microprocessor Interface

The TSI has a versatile 16-bit microprocessor interface, that provides fast access to its registers and switching configuration memory. This interface is designed to connect directly to the address and data buses of a synchronous general-purpose microprocessor.

Concentration Highway Interface (CHI)

The TSI transmits and receives time slot data via 32 transmit CHIs and 32 receive CHIs which are single-ended serial TDM links. A programmable clock signal and a global frame-synch signal provide the required timing references to the CHI Interface. The TSI supports CHIs with unaligned framing; that is, each CHI's offset from the frame-synchronous signal is independently programmable. The transmit CHIs may be placed into the high-impedance (Hi-Z) state to allow bussing of multiple drivers. Each physically identical CHI may be independently configured for direct connection to a variety of serial TDM interfaces operating at a variety of data rates, including IOM2, GCI, SLD and H110. The CHI supports data rates from 2.048 Mbits/s (32 time slots) to 16.384 Mbits/s (256 time slots).

Test Pattern Generator and Monitor

The test pattern generator (TPG) and test pattern monitor (TPM) is a set of configurable test logic for support of transmission facility testing and maintenance. This block can supply and check any one of the test patterns defined in ITU-T O.150, O.151, or O.152 as well as user-defined patterns. Any combination of DS0s can be concatenated as a single broadband stream to test high-speed facilities. Additionally, the TPG/TPM provides the ability to perform diagnostic tests at both the system and chip levels of operation. System level troubleshooting is facilitated with full narrow-band/wide-band test pattern generation and detection. Extensive chip-level testing can quickly be performed with specialized test pattern generation and monitoring functions targeted at the CHI interface as well as the interchange fabric itself. The self-test abilities of this chip will simplify testing, operation, and maintenance of this product.

Time-Slot Transform Logic (Look-up Tables)

The time-slot transform logic (TTL) is a set of 16 look-up tables that are inserted in the TDM path at the output of the interchange fabric. This allows the end user to perform real-time digital transforms on the outgoing TDM data. These look-up tables are user programmable and are useful for various TDM related transform functions such as µ-law to a-law conversion or gain adjustment. The various transforms can be enabled on a per-time-slot basis using data stored in the connection store.

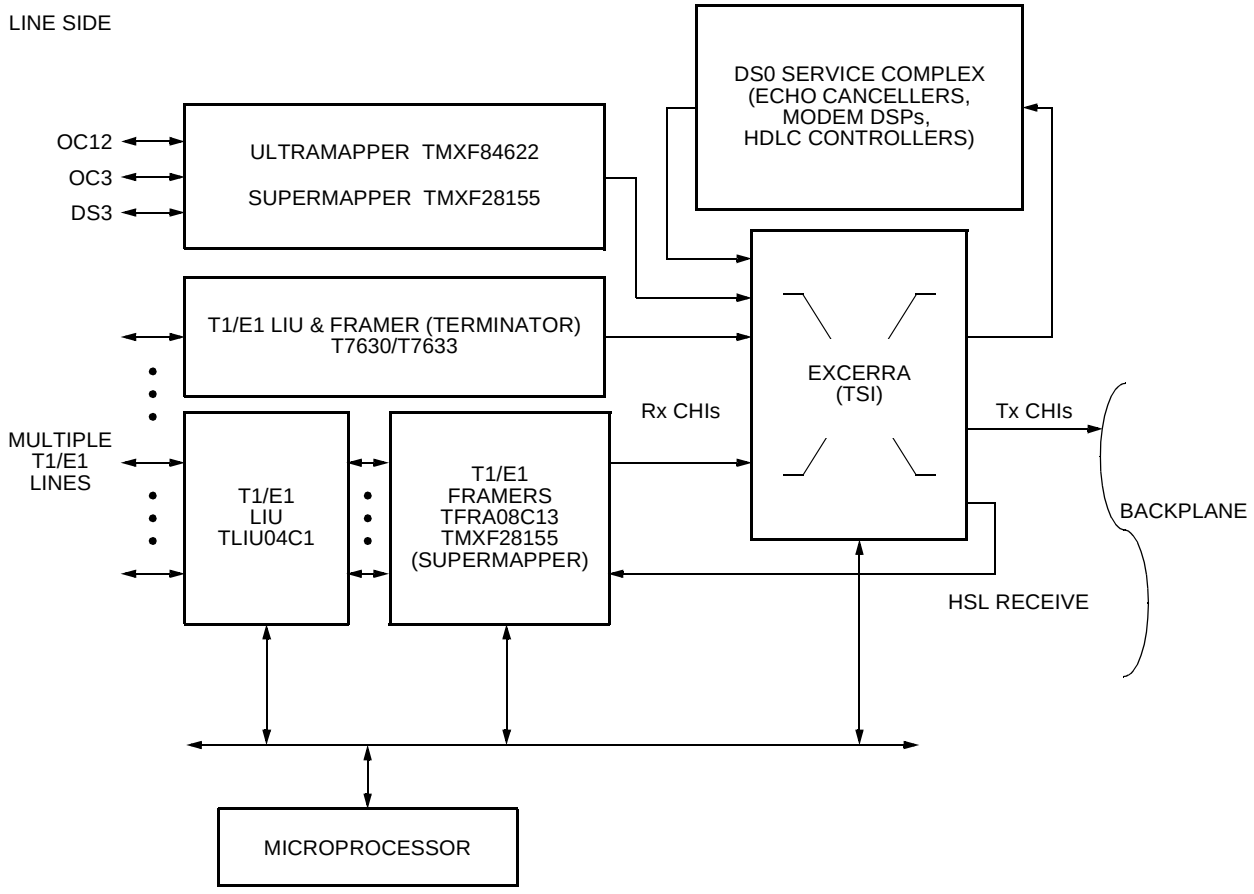

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Figure 2. Typical TSI Application

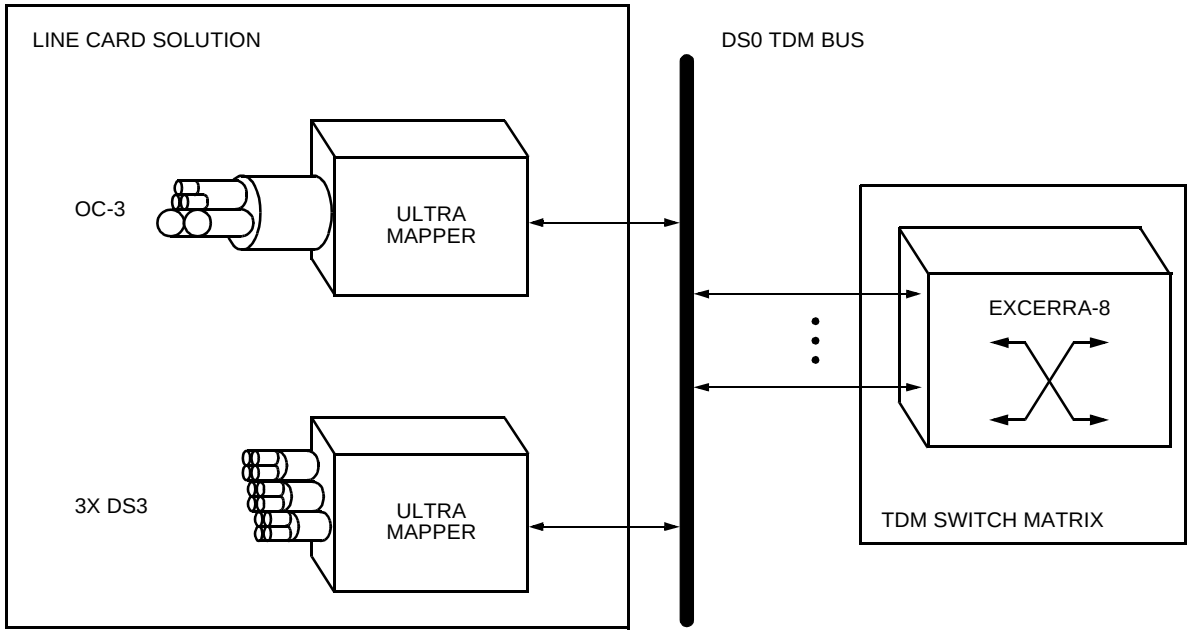

Figure 3. High Capacity Channelized Aggregation Solution

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