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Product Brief
June 2001

Excerra-144 TTSI14464 Time-Slot Interchanger (TSI)

Features

- 144K X 16K nonblocking time/space switch fabric.
- Concentration highway interface (CHI) compatible with IOM2, GCI, and SLD, and H.110 interfaces.
- 64 full-duplex, serial TDM highways (CHIs).
- Programmable CHI data rates from 2.048 Mbits/s (32 time slots) to 16.384 Mbits/s (256 time slots) data rates, independently programmable per highway.
- 16 high-speed serial links operate at an STS-12 data rate (622.08 Mbits/s) utilizing pseudo-SONET framing.
- Frame integrity mode to ensure proper operation with wideband data (N x DS0, ISDN H-channels).
- Low latency mode for voice channels.
- Independently programmable bit and byte offsets with 1/4 bit resolution for all highways.
- 16-bit microprocessor interface allows fast access to connection data and device registers.
- Expandable architecture (ability to cascade multiple devices to make larger switches).
- Time-slot translation look-up tables allow the user to perform real-time digital transforms on outgoing TDM data.
- *IEEE** 1149.1 boundary scan (JTAG).
- Test-pattern generation and checking for on-line system testing (PRBS, QRSS, or user-defined byte).
- Low-power 1.5 V core power supply with 3.3 V digital I/O compatibility. Maximum power estimated to be 2 W.
- 388-pin ball grid array (PBGA) package, which is 27 mm square with 1.0 mm ball pitch.
- –40° C to 85° C industrial temperature range.

Applications

- Small and medium TDM switches
- Digital loop carriers
- Digital cross connects
- Remote access concentrators with voice/IP
- Remote access servers
- Multiservice voice/IP gateways
- Multiservice access switching

Description

The TTSI14464 time-slot interchanger (TSI) is a DS0 cross-connect. The TSI receives and transmits TDM traffic via multiple concentration highway interfaces (CHI) and multiple high speed serial links (HSLs). The high-speed serial links permit the creation of large distributed switch fabrics. Each CHI is independently programmed and the output CHIs support multidriver bussing. The TSI is configured via a 16-bit microprocessor interface. The 16-bit microprocessor can be configured as a synchronous host bus. This interface is designed to configure connection data and access device registers. Each CHI has a programmable data rate (up to 16.384 Mbits/s), virtual frame offsets, and individually controlled transmit and receive configurations. The TTSI14464 has internal circuitry to ensure frame integrity. Frame integrity is a requisite feature for applications that switch wideband data (i.e., N x DS0 or ISDN H-channels). Low latency mode is available for voice applications where reduced latency is an advantage.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Overview

The TTSI14464 time-slot interchanger is a 144K X 16K nonblocking time-slot (DS0) switch for use with serial TDM data streams. The TSI comprises several major design elements: receive TDM logic, microprocessor interface, interchange fabric, transmit TDM logic, CHI logic, HSL logic, clock/reset logic, JTAG/UBS logic, and test pattern generation and monitoring (TPG/TPM) logic. Figure 1 represents a high-level block diagram of the TTSI14464.

The TSI switches DS0 data received from two types of TDM links (streams). The CHI is a very flexible link that can be programmed to interface to most serial TDM data links. Each of these CHIs can contain a minimum of 32 time slots at 2.048 Mbits/s to a maximum of 256 time slots at 16.384 Mbits/s. Each HSL operates at an STS-12 data rate (622.08 Mbits/s) and caries 8192 time slots. The TSI's high speed interface (HSI) handles 16 receive HSLs and 16 transmit HSLs. TDM traffic can be received via the high-speed serial interface. The HSLs can be programmed to broadcast either unswitched or switched TDM data. Moreover, the high-speed serial data links allow the TTSI14464 to be scaled linearly from 144K X 16K switch to a 144K X 144K switch for use in large distributed switch fabrics. The HSIRx and CHIRx blocks format the TDM data for storage in the switch fabric. The interchange fabric stores the time-slot data and the switch parameters. The interchange fabric can rearrange time-slot data in time (order with in a frame) and space (among data links). The HSITx and CHITx blocks perform the inverse function of the receive interface. They format the byte-wide time-slot data for transmission on the CHI or HSL interface. The HSL interface decodes the received TDM data and encodes TDM data for transmission over the HSLs. The transmit HSLs are programmable to broadcast either unswitched (a copy of what comes in via the CHIs) or switched TDM data (output from the interchange fabric). The microprocessor interface provides fast access to the device's registers and switching configuration memory. The TSI is configured via microprocessor interface. The microprocessor interface allows fast access to time-slot data and device registers. The microprocessor interface is a 16-bit interface compatible with most synchronous general-purpose processors.

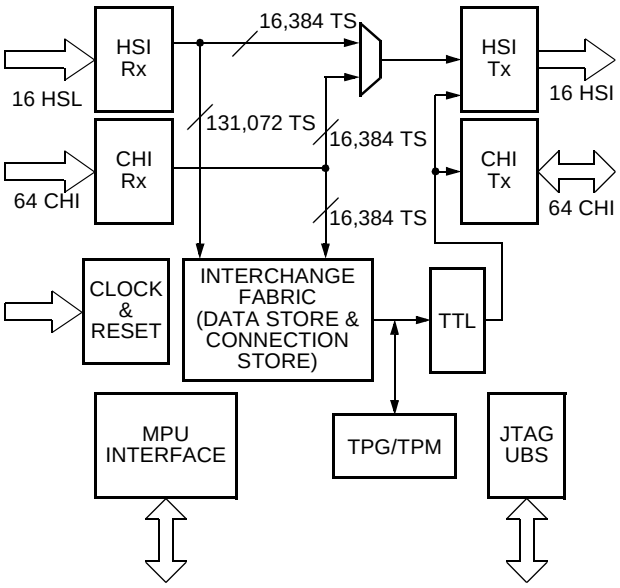

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Figure 1. Functional Diagram of Time-Slot Interchanger

Interchange Fabric

The interchange fabric performs the nonblocking switching function, and its core has a memory for the time-slot data and another memory for the switching configuration. The interchange fabric switches any of the 147456 possible incoming time slots to any of the 16384 possible outgoing time slots. The interchange fabric performs this switching function without regard to the physical link from which the time slot was taken, which allows this TSI to be called a time space switch.

An important feature of the interchange fabric is the ability to select one of two latency modes on a per-time-slot (DS0) basis: frame integrity and low latency. Frame integrity mode ensures proper operation with wideband data by getting all of the time slots in an output frame from the same input frame. Low latency mode minimizes delay for voice applications.

Expansion

To interconnect more DS0 traffic than 144K input and 16K output time slots which a single TSI allows, multiple TSIs can be combined into a fabric using the HSLs. The rectangular architecture of the TSI allows linear scaling of a nonblocking switching fabric of n (from one to nine) TSIs to a size of 144K x n * 16K. Figure 2 illustrates the largest linearly-scaled non-blocking switching system employing nine TSIs. Beyond a nine-TSI switching fabric, a nonblocking architecture, while possible, is impractical since the number of TSIs required in the fabric increases geometrically. Customers with needs for larger switching fabrics should contact their Agere Field Applications Engineer.

Microprocessor Interface

The TSI has a versatile 16-bit microprocessor interface, which provides fast access to its registers and switching configuration memory. This interface is designed to connect directly to the address and data buses of a synchronous general-purpose microprocessor.

Concentration Highway Interface (CHI)

The TSI transmits and receives time-slot data via 64 transmit CHIs and 64 receive CHIs which are single-ended serial TDM links. A programmable clock signal and a global frame-synch signal provide the required timing references to the CHI Interface. The TSI supports CHIs with unaligned framing; that is, each CHI's offset from the frame-synchronous signal is independently programmable. The transmit CHIs may be placed into the high-impedance (Hi-Z) state to allow bussing of multiple drivers. Each physically identical CHI may be independently configured for direct connection to a variety of serial TDM interfaces operating at a variety of data rates, including IOM2, GCI, SLD, and H.110. The CHI supports data rates from 2.048 Mbits/s (32 time slots) to 16.384 Mbits/s (256 time slots).

High-Speed Serial Link Interface (HSI)

The HSI provides a robust interface for high-speed serial communication across a backplane. It provides multichannel clock/data timing recovery with serial-to-parallel demultiplexing for inbound data and parallel-to-serial multiplexing for outbound data (SERDES). Outbound parallel data from the interchange fabric will be inserted into pseudo-SONET frames and transmitted over the HSLs. Inbound data from the HSLs is received by the HSI, the framing and overhead are removed, and the parallel data is sent to the interchange fabric. The use of pseudo-SONET framing for the high-speed serial format provides robust framing and error detection.

Test Pattern Generator and Monitor

The test pattern generator (TPG) and test pattern monitor (TPM) is a set of configurable test logic for support of transmission facility testing and maintenance. This block can supply and check any one of the test patterns defined in ITU-T O.150, O.151, or O.152 as well as user-defined patterns. Any combination of DS0s can be concatenated as a single broadband stream to test high-speed facilities. Additionally, the TPG/TPM provides the ability to perform diagnostic tests at both the system and chip levels of operation. System level trouble-shooting is facilitated with full narrow-band/wide-band test pattern generation and detection. Extensive chip-level testing can quickly be performed with specialized test pattern generation and monitoring functions targeted at the CHI and HSL interfaces as well as the interchange fabric itself. The self-test abilities of this chip will simplify testing, operation, and maintenance of this product.

Time-Slot Transform Logic (Look-up Tables)

The time-slot transform logic (TTL) is a set of 16 look-up tables that are inserted in the TDM path at the output of the interchange fabric. This allows the end user to perform real-time digital transforms on the outgoing TDM data. These look-up tables are user programmable and are useful for various TDM related transform functions such as µ-law to a-law conversion or gain adjustment. The various transforms can be enabled on a per-time-slot basis using data stored in the connection store.

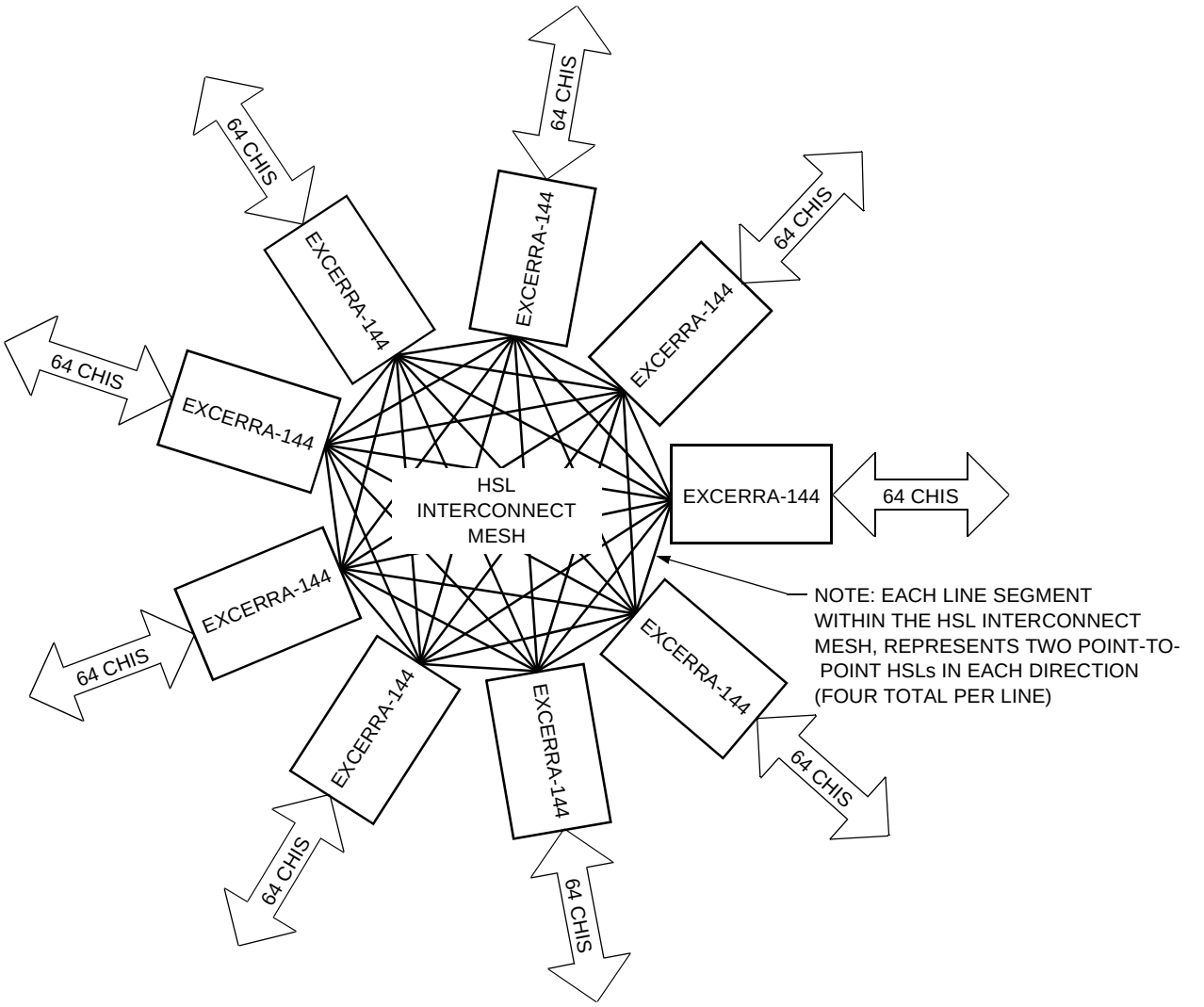

Figure 2. Combining TSIs to Form Larger Switch Fabrics

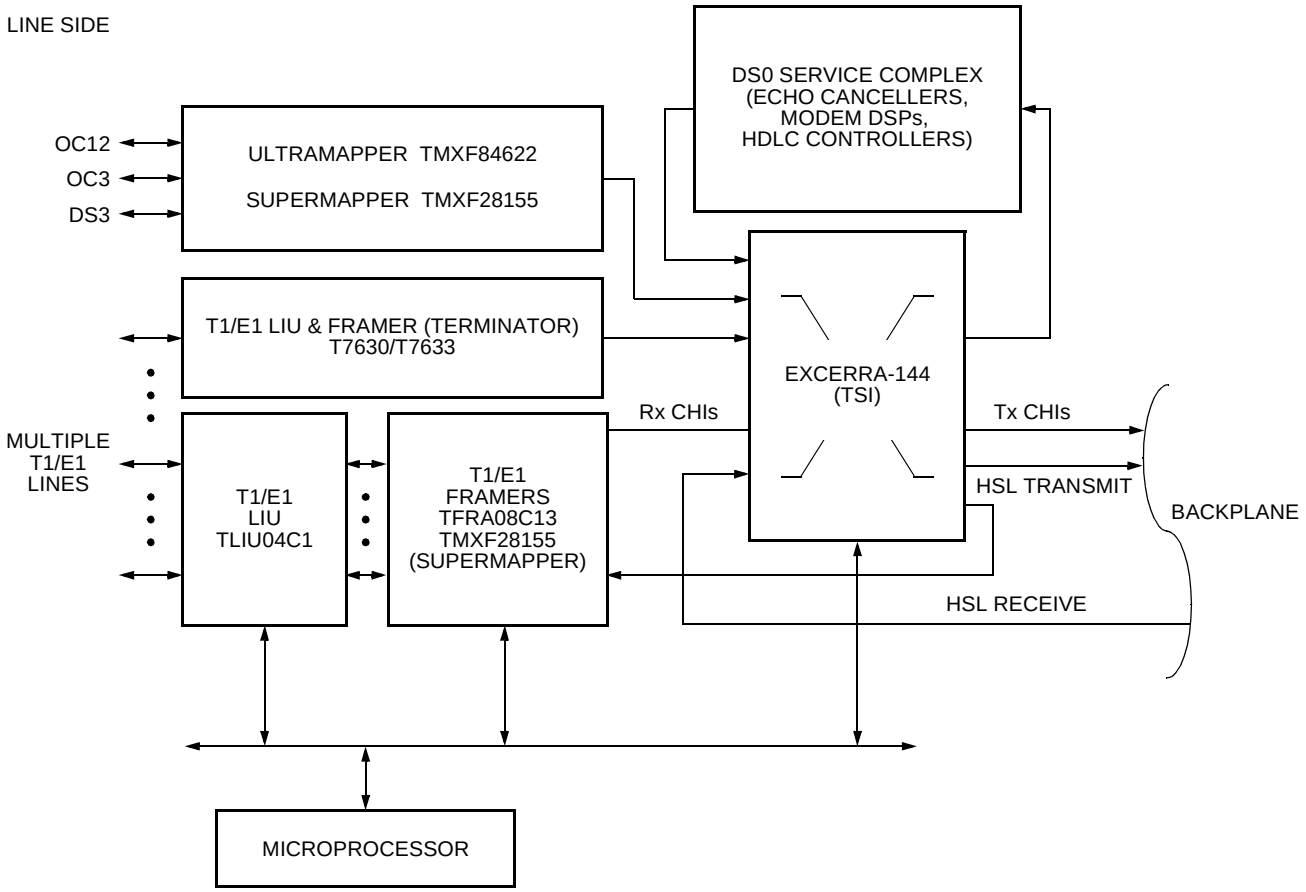

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Figure 3. Typical TSI Application

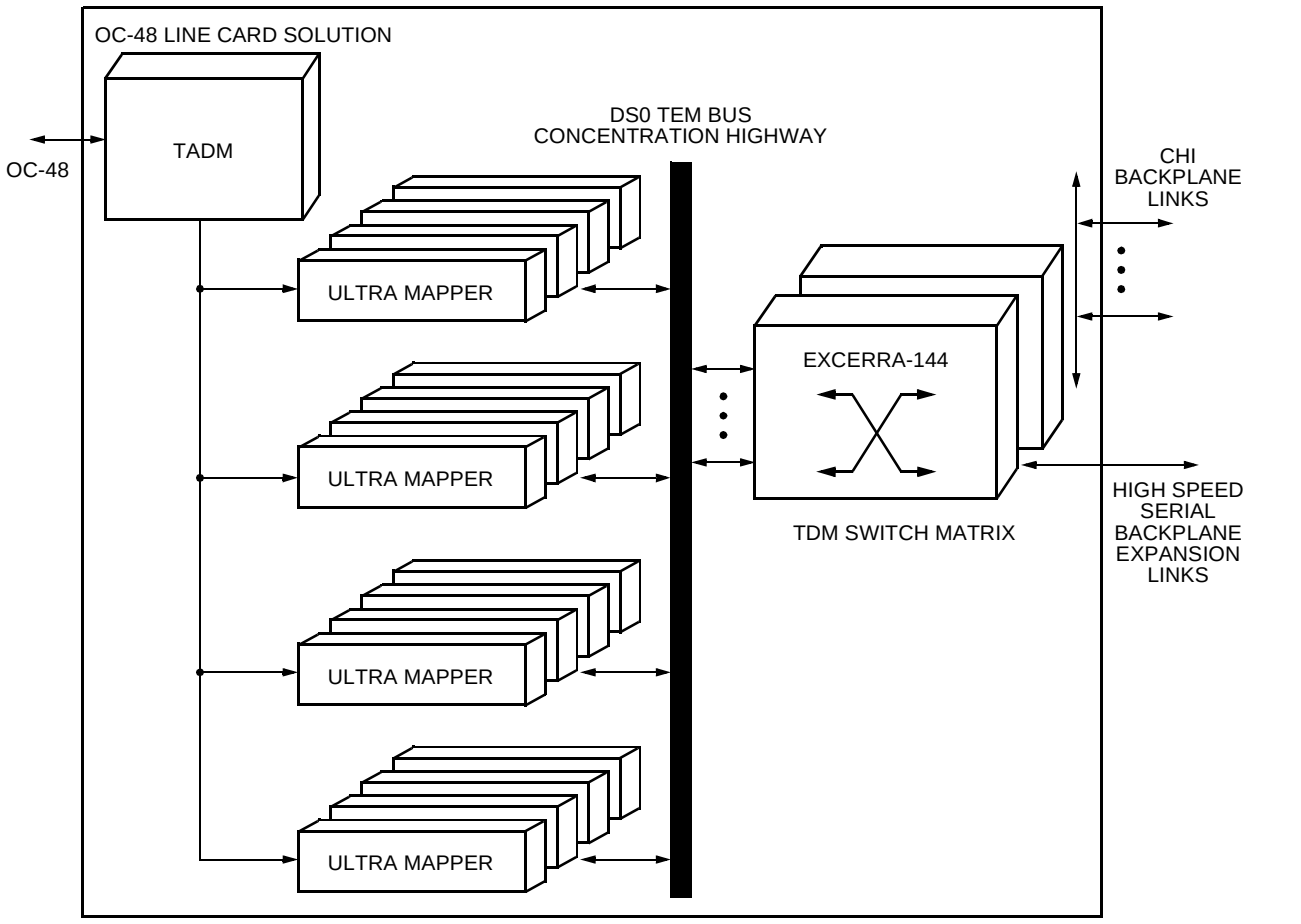

Figure 4. High Capacity OC-48 Channelized Aggregation Solution

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Agere Systems Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Agere Systems (Shanghai) Co., Ltd., 33/F Jin Mao Tower, 88 Century Boulevard Pudong, Shanghai 200121 PRC
Tel. (86) 21 50471212, FAX (86) 21 50472266
JAPAN: Agere Systems Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

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