

Intel® TRN4035BS 10Gbps Optical Serializer/Deserializer Transceiver

16-Channel 622Mbps Multiplexer/Demultiplexer

Product Overview

The Intel® TRN4035BS line of 10Gbps Serializer/Deserializer (SerDes) transceivers is designed to provide a SONET/SDH-compliant interface between the photonic physical layer and the electrical section layer. The module is comprised of an optical transmitter and receiver pair integrated with electrical Multiplexer (MUX) and Demultiplexer (DeMUX) functions. The transmitter section MUXs 16 channels at 622Mbps from a differential Low Voltage Differential Signaling (LVDS) parallel data bus into a 9.95328Gbps optical signal launched into a single-mode optical fiber pigtail. The receiver section DeMUXs a single 9.95328Gbps optical signal back to 16-channel parallel 622Mbps differential LVDS electrical signals. The receiver includes a photodiode, transimpedance amplifier, clock data recovery, decision circuit, and DeMUX. The receiver operates over both 1310nm and 1550nm bands and is compliant with SONET/SDH OC-192/STM 64 physical layer specifications. A block diagram of the module is provided on the reverse side.

The SerDes transceiver is assembled in a Multi-Source Agreement (MSA)-compatible 4.0" L x 3.5" W x 0.53" H package. The heat sinking was designed for 55°C ambient temperature/200 linear feet per minute airflow, with alternative heat sinking options also available. The LVDS interface connection is made using an MSA-compliant 300-pin Berg* MEG-array connector with standard pin-out. Optical connections are made with standard SC-UPC, FC-UPC, or LC-UPC optical connectors.



Both short and intermediate reach versions are compliant with Telcordia GR-253 requirements for OC-192 SONET interfaces. The short reach versions are intended for link spans of 2km or 12km, using a 1310nm Distributed Feedback laser source and a PIN photodetector. The intermediate reach version is intended for link spans up to 40km and uses a 1550nm Externally Modulated Laser as the transmitter and a PIN photodetector as the receiver.

Applications

OC-192 SONET/SDH equipment, including:

- Optical switches and routers
- Cross connects
- Add/drop MUXs
- Dense wavelength division multiplex terminals
- Other WDM and non-WDM metro system equipment
- Optical test equipment

The schematic diagram illustrates the internal architecture of the IC EPROM. It features a central MUX (Multiplexer) and a CDR/DeMUX (Clock Data Recovery/De-Multiplexer) block. The MUX is connected to various input pins including TxRESET, TxCLKP(N), TxMCLKP(N), TxLOCKERR, TxREFSEL, TxLINESEL, TxREFCLKP(N), RxMCLKP(N), RxPOCLKP(N), RxOUT 0-15 P(N), RxREFCLKP(N), RxLOCKERR, RxRESET, RxLCKREF, RxLOPOM, and RxLOSALM. The CDR/DeMUX is connected to RxMCLKP(N), RxPOCLKP(N), RxOUT 0-15 P(N), RxREFCLKP(N), RxLOCKERR, RxRESET, RxLCKREF, RxLOPOM, and RxLOSALM. A 10GHz CLK signal is provided to the MUX and the Clock Multiplier. The Clock Multiplier is connected to the PLL (Phase-Locked Loop) and the Clock Select block. The PLL is connected to the Clock Select block and the CDR/DeMUX. The Clock Select block is connected to the CDR/DeMUX. The CDR/DeMUX is connected to the PIN/TIA Receiver (Pin-to-Internal Transistor Array Receiver). The PIN/TIA Receiver is connected to the Rx Opt In 10Gbps pin. The PIN/TIA Receiver is also connected to the Tx Opt Out 10Gbps pin. The Tx Opt Out 10Gbps pin is connected to the Laser Transmitter. The Laser Transmitter is connected to the Driver Amp. The Driver Amp is connected to the MUX. The MUX is connected to the TxCLKP(N) pin. The TxCLKP(N) pin is connected to the TxMCLKP(N) pin. The TxMCLKP(N) pin is connected to the TxLOCKERR pin. The TxLOCKERR pin is connected to the TxREFSEL pin. The TxREFSEL pin is connected to the TxLINESEL pin. The TxLINESEL pin is connected to the TxREFCLKP(N) pin. The TxREFCLKP(N) pin is connected to the RxMCLKP(N) pin. The RxMCLKP(N) pin is connected to the RxPOCLKP(N) pin. The RxPOCLKP(N) pin is connected to the RxOUT 0-15 P(N) pin. The RxOUT 0-15 P(N) pin is connected to the RxREFCLKP(N) pin. The RxREFCLKP(N) pin is connected to the RxLOCKERR pin. The RxLOCKERR pin is connected to the RxRESET pin. The RxRESET pin is connected to the RxLCKREF pin. The RxLCKREF pin is connected to the RxLOPOM pin. The RxLOPOM pin is connected to the RxLOSALM pin. A legend indicates that solid lines represent Clock, dashed lines represent Data, and dotted lines represent Write Protect. The IC EPROM is shown as a purple rectangle with a gold pin.

- 10Gbps optical transmitter and receiver pair with 16-channel 622Mbps MUX/DeMUX
- Available in short reach (2km) and intermediate reach (40km) versions
- Multi-source agreement compatible form factor and pin configuration
- LVDS data interface via 300-pin Berg* MEG-array connector

- Integral heat sinking designed for 200 linear feet per minute, 55°C ambient airflow; optional heat sinks for higher temperature and/or lower airflow conditions
- Laser bias, laser temperature, laser power, and receiver power monitors
- Rx and Tx loss of lock, Rx loss of signal, laser bias, and laser temperature alarms
- Integrated power supply sequencing

Item	Description	Order Number
Evaluation Board	■ Intel® EVL4035BS-002 Evaluation Board	Contact local sales rep

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