PART 5

TMP68305F-16

Chapter 1 Introduction

TMP68305 uses the 68HC000, the CMOS version of the 68000, as its core processor. It also includes peripheral circuits such as a serial interface, timer, interrupt controller, DMA controller, clock generator, and address decoder.

In addition, TMP68305 can directly use 68000 development environments and software resources.

- Core processor 68HC000
- Minimum instruction execution time : 240 ns (with 16.67 MHz-system clock)
- 17 32-bit registers
- 16M-byte direct addressing
- 56 powerful basic instructions
- 14 addressing modes

- 2-channel asynchronous serial interface
- 1-channel 16-bit timer/counter
- 9-channel interrupt controller (4 external channels, 5 internal channels)
- 2-channel DMA controller (8MB/s max.)
- Clock generator (duty controller built in)
- 4-channel chip-select signal output ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$)
- Bus monitor function
- Low power consumption (CMOS)
- 100-pin QFP

TMP68305 has two operating modes: normal operating mode, and emulation mode that enables use of an in-circuit emulator (ICE), a 68000 development tool. In emulation mode, the 68HC000 core built into TMP68305 is disconnected from the bus, and the internal peripheral circuits are controlled by address, data, and control signals from the development tool.

The 68HC000 core built into TMP68305 is the same as the standard TMP68HC000, except that 8-bit peripheral device control signals E, $\overline{VPA}$, and $\overline{VMA}$ are disabled. For 68HC000 operation and instructions, refer to your TLCS-68000 Data Book.

Figure 1.1 is the TMP68305 block diagram.

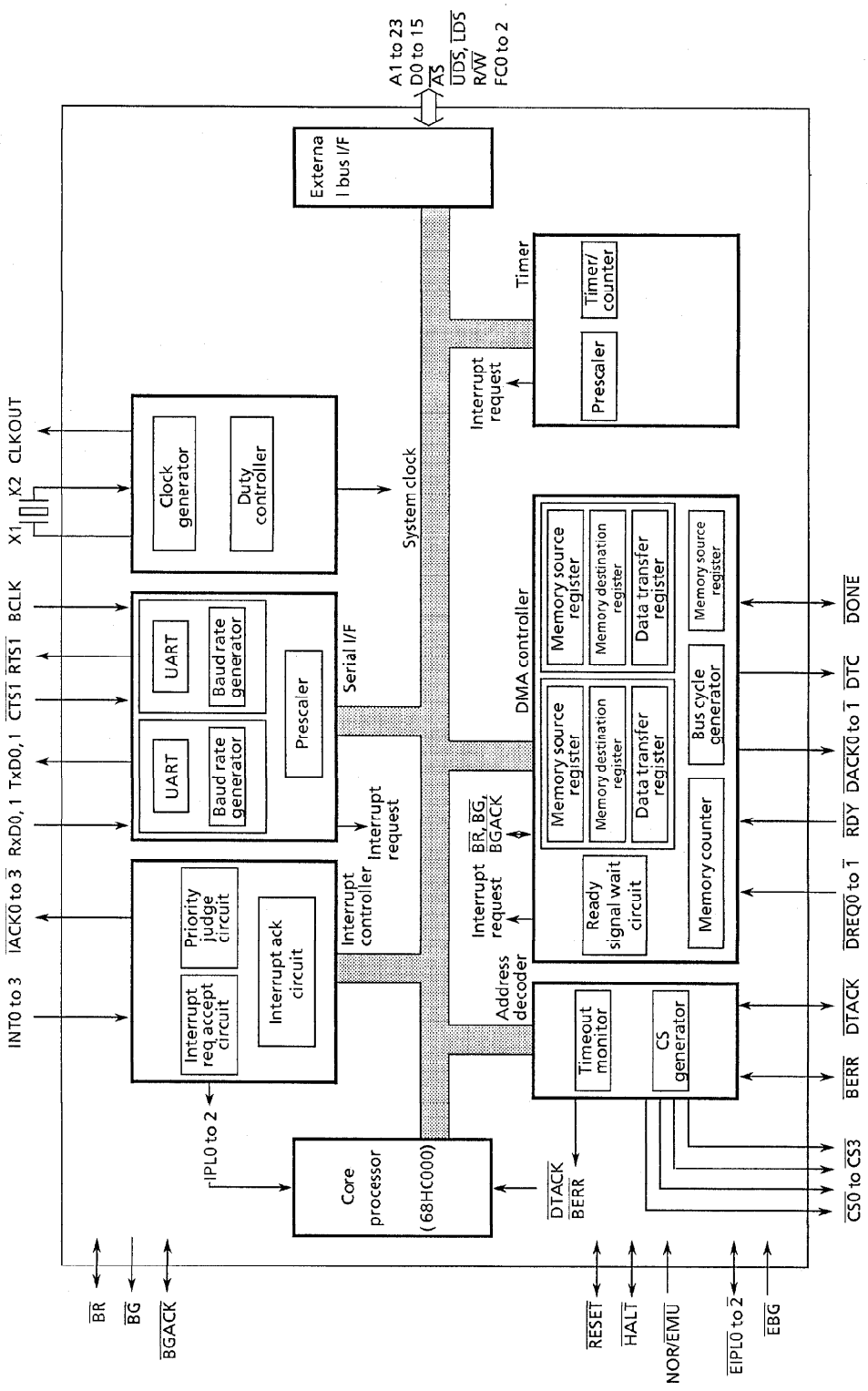

Figure 1.1 TMP68305 Block Diagram