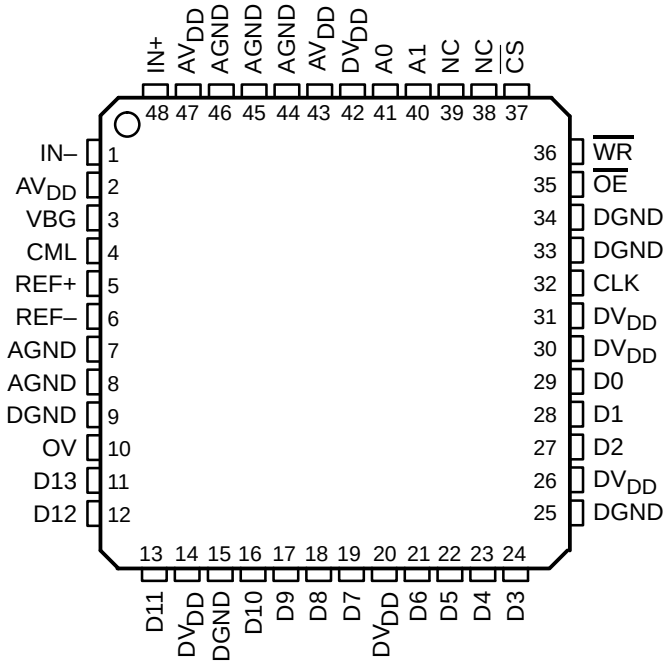
features

- 14-Bit Resolution
- 1, 3, and 8 MSPS Speed Grades Available
- Differential Nonlinearity (DNL) ±0.6 LSB Typ
- Integral Nonlinearity (INL) ±1.5 LSB Typ
- Internal Reference
- Differential Inputs
- Programmable Gain Amplifier
- µP Compatible Parallel Interface
- Timing Compatible With TMS320C6000 DSP
- 3.3-V Single Supply
- Power-Down Mode
- Monolithic CMOS Design

applications

- xDSL Front Ends
- Communication
- Industrial Control
- Instrumentation
- Automotive

PFB AND PHP PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

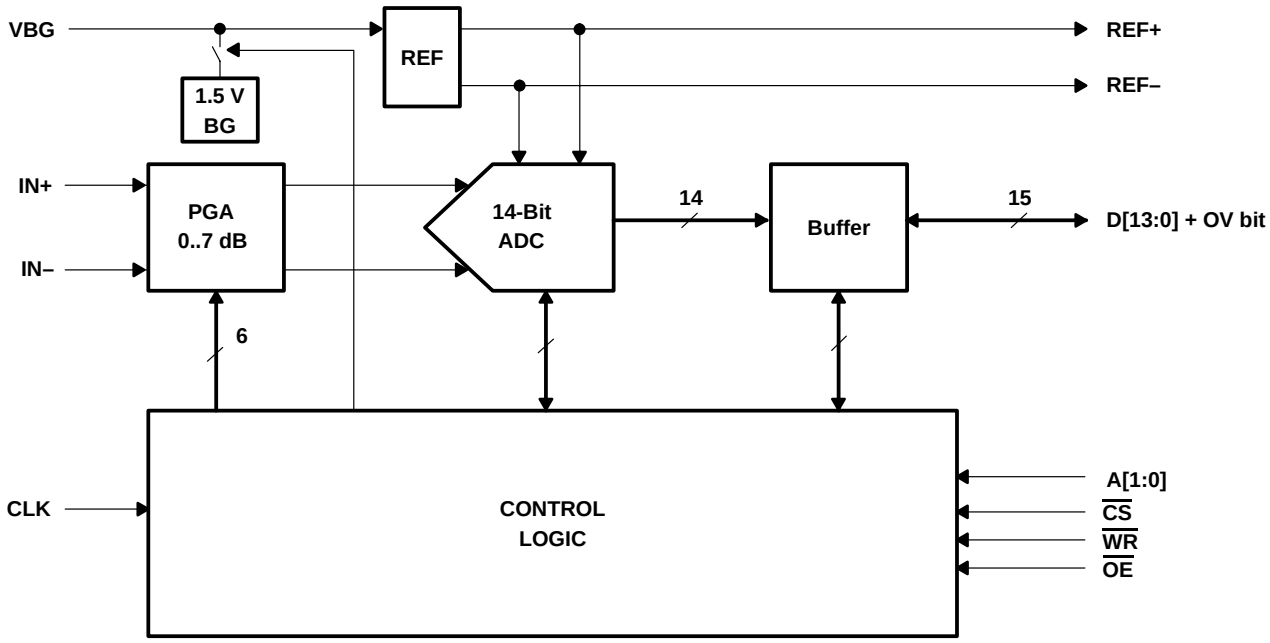
description

The THS1401, THS1403, and THS1408 are 14-bit, 1/3/8 MSPS, single supply analog-to-digital converters with an internal reference, differential inputs, programmable input gain, and an on-chip sample and hold amplifier.

Implemented with a CMOS process, the device has outstanding price/performance and power/speed ratios. The THS1401, THS1403, and THS1408 are designed for use with 3.3-V systems, and with a high-speed µP compatible parallel interface, making them the first choice for solutions based on high-performance DSPs like the TI TMS320C6000 series.

The THS1401, THS1403, and THS1408 are available in a TQFP-48 package in standard commercial and industrial temperature ranges. The THS1401, THS1403, and THS1408 are available in a PQFP-48 package in automotive temperature range, and the THS1408 is available in a PQFP-48 package in military temperature range.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	
	TQFP (PFB)	PQFP (Power Pad) (PHP)
0°C to 70°C	THS1401CPFB, THS1403CPFB, THS1408CPFB,	—
–40°C to 85°C	THS1401IPFB, THS1403IPFB, THS1408IPFB	—
–40°C to 125°C	—	THS1401QPHP, THS1403QPHP, THS1408QPHP
–55°C to 125°C	—	THS1408MPHP

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A[1:0]	40, 41	I	Address input
AGND	7,8, 44, 45, 46		Analog ground
AV_{DD}	2, 43, 47		Analog power supply
CLK	32	I	Clock input
CML	4		Reference midpoint. This pin requires a 0.1-μF capacitor to AGND.
$\overline{CS}$	37	I	Chip select input. Active low
DGND	9, 15, 25, 33, 34		Digital ground
DV_{DD}	14, 20, 26, 30, 31, 42		Digital power supply
D[13:0]	11, 12, 13, 16, 17, 18, 19, 21, 22, 23, 24, 27, 28, 29	I/O	Data inputs/outputs
NC	38, 39		No connection, do not use. Reserved
IN+	48	I	Positive differential analog input
IN–	1	I	Negative differential analog input
$\overline{OE}$	35	I	Output enable. Active low
OV	10	O	Out of range output
REF+	5	O	Positive reference output. This pin requires a 0.1-μF capacitor to AGND.
REF–	6	O	Negative reference output. This pin requires a 0.1-μF capacitor to AGND.
VBG	3	I	Reference input. This pin requires a 1-μF capacitor to AGND.
$\overline{WR}$	36	I	Write signal. Active low

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, (AV_{DD} to AGND) 4V
Supply voltage, (DV_{DD} to DGND) 4V
Reference input voltage range, VBG . . . . . – 0.3 V to AV_{DD} + 0.3 V
Analog input voltage range . . . . . – 0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . – 0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Q suffix . . . . . –40°C to 125°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

		TYP	UNIT
Thermal resistance, junction-to-ambient, Θ_{JA}	PFB package	85.9	°C/W
	PHP package	28.8	
Thermal resistance, junction-to-case, Θ_{JC}	PFB package	19.6	°C/W
	PHP package	0.79	

† Thermal resistance is modeled data, is not production tested, and is given for informational purposes only.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}		3	3.3	3.6	V
High level digital input, V_{IH}		2	3.3		V
Low level digital input, V_{IL}			0	0.8	V
Load capacitance, C_L			5	15	pF
Clock frequency, f_{CLK}	THS1401	0.1	1	1	MHz
	THS1403	0.1	3	3	MHz
	THS1408	0.1	8	8	MHz
Clock duty cycle	C and I suffix	40%	50%	60%	
	Q and M suffix	45%	50%	55%	
Operating free-air temperature	C suffix	0	25	70	°C
	I suffix	–40	25	85	
	Q suffix	–40	25	125	
	M suffix	–55	25	125	

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 3.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply							
I_{DDA}	Analog supply current		AV_{DD} = 3.6 V		81	90	mA
I_{DDD}	Digital supply current		DV_{DD} = 3.6 V		5	10	mA
	Power		AV_{DD} = DV_{DD} = 3.6 V		270	360	mW
	Power down current				20		μA
DC Characteristics							
	Resolution				14		Bits
DNL	Differential nonlinearity				±0.6	±1	LSB
INL	Integral nonlinearity	THS1401	Best fit		±1.5	±2.5	LSB
		THS1403C/I			±1.5	±2.5	
		THS1403Q			±2	±3	
		THS1408C/I			±3	±5	
		THS1408Q/M			±3.5	±7.5	
	Offset error		IN+ = IN–, PGA = 0 dB			0.3	%FSR
	Gain error	C and I suffix	PGA = 0 dB			1	%FSR
		Q and M suffix				1.75	%FSR
AC Characteristics							
ENOB	Effective number of bits			11.2	11.5		Bits
THD	Total harmonic distortion	THS1401/3/8	f_i = 100 kHz		–81		dB
		THS1403/8	f_i = 1 MHz		–78		
		THS1408	f_i = 4 MHz		–77		
SNR	Signal-to-noise ratio	THS1401/3/8	f_i = 100 kHz		72		dB
		THS1403/8	f_i = 1 MHz	70	72		
		THS1408	f_i = 4 MHz		71		
SINAD	Signal-to-noise ratio + distortion	THS1401/3/8	f_i = 100 kHz		70		dB
		THS1403/8	f_i = 1 MHz	69	70		
		THS1408	f_i = 4 MHz		70		
SFDR	Spurious free dynamic range	THS1401/3/8	f_i = 100 kHz		80		dB
		THS1403C/I, THS1408C/I	f_i = 1 MHz	73	80		
		THS1403Q, THS1408Q/M		71	80		
		THS1408	f_i = 4 MHz		80		
	Analog input bandwidth				140		MHz

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 3.3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Voltage						
	Bandgap voltage, internal mode		1.425	1.5	1.575	V
	Input impedance			40		kΩ
	Positive reference voltage, REF+			2.5		V
	Negative reference voltage, REF–			0.5		V
	Reference difference, ΔREF, REF+ – REF–			2		V
	Accuracy, internal reference			5%		
	Temperature coefficient			40		ppm/°C
	Voltage coefficient			200		ppm/V
Analog Inputs						
	Positive analog input, IN+		0		AV_{DD}	V
	Negative analog input, IN–		0		AV_{DD}	V
	Analog input voltage difference	ΔAin = IN+ – IN–, V_{ref} = REF+ – REF–	$-V_{ref}$		V_{ref}	V
	Input impedance			25		kΩ
	PGA range		0		7	dB
	PGA step size			1		dB
	PGA gain error				±0.25	dB
Digital Inputs						
V_{IH}	High-level digital input		2			V
V_{IL}	Low-level digital input				0.8	V
	Input capacitance			5		pF
	Input current				±1	μA
Digital Outputs						
V_{OH}	High-level digital output	I_{OH} = 50 μA	2.6			V
V_{OL}	Low-level digital output	I_{OL} = 50 μA			0.4	V
I_{OZ}	Output current, high impedance				±10	μA
Clock Timing (CS low)						
f_{CLK}	Clock frequency	THS1401	0.1†	1	1	MHz
		THS1403	0.1†	3	3	MHz
		THS1408	0.1†	8	8	MHz
t_d	Output delay time				25	ns
	Latency			9.5		Cycles

† This parameter is not production tested for Q and M-suffix devices.

PARAMETER MEASUREMENT INFORMATION

sample timing

The THS1401/3/8 core is based on a pipeline architecture with a latency of 9.5 samples. The conversion results appear on the digital output 9.5 clock cycles after the input signal was sampled.

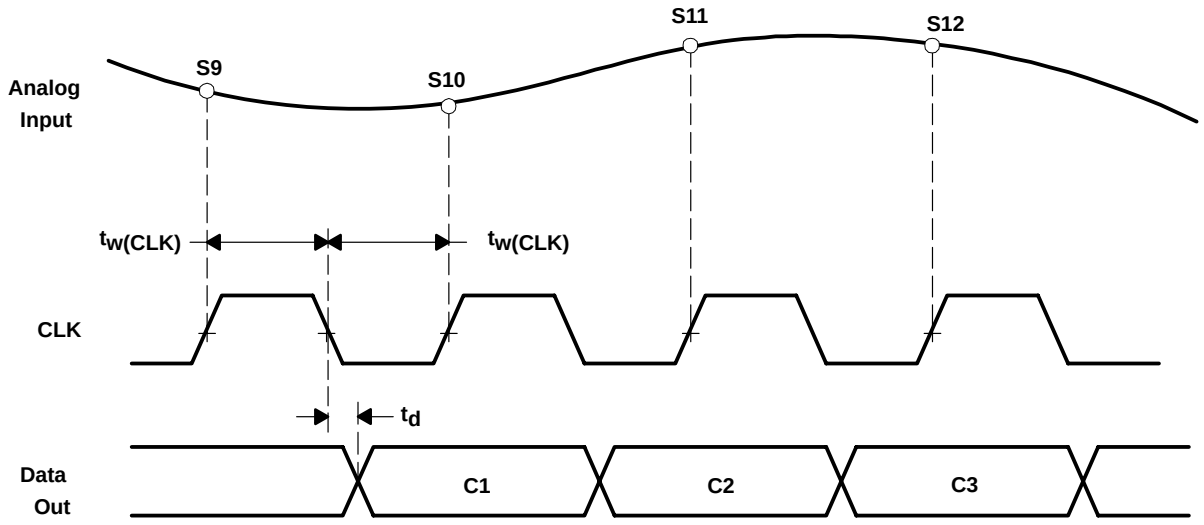


Figure 1. Sample Timing

The parallel interface of the THS1401/3/8 ADC features 3-state buffers, making it possible to directly connect it to a data bus. The output buffers are enabled by driving the OE input low.

Besides the sample results, it is also possible to read back the values of the control register, the PGA register, and the offset register. Which register is read is determined by the address inputs A[1,0]. The ADC results are available at address 0.

The timing of the control signals is described in the following sections.

PARAMETER MEASUREMENT INFORMATION

read timing (15-pF load)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(OE–ACS)}$	Address and chip select setup time	4			ns
t_{en}	Output enable			15	ns
t_{dis}	Output disable		10		ns
$t_{h(A)}$	Address hold time	1			ns
$t_{h(CS)}$	Chip select hold time	0			ns

NOTE: All timing parameters refer to a 50% level.

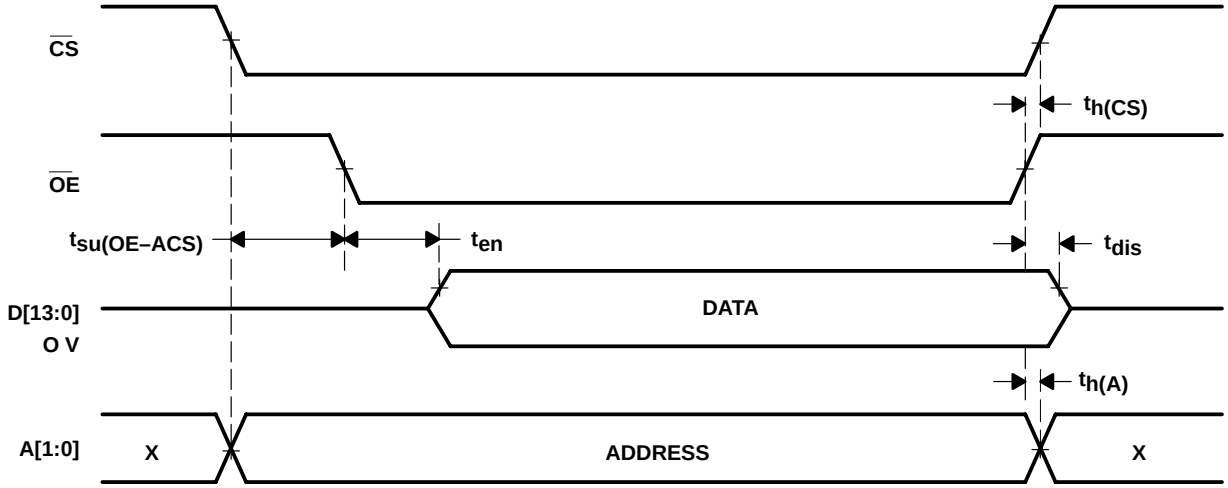


Figure 2. Read Timing

PARAMETER MEASUREMENT INFORMATION

write timing (15-pF load)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(WE–CS)}$	Chip select setup time	4			ns
$t_{su(DA)}$	Data and address setup time	29			ns
$t_{h(DA)}$	Data and address hold time	0			ns
$t_{h(CS)}$	Chip select hold time	0			ns
$t_{wH(WE)}$	Write pulse duration high	15			ns

NOTE: All timing parameters refer to a 50% level.

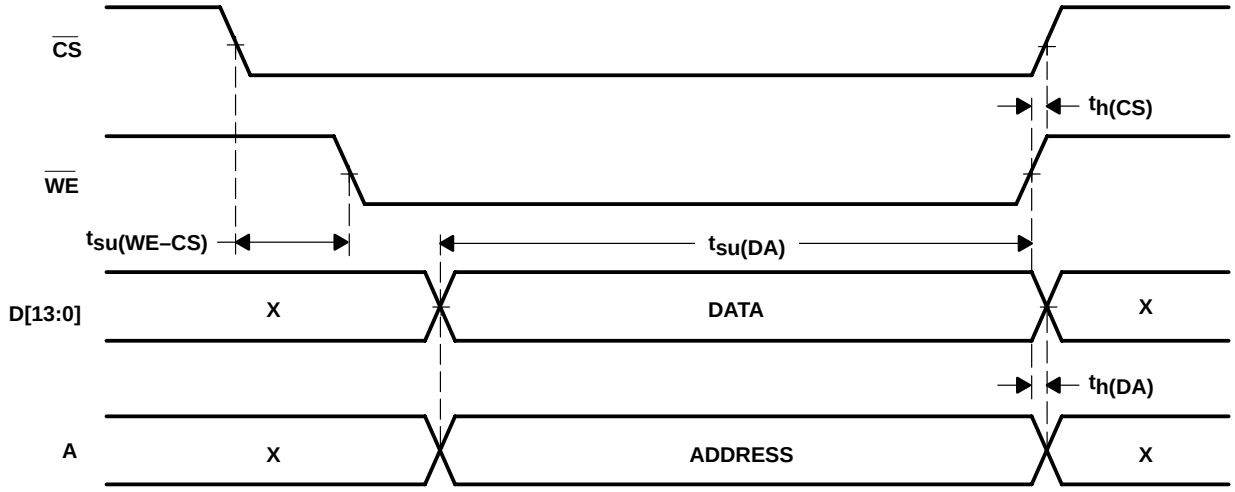


Figure 3. Write Timing

TYPICAL CHARACTERISTICS

POWER vs FREQUENCY

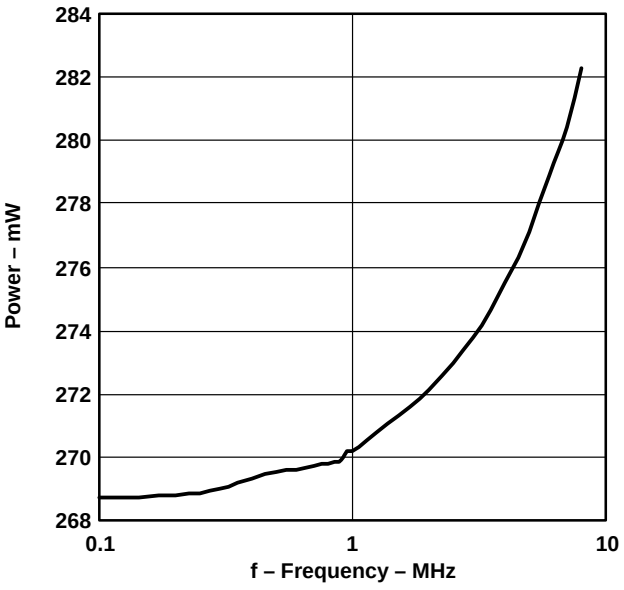


Figure 4

SUPPLY CURRENT vs TIME

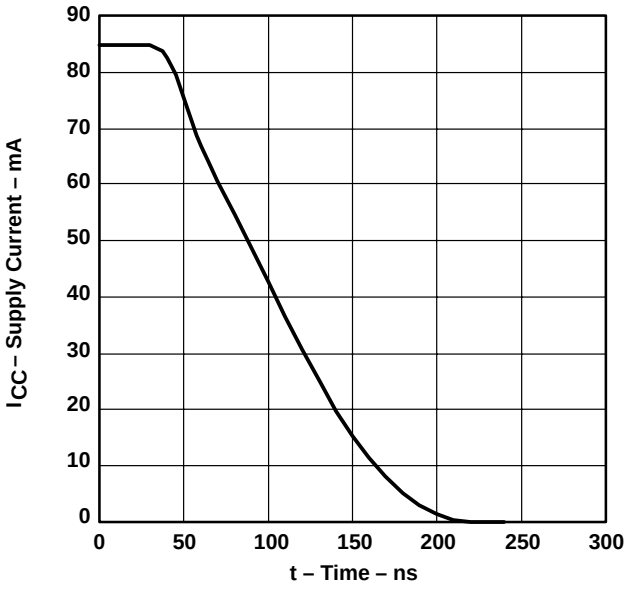


Figure 5

FAST FOURIER TRANSFORM

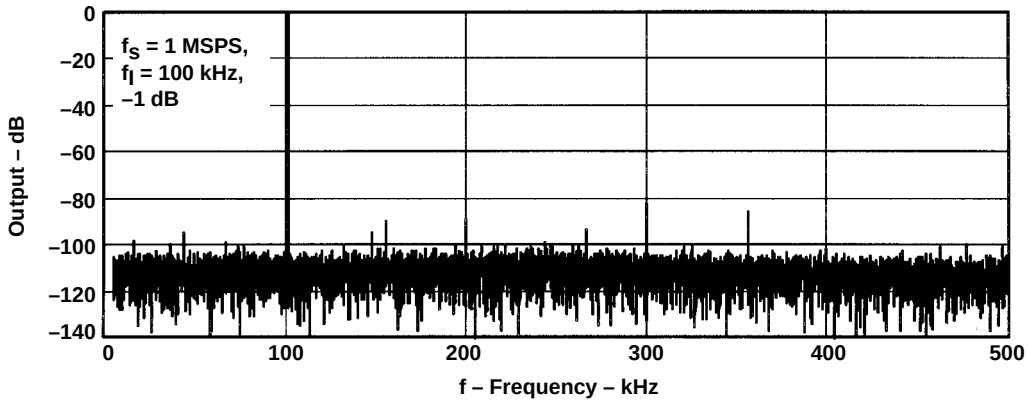


Figure 6

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM

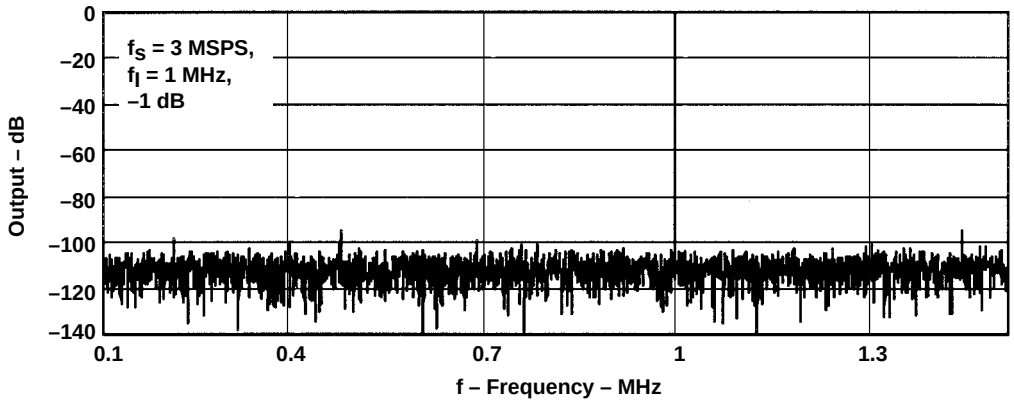


Figure 7

FAST FOURIER TRANSFORM

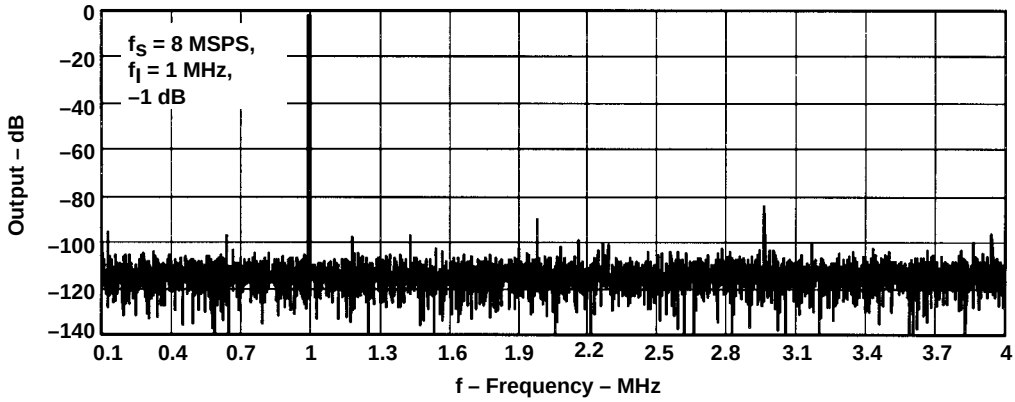


Figure 8

INTEGRAL NONLINEARITY

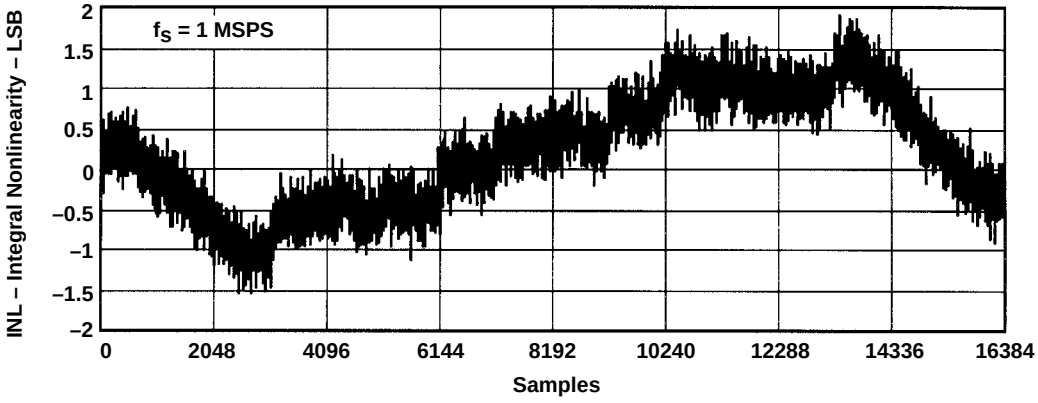


Figure 9

TYPICAL CHARACTERISTICS

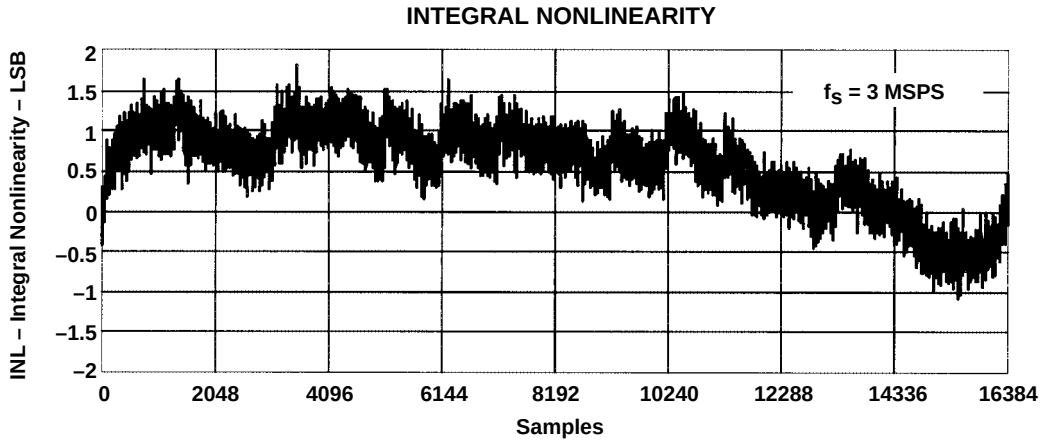


Figure 10

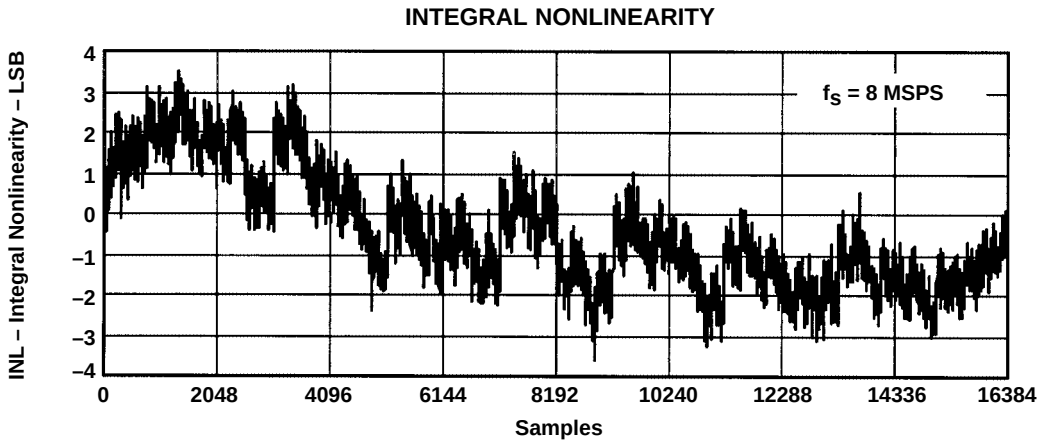


Figure 11

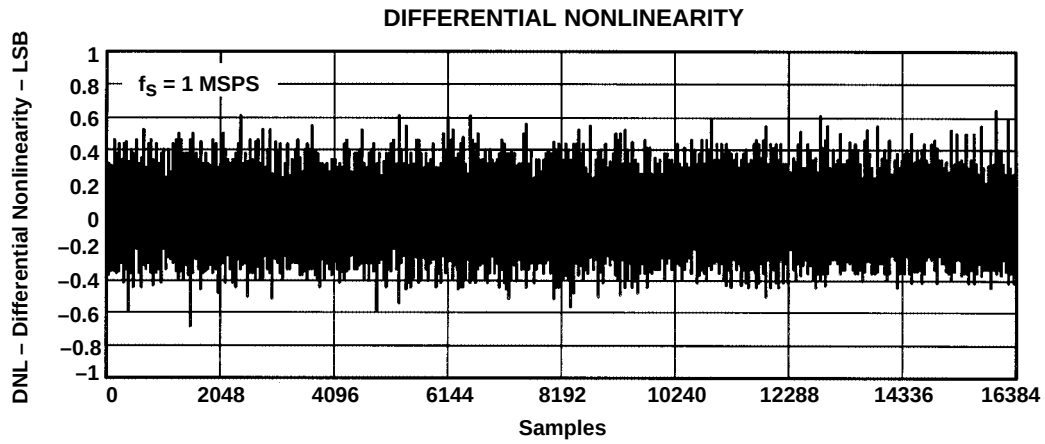


Figure 12

TYPICAL CHARACTERISTICS

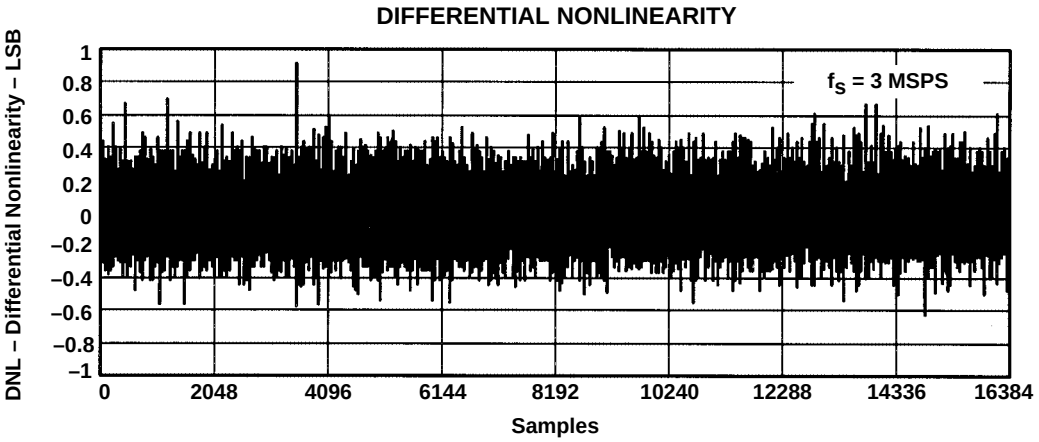


Figure 13

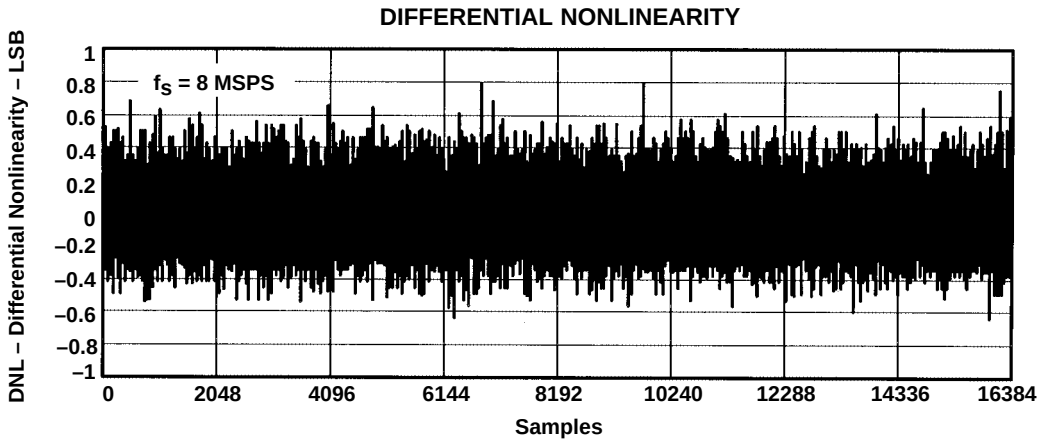


Figure 14

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

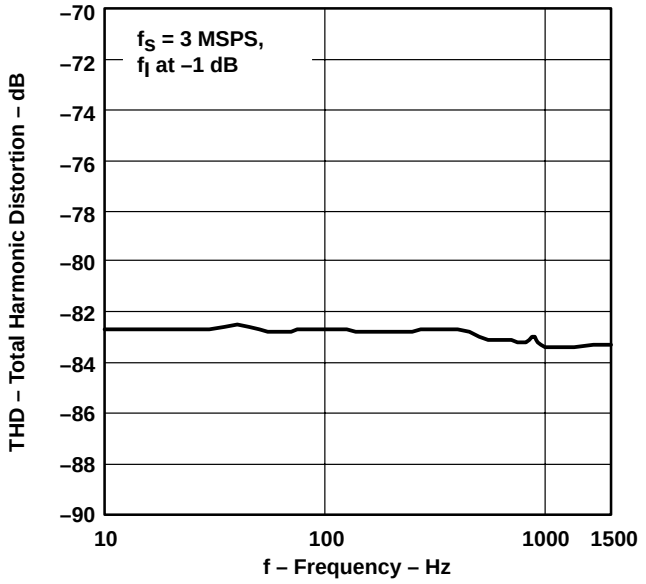


Figure 15

TOTAL HARMONIC DISTORTION vs FREQUENCY

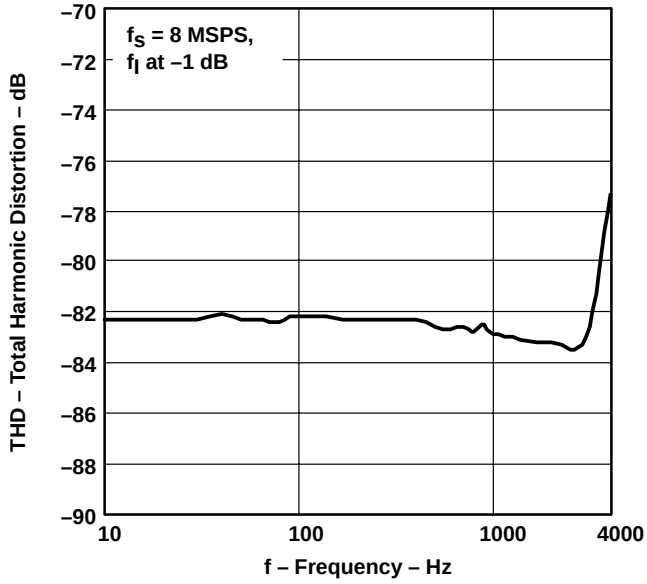


Figure 16

SIGNAL-TO-NOISE RATIO vs FREQUENCY

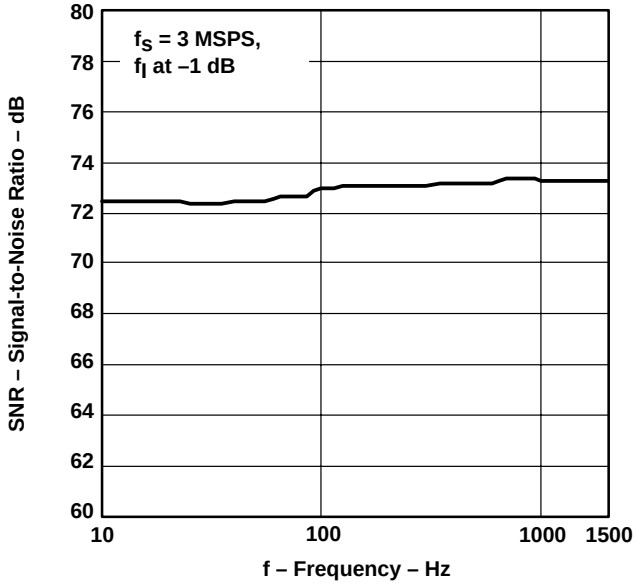


Figure 17

SIGNAL-TO-NOISE RATIO vs FREQUENCY

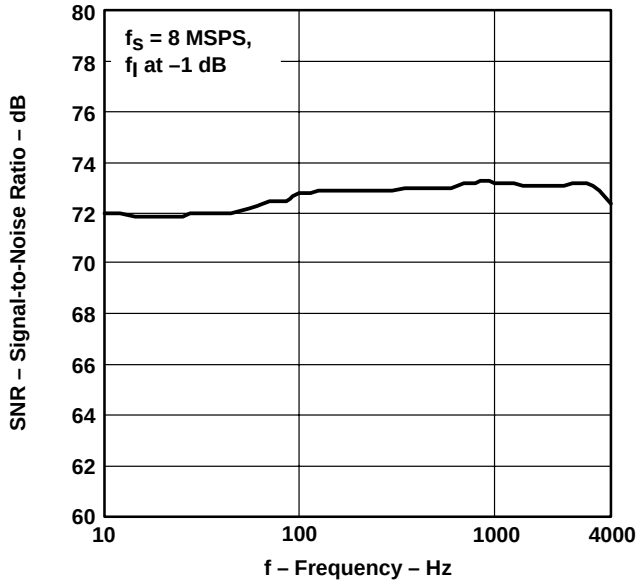


Figure 18

PRINCIPLES OF OPERATION

registers

The device contains several registers. The A register is selected by the values of bits A1 and A0:

A1	A0	Register
0	0	Conversion result
0	1	PGA
1	0	Offset
1	1	Control

Tables 1 and 2 describe how to read the conversion results and how to configure the data converter. The default values (were applicable) show the state after a power-on reset.

Table 1. Conversion Result Register, Address 0, Read

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	MSB	...	…	…	…	…	…	…	…	…	…	…	…	LSB

The output can be configured for 2s complement or straight binary format (see D11/control register).

The output code is given by:

2s complement:		Straight binary:	
–8192	at ΔIN = –ΔREF	0	at ΔIN = –ΔREF
0	at ΔIN = 0	8192	at ΔIN = 0
8191	ΔIN = –ΔREF – 1 LSB	16383	at ΔIN = –ΔREF – 1 LSB

$$1\ \text{LSB} = \frac{2\Delta\text{REF}}{16384}$$

Table 2. PGA Gain Register, Address 1, Read/Write

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	X	X	X	X	G2	G1	G0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PGA gain is determined by writing to G2–0.

Gain (dB) = 1dB × G2–0. max = 7dB. The range of G2–0 is 0 to 7.

Table 3. Offset Register, Address 2, Read/Write

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	MSB	…	…	…	…	…	…	LSB
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The offset correction range is from –128 to 127 LSB. This value is added to the conversion results from the ADC.

PRINCIPLES OF OPERATION

Table 4. Control Register, Address 3, Read

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF	RES	RES	RES	RES	RES	RES	RES

Table 5. Control Register, Address 3, Write

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWD:	Power down	0 = normal operation	1 = power down
REF:	Reference select	0 = internal reference	1 = external reference
FOR:	Output format	0 = straight binary	1 = 2s complement
TM2–0:	Test mode	000 = normal operation	
		001 = both inputs = REF–	
		010 = IN+ at $V_{ref}/2$, IN– at REF–	
		011 = IN+ at REF+, IN– at REF–	
		100 = normal operation	
		101 = both inputs = REF+	
		110 = IN+ at REF–, IN– at $V_{ref}/2$	
		111 = IN+ at REF–, IN– at REF+	
OF:	Offset correction	0 = enable	1 = disable
RES	Reserved	Must be set to 0.	

APPLICATION INFORMATION

driving the analog input

The THS1401/3/8 ADCs have a fully differential input. A differential input is advantageous with respect to SNR, SFDR, and THD performance because the signal peak-to-peak level is 50% of a comparable single-ended input.

There are three basic input configurations:

- Fully differential
- Transformer coupled single-ended to differential
- Single-ended

fully differential configuration

In this configuration, the ADC converts the difference (ΔIN) of the two input signals on IN+ and IN–.

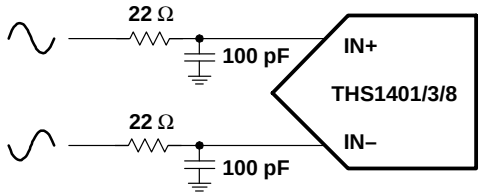


Figure 19. Differential Input

The resistors and capacitors on the inputs decouple the driving source output from the ADC input and also serve as first order low pass filters to attenuate out of band noise.

The input range on both inputs is 0 V to AV_{DD}. The full-scale value is determined by the voltage reference. The positive full-scale output is reached, if ΔIN equals ΔREF, the negative full-scale output is reached, if ΔIN equals –ΔREF.

ΔIN [V]	OUTPUT
–ΔREF	– full scale
0	0
ΔREF	+ full scale

APPLICATION INFORMATION

transformer coupled single-ended to differential configuration

If the application requires the best SNR, SFDR, and THD performance, the input should be transformer coupled.

The signal amplitude on both inputs of the ADC is one half as high as in a single-ended configuration thus increasing the ADC ac performance.

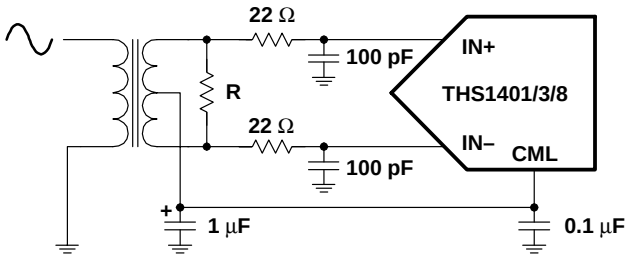


Figure 20. Transformer Coupled

The following table shows the input voltages for negative full-scale output, zero output, and positive full-scale output:

IN [V_{PEAK}]	OUTPUT [$_{PEAK}$]
–ΔREF	– full scale†
0	0
ΔREF	+ full scale†

† n = 1 (winding ratio)

The resistor R of the transformer coupled input configuration must be set to match the signal source impedance $R = n^2 Rs$, where Rs is the source impedance and n is the transformer winding ratio.

APPLICATION INFORMATION

single-ended configuration

In this configuration, the input signal is level shifted by ΔREF/2.

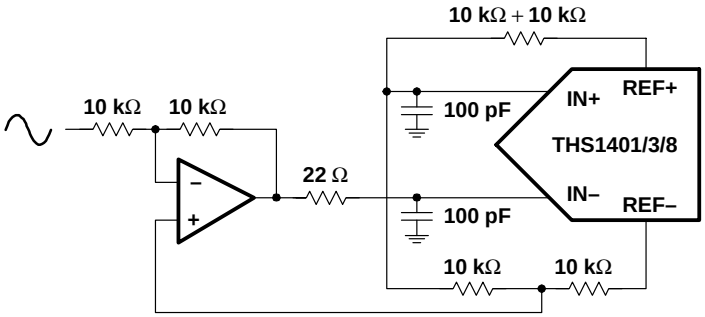


Figure 21. Single-Ended With Level Shift

The following table shows the input voltages for negative full-scale output, zero output, and positive full-scale output:

ΔIN+ [V]	OUTPUT
–ΔREF	– full scale
0	0
ΔREF	+ full scale

Note that the resistors of the op-amp and the op-amp all introduce gain and offset errors. Those errors can be trimmed by varying the values of the resistors.

Because of the added offset, the op-amp does not necessarily operate in the best region of its transfer curve (best linearity around zero) and therefore may introduce unacceptable distortion. For ac signals, an alternative is described in the following section.

APPLICATION INFORMATION

AC-coupled single-ended configuration

If the application does not require the signal bandwidth to include dc, the level shift shown in Figure 21 is not necessary.

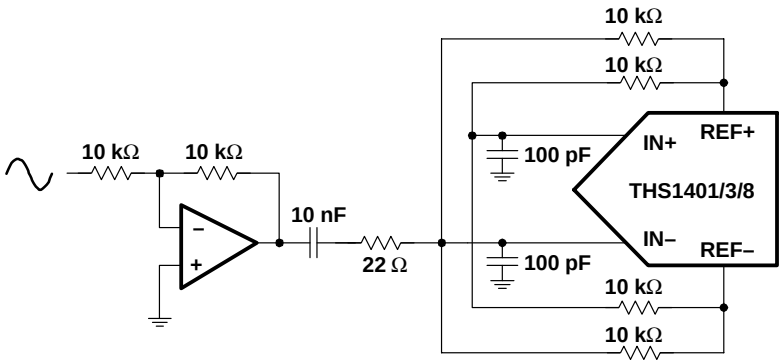


Figure 22. Single-Ended With Level Shift

Because the signal swing on the op-amp is centered around ground, it is more likely that the signal stays within the linear region of the op-amp transfer function, thus increasing the overall ac performance.

IN [V_{PEAK}]	OUTPUT [$_{PEAK}$]
–ΔREF	– full scale
0	0
ΔREF	+ full scale

Compared to the transformer-coupled configuration, the swing on IN– is twice as big, which can decrease the ac performance (SNR, SFD, and THD).

APPLICATION INFORMATION

internal/external reference operation

The THS1401/3/8 ADC can either be operated using the built-in band gap reference or using an external precision reference in case very high dc accuracy is needed.

The REF+ and REF+ outputs are given by:

$$\text{REF} + = \text{VBG}\left(1 + \frac{2}{3}\right) \text{ and } \text{REF}- = \text{VBG}\left(1 - \frac{2}{3}\right)$$

If the built-in reference is used, VBG equals 1.5 V which results in REF+ = 2.5 V, REF– = 0.5 V and ΔREF = 2 V.

The internal reference can be disabled by writing 1 to D12 (REF) in the control register (address 3). The band gap reference is then disconnected and can be substituted by a voltage on the VBG pin.

programmable gain amplifier

The on-chip programmable gain amplifier (PGA) has eight gain settings. The gain can be changed by writing to the PGA gain register (address 1). The range is 0 to 7dB in steps of one dB.

out of range indication

The OV output of the ADC indicates an out of range condition. Every time the difference on the analog inputs exceeds the differential reference, this signal is asserted. This signal is updated the same way as the digital data outputs and therefore subject to the same pipeline delay.

offset compensation

With the offset register it is possible to automatically compensate system offset errors, including errors caused by additional signal conditioning circuitry. If the offset compensation is enabled (D7 (OFF) in the control register), the value in the offset register (address 2) is automatically added to the output of the ADC.

In order to set the correct value of the offset compensation register, the ADC result when the input signal is 0 must be read by the host processor and written to the offset register (address 2).

test modes

The ADC core operation can be tested by selecting one of the available test modes (see control register description). The test modes apply various voltages to the differential input depending on the setting in the control register.

digital I/O

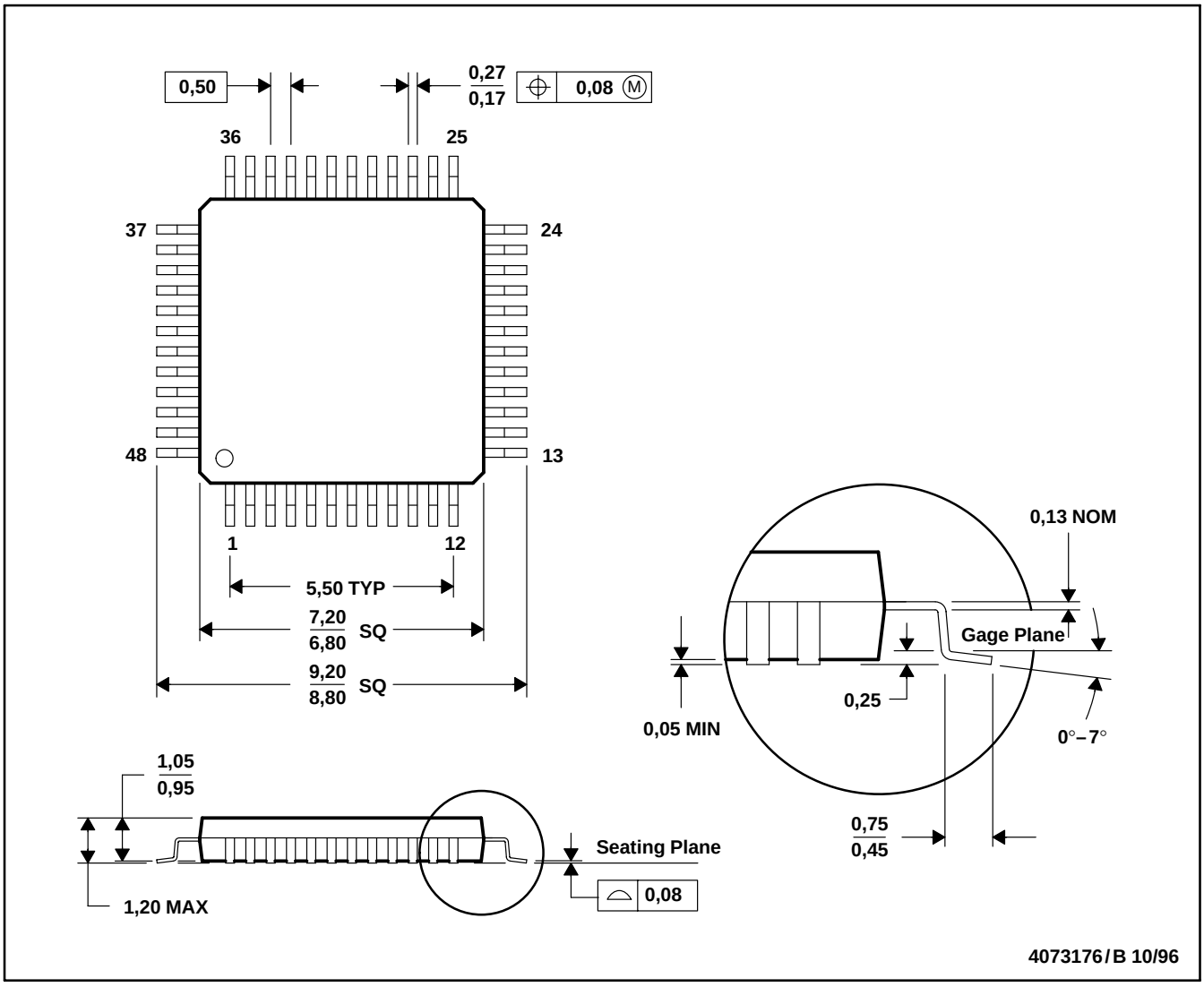
The digital inputs and outputs of the THS1401/3/8 ADC are 3-V CMOS compatible. In order to avoid current feed back errors, the capacitive load on the digital outputs should be as low as possible (50 pF max). Series resistors (100 Ω) on the digital outputs can improve the performance by limiting the current during output transitions.

The parallel interface of the THS1401/3/8 ADC features 3-state buffers, making it possible to directly connect it to a data bus. The output buffers are enabled by driving the $\overline{\text{OE}}$ input low.

Refer to the read and write timing diagrams in the parameter measurement information section for information on read and write access.

MECHANICAL DATA

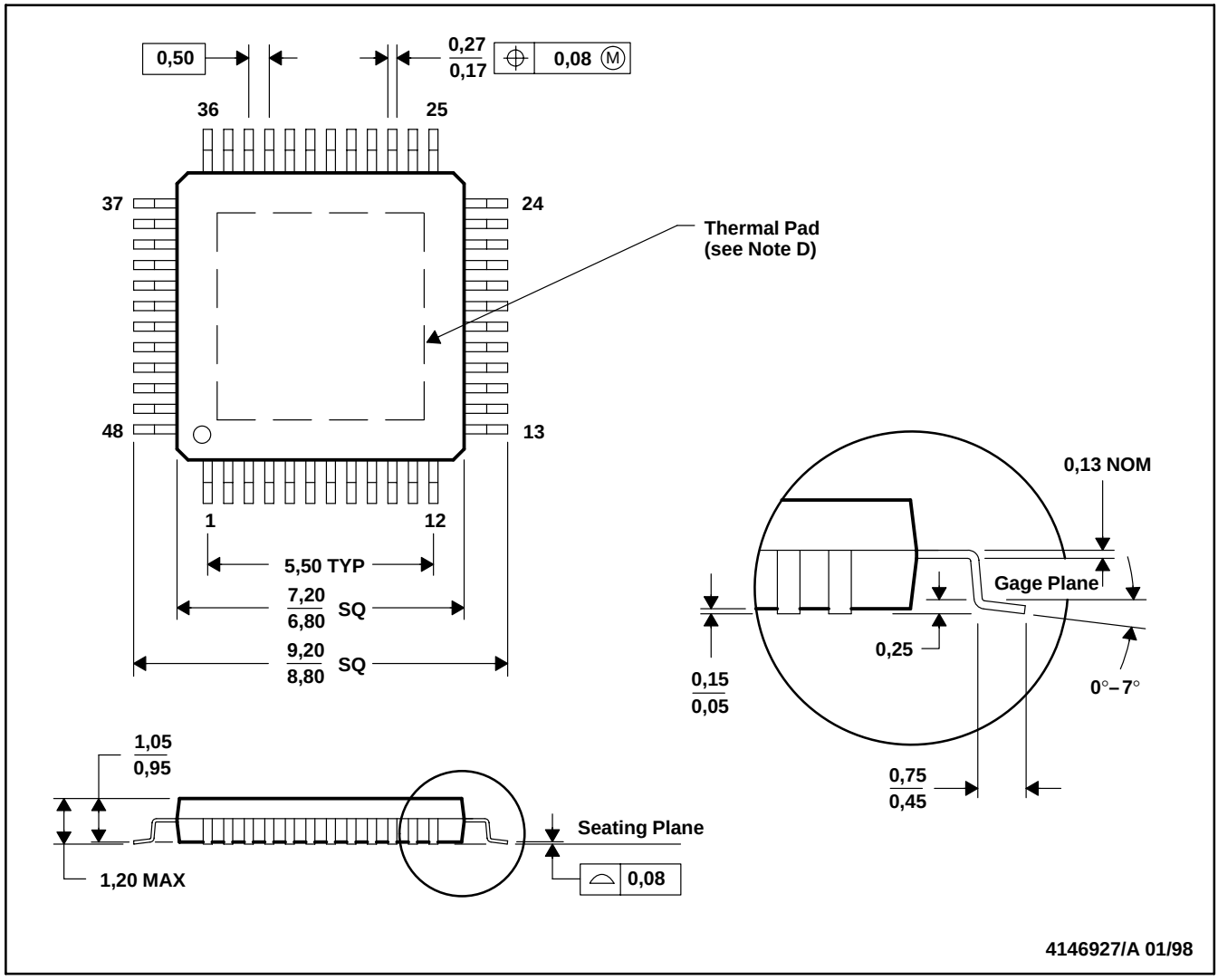
PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MECHANICAL DATA

PHP (S-PQFP-G48) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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