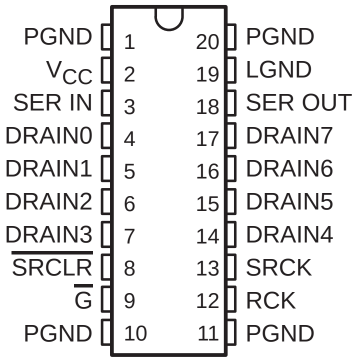
TPIC6596
POWER LOGIC 8-BIT SHIFT REGISTER

SLIS096 – APRIL 2000

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typ**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Enhanced Cascading for Multiple Stages**
- **All Registers Cleared With Single Input**
- **Low Power Consumption**

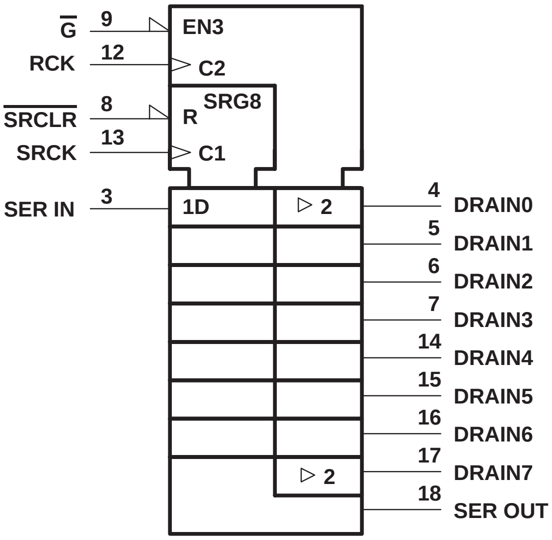
DW OR N PACKAGE
(TOP VIEW)



description

The TPIC6596 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

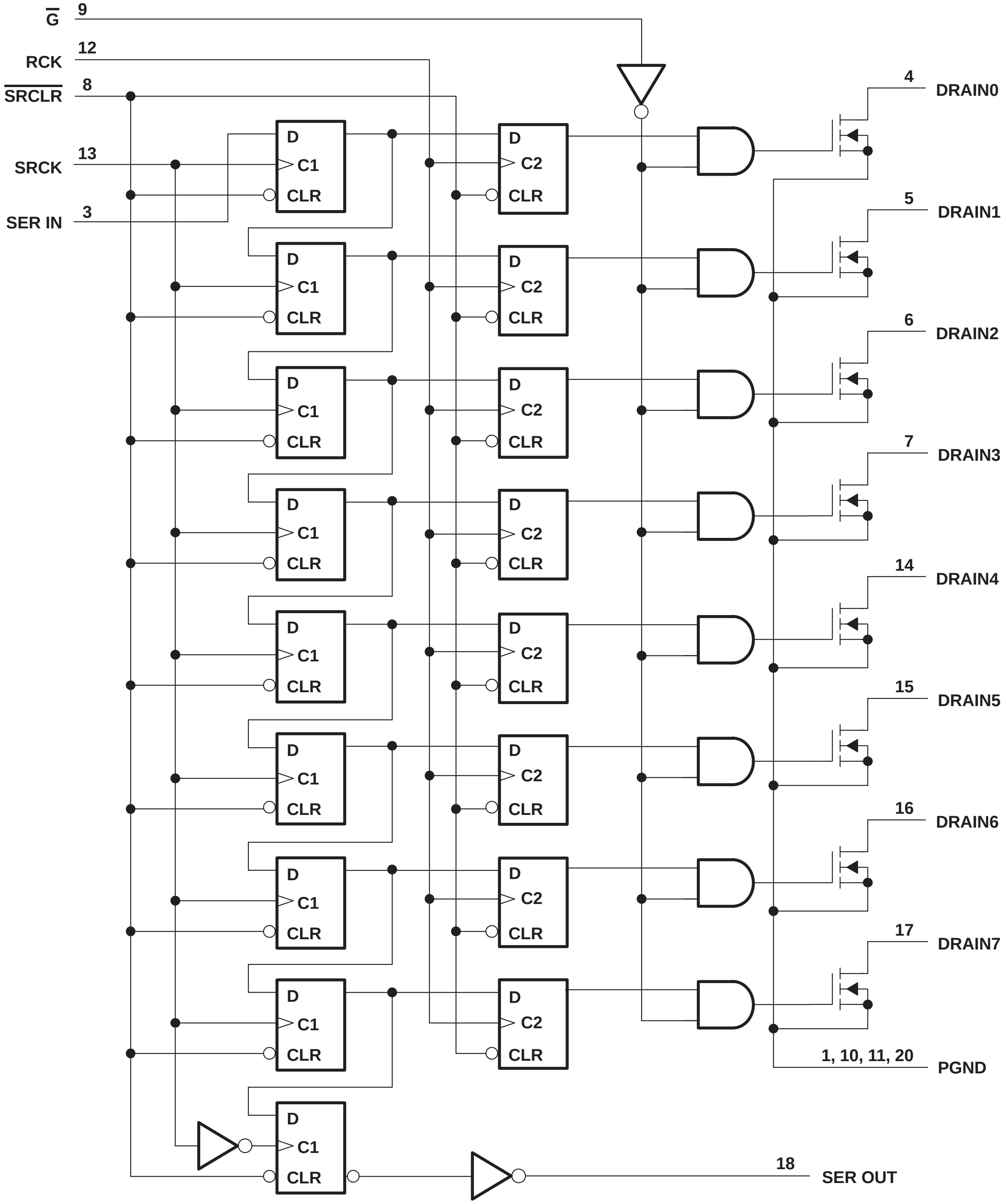
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. When $\overline{\text{SRCLR}}$ is low, all registers in the device are cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

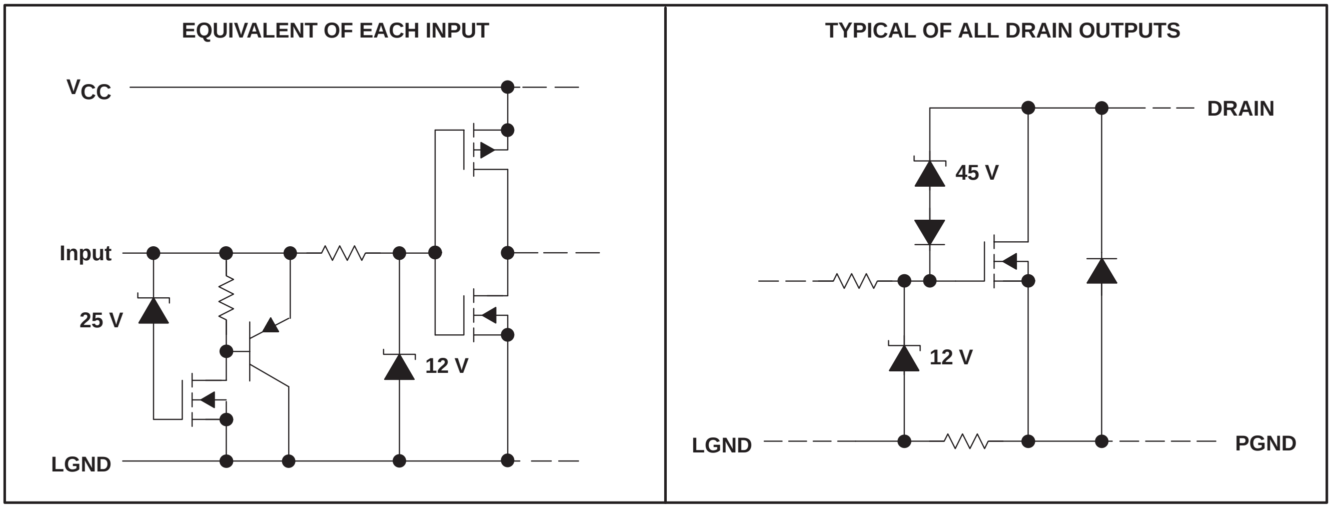
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6596 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)[†]

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	1.5	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	–40	125	°C

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J – T_C$ to 10°C maximum.

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 mA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = –4 mA, V_{CC} = 4.5 V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 mA, V_{CC} = 4.5 V			0.002	0.1	V
		I_{OH} = 4 mA, V_{CC} = 4.5 V			0.2	0.4	
$V_{(hys)}$	Input hysteresis	V_{DS} = 15 V			1.3		V
I_{IH}	High-level input current	V_{CC} = 5.5 V, $V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				–1	µA
I_{CCL}	Logic supply current	I_O = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, See Figures 1, 2, and 6			0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J – T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 11		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			200		ns
t_r	Rise time, drain output			230		ns
t_f	Fall time, drain output			170		ns
t_{pd}	Propagation delay time, SRCK↓ to SER OUT	C_L = 30 pF, I_D = 250 mA, See Figure 2		50		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 250 mA, See Note 8			5	MHz
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/μs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.

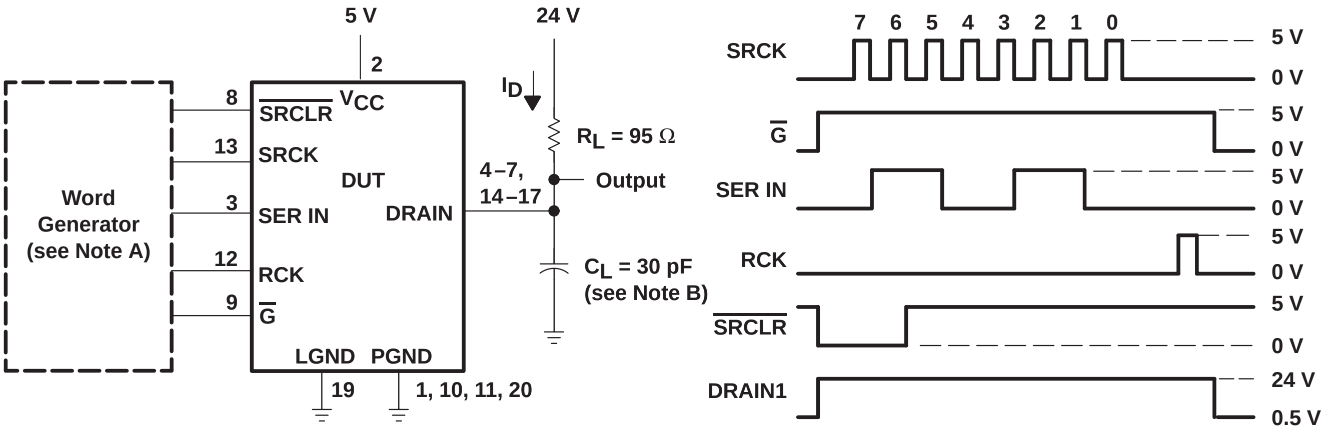
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows SRCK → SER OUT propagation delay and setup time plus some timing margin.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

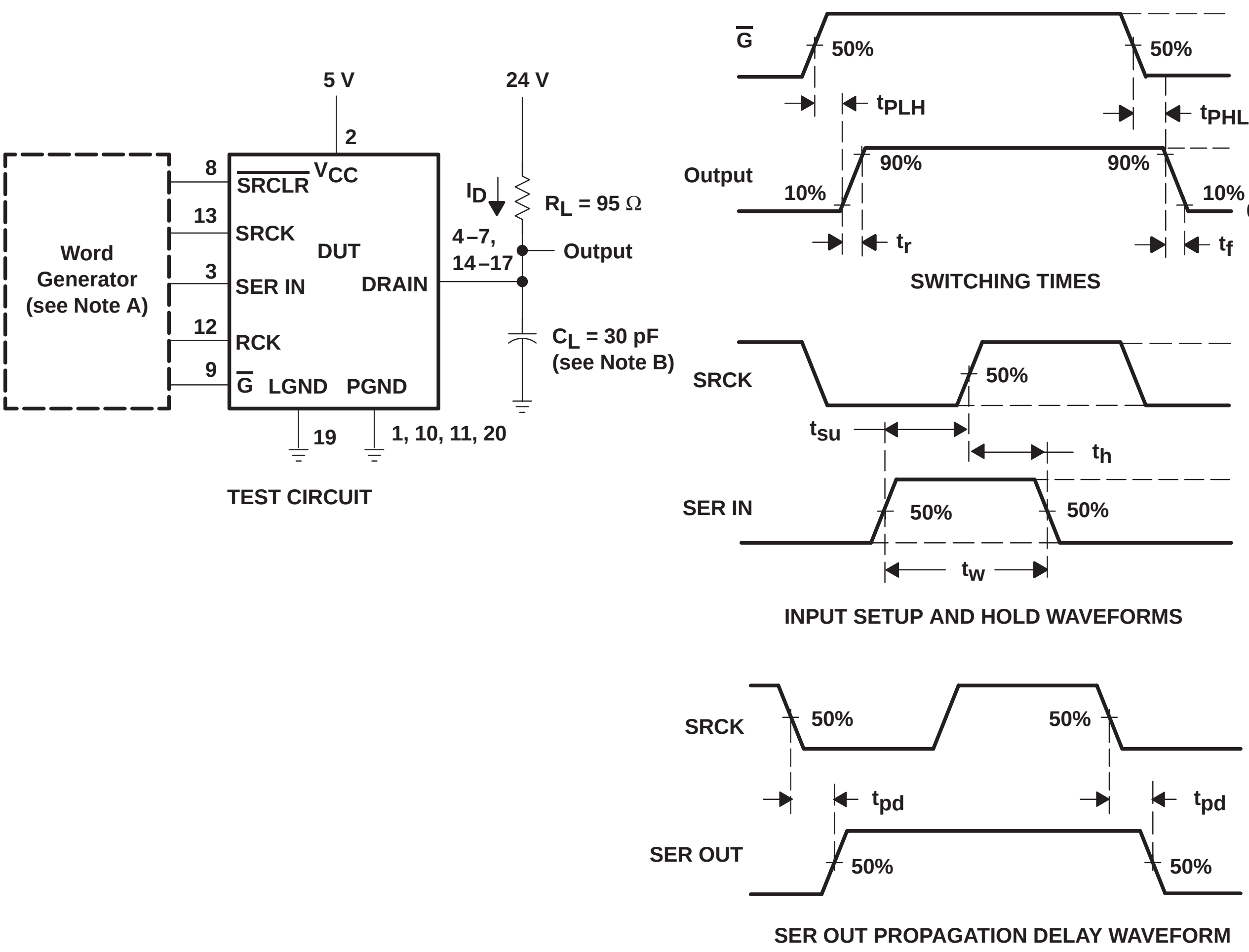


TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 1. Resistive Load Operation

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

SWITCHING TIMES

INPUT SETUP AND HOLD WAVEFORMS

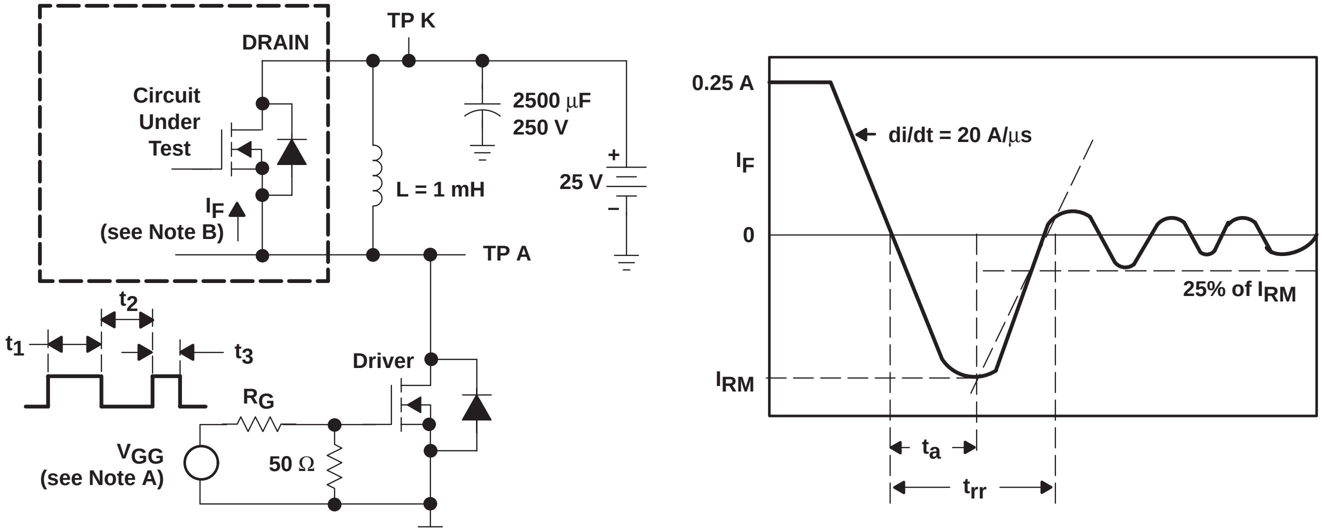
SER OUT PROPAGATION DELAY WAVEFORM

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



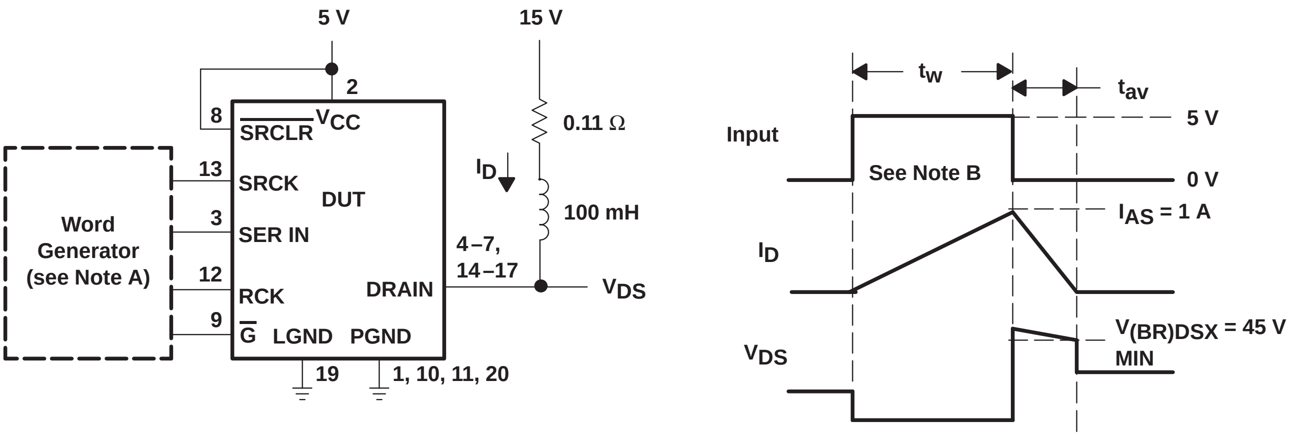
TEST CIRCUIT

CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

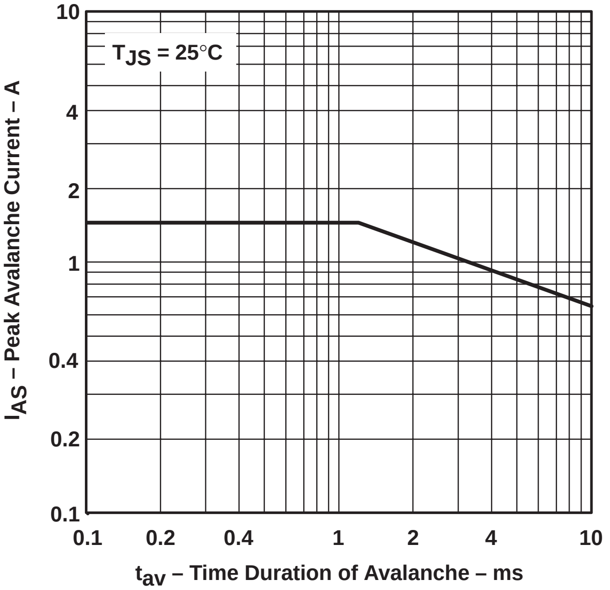


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

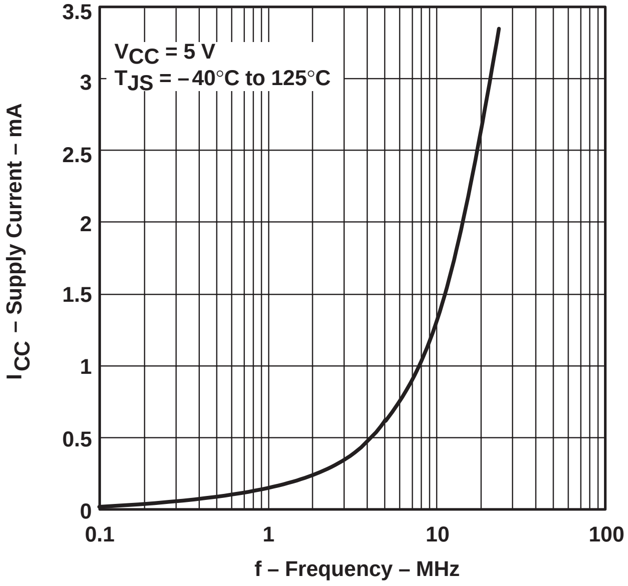


Figure 6

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

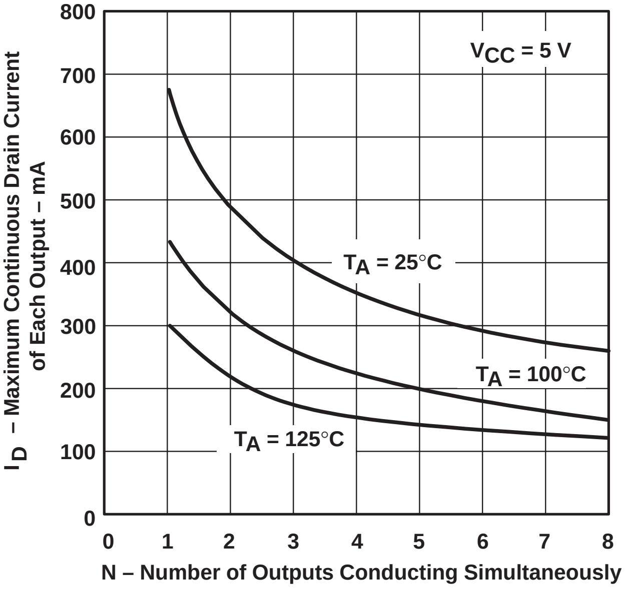


Figure 7

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

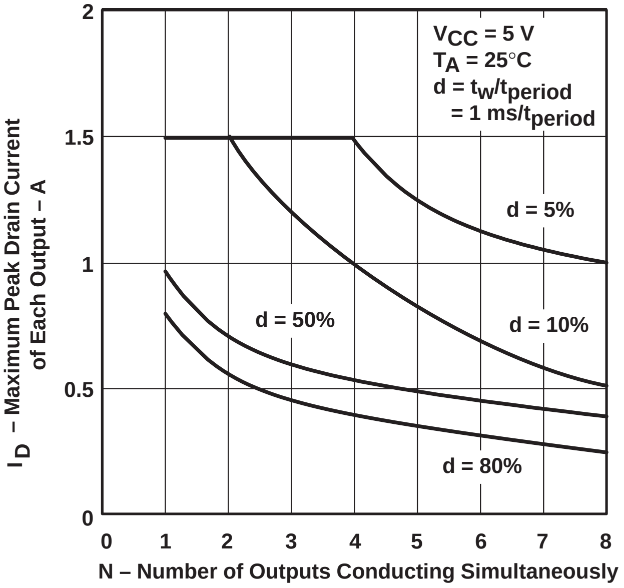


Figure 8

TYPICAL CHARACTERISTICS

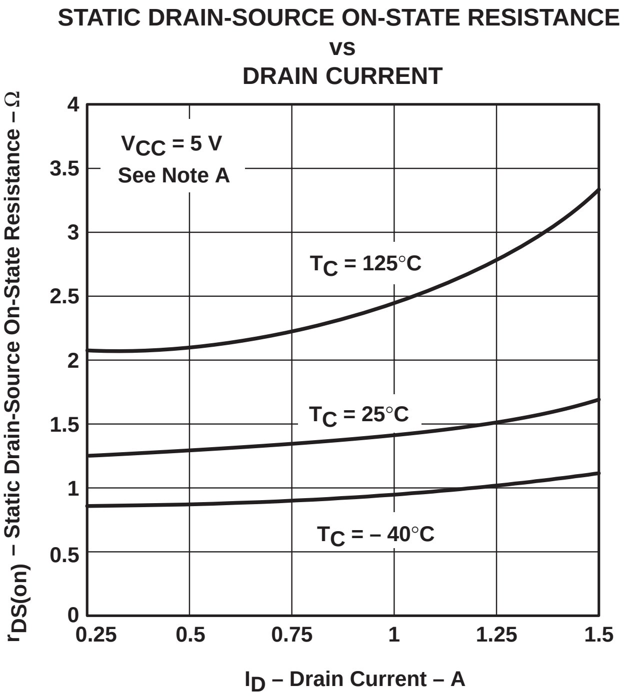


Figure 9

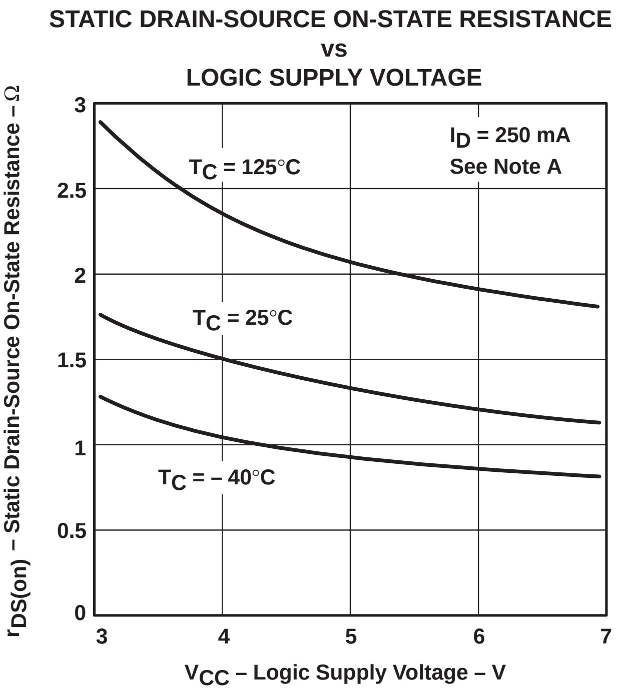


Figure 10

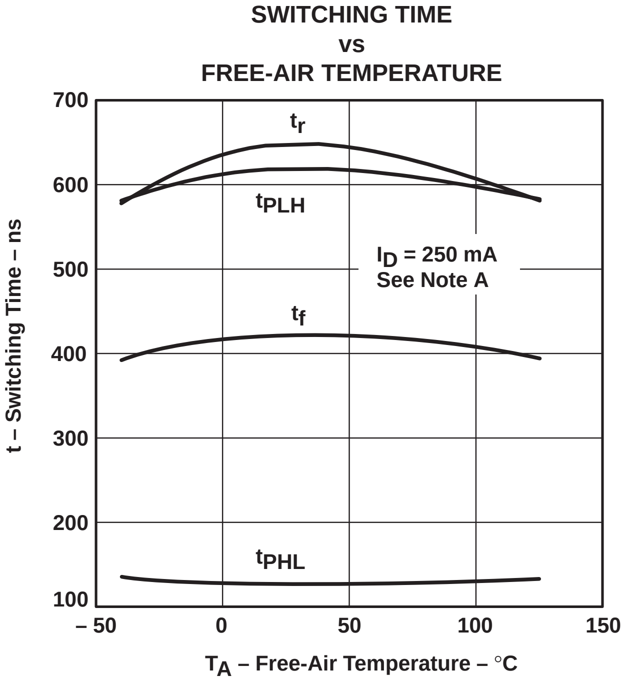


Figure 11

NOTE A: Technique should limit T_J – T_C to 10°C maximum.

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