TOSHIBA

System ASIC
TC200 Series CMOS ASICs

0.4µ 3.0/3.3V ASIC Family

The TC200 series is a family of 0.4µm, 3.0/3.3V ASICs. They are the first of a new generation of deep sub-micron "System ASIC" products with highly accurate delay models, area efficient memory cells and a very fine pitch TAB bonding capability for high I/O requirements. The family consists of Gate Array (TC200G), Embedded Array (TC200E) and Standard Cell (TC200C) ASIC products. The TC200E is a gate array based product that incorporates the ability to embed large diffused cell based hardmacro-cells and compilable cells (RAM, ROM, DAC, multipliers, PLLs, etc) rather than building metalized functions. This enables denser, faster, higher performance ASICS to be designed while still exhibiting quick "gate array" type turn around times.

Benefits

- Advanced 0.4µ micron CMOS process with fast 190ps (TC200G/E, 170ps TC200C) gate delays.
- New highly accurate delay model with non-linear dependency on slew rate, load and logic state.
- 1.27 µW/gate/MHz core power consumption.
- 707,000 equivelent gates (TC200G, 730,000 TC200C) provide high levels of integration for improved performance and board area savings.
- New RAM cell archetecture allows additional savings in area and provides higher performance than previous ASIC generations.
- Extensive libraries with a wide range of macrocells, compilable cells and megacells availible.
- Design Kit support for a wide range of EDA environments.
- VERILOG-XL sign off capability.
- Library compatibility with Toshiba's gate array families of previous generation ASICs for ease of migration of designs.
- 62µ TAB pad pitch allows higher number of I/O per gate than previous product generations.
- A wide range of packages are availible, including heat spreader plastic QFP, TABFP, BGA, tape BGA, and others.

System ASIC

The TC200 family of System ASICS offer you Toshiba's high quality and high capacity manufacturing expertise. A partnership with Toshiba brings you not only the performance of this family, but also comprehensive design support, an Open EDA Strategy, fast (3 day for gate array) prototype turnaround time, steep production ramp-up and proven high volume manufacturing capacity.

System Performance

Implementing a design using the TC200 increases system performance in two ways:

1. Improved circuit performance due to fast 170ps (Standard Cell) or 190ps (Gate array/embedded array) gate delays. Critical path performance improves by more than 15% compared to an identcally implemented .5µ TC180 device. This improvement allows designs to operate at a high clock rate with more safety margins.
2. The ability to implement larger portions of an entire system design on a single ASIC, thus minimizing the amount of chip to chip communication (reducing capacitive loading, improving switching performanceand reducing power consumption).

Features

TC200G	TC200E/C
– 12K - 707K usable gates	up to 730K
– 14 standard master sizes	21 standard master sizes
– up to 512 wire bonds	Same
– up to 776 TAB bond pads	Same
– 300+ primitive cells (scan, standard, high drive cells)	Same
– 450+ I/O cells hign drive (24mA), slew rate control and high speed output buffers	Same
Compiled cells – sync/async,	Same
– single, dual port RAM, ROM	
– Special I/O include:	
PCI, GTL, 3V fail safe I/Os	Same
5V tolerant inputs	Same
5V open drain outputs	Same
PLLs	Same

Reduced Power Vonsumption and Packaging Costs

The TC200 family was designed and optomized for 3.0/3.3V core operation. It is a true 3V product based on a 3V process technology. The reduction in power is nearly 15% in the core as compared to that of the 0.5µ technology TC180. Alternatively, for the same power much higher integration can be acheived with the TC200 as compared to earlier products. Power consumption savings are of a greater magnitude when compared to 5V devices and are enough to justify a design move to eliminate the need for expensive ceramic packaging.

TC200G Gate Array Product Summary

Reference	Available Gates (k)	Equivalent Gates (k)		Wirebond Pads	TAB Pad Options	
		DLM*	TLM*	125µ Pitch	62µ Pitch	83µ Pitch
TC200G/E42/92	1154	404	707	512	—	776
TC200G/E40/90	824	288	505	432	—	656
TC200G/E36/86	652	228	400	384	—	584
TC200G/E32/82	501	175	307	336	—	512
TC200G/E24/74	330	125	219	272	—	416
TC200G/E20/70	257	98	171	240	—	368
TC200G/E16/66	194	82	143	208	428	320
TC200G/E14/64	160	67	117	192	388	288
TC200G/E12/62	134	56	99	176	356	264
TC200G/E10/60	111	47	81	160	324	240
TC200G/E08/58	92	39	68	144	296	220
TC200G/E06/56	68	31	54	128	256	192
TC200G/E04/54	45	22	38	104	208	156
TC200G/E02/52	26	12	22	80	160	120

* Double Layer Metal / Triple Layer Metal

TC200E/C Embedded Array and Standard Cell Product Summary

Reference	Equivalent Gates		I/O Pads		
	DLM*	TLM*	Wirebond Pads	TAB 62µm	TAB 83µm
TC200C02	12,000	-	80	152	112
TC200C04	21,000	-	104	200	148
TC200C06	32,500	-	128	248	186
TC200C08/58	40,900	66,450	144	288	212
TC200C10/60	49,300	80,200	160	316	236
TC200C12/62	59,950	97,450	176	348	260
TC200C14/64	71,600	116,350	192	380	284
TC200C16/66	81,050	131,450	208	420	312
TC200C18/68	94,000	152,400	224	—	336
TC200C20/70	107,850	174,900	240	—	360
TC200C22/72	122,700	198,950	256	—	384
TC200C24/74	138,500	224,600	272	—	408
TC200C26/76	155,250	251,750	288	—	432
TC200C28/78	172,950	280,450	304	—	456
TC200C30/80	181,250	295,200	320	—	480
TC200C32/82	199,800	325,400	336	—	504
TC200C34/84	229,350	373,500	360	—	540
TC200C36/86	260,900	424,950	384	—	576
TC200C38/88	294,500	479,650	408	—	612
TC200C40/90	330,150	537,700	432	—	648
TC200C42/92	437,150	728,550	512	—	768

* Double Layer Metal / Triple Layer Metal

Power Dissipation

at 3.3V	**Power = 1.27µW/gate/MHz**

NOTE 1: These typical numbers are for estimation purposes only. Power dissapation is dependent on wire loading and gate switching rates.

Clock Distribution Network

Toshiba implements clock distribution networks in ASIC designs using a variety of different topologies including loop, grid, tree or trunk. The actual topology used depends on the desired clock skew specification and other design criteria such as power consumption limits and availible gates. Typical on-chip skew delays will be less than 0.5ns. Toshiba plans to offer tighter links between logical and physical; design processes, i.e. synthesis, floor planning and layout, which will further enable designers to optimize their designs.

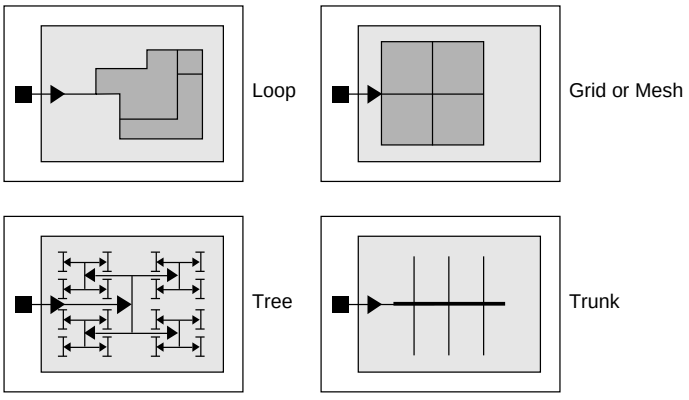


Figure 1. Clock Delay and Skew Control Layout Topologies

Open EDA Strategy

Toshiba's EDA strategy is to support commercial EDA tools - Simulator sign off, Floorplanning and DFT solutions which will give the designer the ability to complete their designs effectively. Toshiba works in an ongoing process of establishing partnerships with key EDA vendors—Synopsys, Cadence, Viewlogic, Mentor, Compass—to ensure compatibility between our processes and products with theirs. The strategy provides for a focus on deep sub-micron (0.5µm and below) technology solutions, and to develop future design methodologies based on customer requirements, as well as supporting an array of industry standard formats—SDF, PDFF etc.

Sign-off Verilog-XL and Other Simulators

ASIC designers can take advantage of the sign-off capabiliy offered by Toshiba for the TC200 family. Sign-off is supported from Version 2.1 of Verilog-XL. SUN wokstations running SunOS 4.1 are supported. The Verilog-XL sign-off libraries use the new highly accurate delay model and are supported by new tools, utilities and interfaces to improve the efficiency of the design flow. Support for other simulators will be provided in future releases of TC200 design kits.

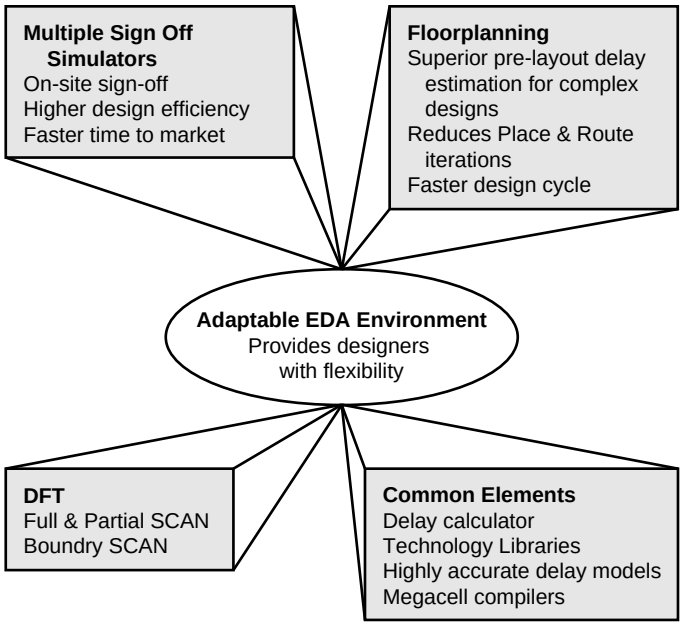


Figure 2. Flexible ASIC Design Support

DFT Support

Toshiba provides users considerable flexibility on the choice of DFT for their design. Both full and partial scan methodologies are supported through the use of commercial tools such as Sunrise and Synopsys Test Compilers for scan synthesis and ATPG. Toshiba's design kits include utilities and tools to accomplish boundry scan. A range of different IEEE 1149.1 JTAG compliant controllers and Boundry Scan Registers are offered. Toshiba also plans to offer automated SRAM BIST compiler supporting multiple memory blocks.

Accurate Models

TC200 ASIC devices incorporate Toshiba's new highly accurate delay model wich includes the following features:

– Pin to pin type
– State Dependent Delay
– Table Look up Delay
– Input Slew
– Non-Linear Equation

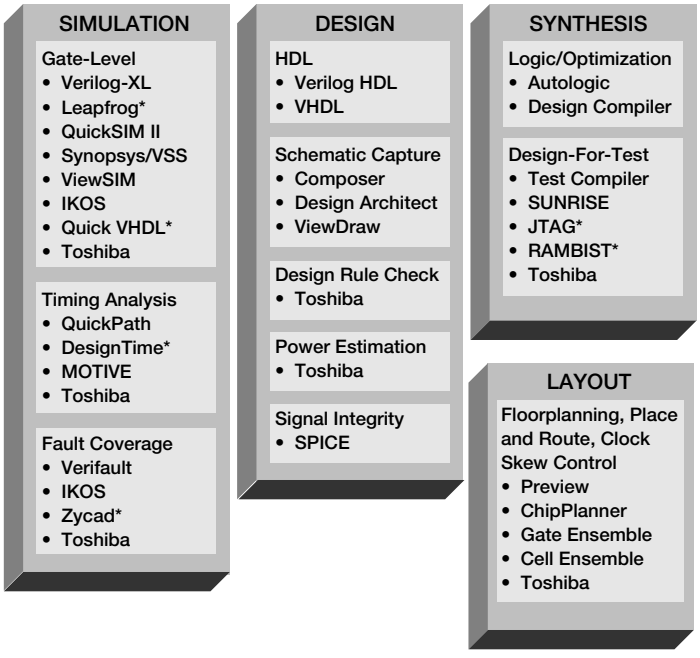
EDA Libraries and Design Kits

The TC190 series is supported by two design environments:

– The Toshiba traditional EDA system based on distriputed delay models
– The Toshiba Non-Linear Delay Model (NDM), which uses pin to pin timing and table lookup while taking into account the input slew rate as well as output load capacities.

Designers can use the traditional EDA option or the Verilog NDM sign-off system for the TC190 series. The libraies are upward compatible with the Toshiba 0.8µm ASIC family, thus reducing the effort needed when transferring a design from 0.8µm to 0.6µ technologies.

Toshiba Design Environment II



* In development

AS31710496

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