

### Description

TC280 is Toshiba's 0.11μm System Level Integration (SLI) ASIC family. TC280 is designed specifically for high-performance applications requiring low power dissipation in highly integrated dense circuits. Coupled with an all copper process, advanced packaging structures and a rich set of library offerings, the TC280 supports 7 levels of metal and high density memory structures. Toshiba offers the TC280 standard cell family for designs requiring tight clock skew and reduced interconnect delays, facilitated by copper process.

### Product Features

- 0.11μm (drawn) gate length
- 7 layer all copper process
- High gate density up to 206Kg/mm<sup>2</sup>
- Two sets of I/O offerings
  - Standard height I/O for pad limited designs
  - Short I/O for core limited designs
- High density SRAM cells
- 18ps with 10ps input slew for 2-Input NAND gate delay at fanout=1
- Vdd = 1.5V +/- 10% and I/O @ 1.5V, 1.8V, 2.5V, 3.3V.
- Typical power dissipation is 10nW/MHz.
- Two technology module options:
  - Precision 2.5V analog module for mixed signal applications
  - Performance module for optimizing timing paths
- Comprehensive core and I/O cell set for SLI implementation
- MegaGate Timing Driven Flow (TDF™)
- Advanced packaging structures with superior thermal & electrical properties

### DRAM Core Features

- There are 2 types of DRAM cores:
  - High-bandwidth, 250MHz SDRAM with 2-32Mb, 1-4 banks 64-256 bits wide per macrocell
  - Fast access DRAM with 10ns t<sub>RC</sub>, 2/4/8 Mb, 256 bits wide per macrocell
- Synchronous interface. All signals referenced to positive edge of the clock
- Automatic refresh
- Byte write data control
- Typical 40mm<sup>2</sup> die for 32Mb DRAM with 3M gates

- Typical 100mm<sup>2</sup> die for 128Mb DRAM with 3.5M gates.
- 1-transistor cell structure utilizing trench capacitor technology.

### Benefits of Embedded DRAM

- Flexibility in configuring the DRAM macrocell based on application requirements
- High bandwidth due to wide and fast memory busses.
- Faster access time than discrete DRAMs.
- Fewer external devices and reduction of total and ASIC pin count.
- Lower power dissipation- systems with fast and wide memory busses will dissipate significantly less power due to low capacitance on-chip connections.
- Lower switching noise on data bus between memory and Logic.

### Trench capacitor benefits

When compared to stacked capacitor technology, the trench capacitor technology has the following benefits:

- Higher density DRAM core and gate count for a given die size.
- Logic transistor performance is not degraded by manufacturing the memory capacitor.
- The trench capacitor, which is formed beneath the surface of the silicon, allows a planar silicon surface topology which improves reliability.
- Better soft error immunity, since these larger capacitors require higher charges to change states.

### System Level Packaging

The TC280 utilizes different I/O slot widths and heights to accommodate different flavors of design goals. The 40μm slot width and standard height I/O is more suitable for high pin count designs, while the 80μm slot width with low height I/O is more suited for core limited designs.

Toshiba's comprehensive package options include low-cost PQFP's, TBGA's and EBGA's. High performance, high pin count Flip chip BGA's are offered for designs requiring pin counts in excess of 1000 pins backed by superior thermal and electrical properties. Toshiba also offers fine-pitch BGA's. The TC280 is available in many other standard package options and pin counts.

## Application Specific IP

Toshiba supports an ever growing selection of IP cores in many technologies. These range from basic cells, such as RAM, ROM, register files, A/D, D/A and PLL through application specific IP such as USB, IEEE 1394, ethernet MAC, gigabit SerDes, DRAC, RISC, MPEG, QAM and QPSK. IP is developed by Toshiba, obtained from third-party partners or provided by customers. Contact Toshiba for detailed TC280 IP availability.

## MegaGate TDF

Toshiba employs an advanced EDA methodology, MegaGate TDF for obtaining performance validation and timing closure which is based upon Toshiba's proven Timing-Driven Flow (TDF) methodology. Also incorporating signal integrity analysis, this is the only appropriate ASIC design methodology for the 0.11 $\mu$ m technology. MegaGate TDF is based upon a tightly integrated commercial EDA tool set for optimal block hierarchy and uses accurate 3D timing models for extraction. Using the TDF methodology results in reduced design cycle time and fewer iterations.

## Technology Resource Centers

Toshiba SLI ASIC Technology Resource Centers are located throughout the U.S. to provide technical support before, during and after the design of a Toshiba ASIC. This includes support with EDA methodologies and design kits, Toshiba design methodologies, ASIC technologies and design implementation. In addition, Toshiba's North American Semiconductor Engineering Development Center based in San Jose, CA is staffed with system, technology and EDA design experts who work with customers on advanced system IC applications, and who can also provide complete design services.

## High Quality Volume Manufacturing

Toshiba's ASIC manufacturing plants are among the largest and most advanced in the world. They are all certified to ISO9000. Rigorous quality control coupled with a sophisticated batch tracking system allows Toshiba to meet the needs of fast-ramping, high-volume markets.

For the more details on this subject, please visit: <http://www.asic.toshiba.com>. dRAMASIC and MegaGate Timing-Driven Flow are all trademarks of Toshiba Corporation.

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