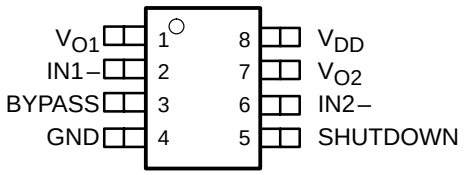
- **150 mW Stereo Output**
- **PC Power Supply Compatible**
  - **Fully Specified for 3.3-V and 5-V Operation**
  - **Operation to 2.5 V**
- **Pop Reduction Circuitry**
- **Internal Midrail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **PowerPAD™ MSOP**
  - **SOIC**
- **Pin Compatible With TPA122, LM4880, and LM4881 (SOIC)**

D OR DGN PACKAGE
(TOP VIEW)

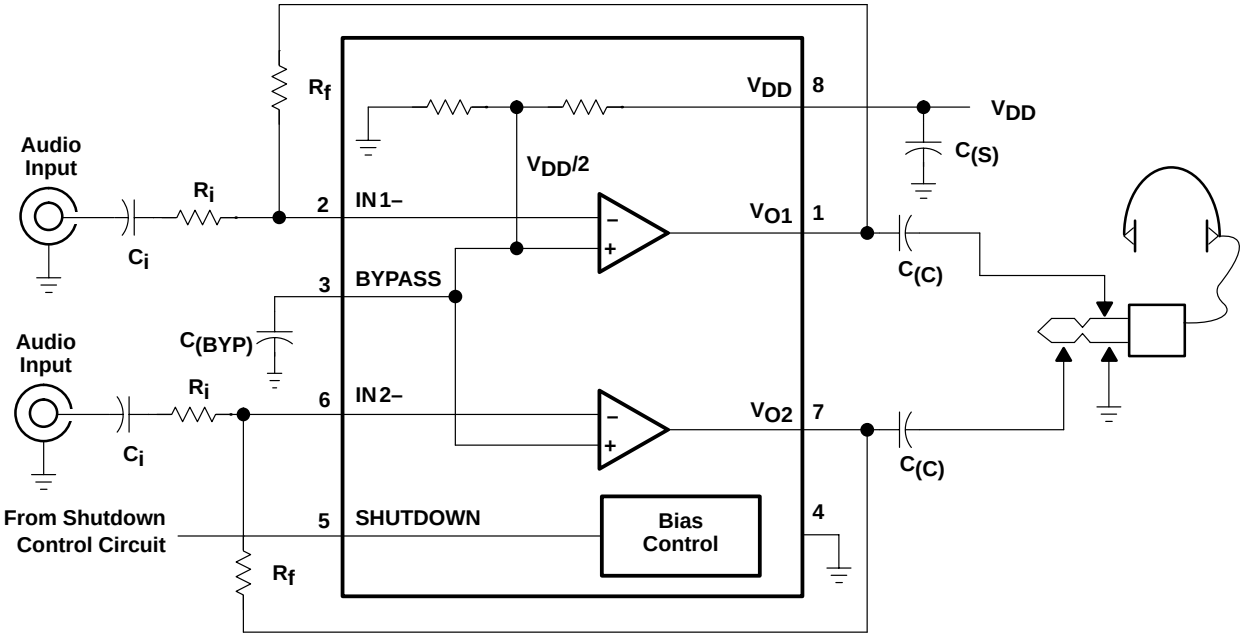


description

The TPA6111A2 is a stereo audio power amplifier packaged in either an 8-pin SOIC or an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 0 to 20 dB.

THD+N, when driving a 16-Ω load from 5 V, is 0.03% at 1 kHz, and less than 1% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.02% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.005% at 1 kHz, and less than 0.5% across the audio band of 20 Hz to 20 kHz.

typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA6111A2D	TPA6111A2DGN	TI AJA

† The D and DGN package is available in left-ended tape and reel only (e.g., TPA6111A2DR, TPA6111A2DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 μF to 1 μF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_{O1}	1	O	V_{O1} is the audio output for channel 1.
V_{O2}	7	O	V_{O2} is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . internally limited
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

§ See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C
High-level input voltage, V_{IH}, (SHUTDOWN)	60% x V_{DD}		V
Low-level input voltage, V_{IL}, (SHUTDOWN)		25% x V_{DD}	V

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	μA
Z_i	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%,	f = 1 kHz		60		mW
THD+N	Total harmonic distortion + noise	P_O = 40 mW,	20 – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB,	THD < 5%		>20		kHz
	Phase margin	Open loop			96°		
	Supply ripple rejection	f = 1 kHz,	$C_{(BYP)}$ = 0.47 μF		71		dB
	Channel/channel output separation	f = 1 kHz,	P_O = 40 mW		89		dB
SNR	Signal-to-noise ratio	P_O = 50 mW,	A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1			11		μV(rms)

dc electrical characteristics at T_A = 25°C, V_{DD} = 5.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.6	3.2	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	μA
$\|I_{IH}\|$	High-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = V_{DD}			1	μA
$\|I_{IL}\|$	Low-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = 0 V			1	μA
Z_i	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%,	f = 1 kHz		150		mW
THD+N	Total harmonic distortion + noise	P_O = 100 mW,	20 – 20 kHz		0.6%		
B_{OM}	Maximum output power BW	G = 20 dB,	THD < 5%		>20		kHz
	Phase margin	Open loop			96°		
	Supply ripple rejection ratio	f = 1 kHz,	$C_{(BYP)}$ = 0.47 μF		61		dB
	Channel/channel output separation	f = 1 kHz,	P_O = 100 mW		90		dB
SNR	Signal-to-noise ratio	P_O = 100 mW,	A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1			11.7		μV(rms)

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%,	f = 1 kHz		35		mW
THD+N	Total harmonic distortion + noise	P_O = 40 mW,	20 – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB,	THD < 2%		>20		kHz
	Phase margin	Open loop			96°		
	Supply ripple rejection	f = 1 kHz,	$C_{(BYP)}$ = 0.47 μF		71		dB
	Channel/channel output separation	f = 1 kHz,	P_O = 25 mW		75		dB
SNR	Signal-to-noise ratio	P_O = 90 mW,	A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1			11		μV(rms)

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%,	f = 1 kHz		90		mW
THD+N	Total harmonic distortion + noise	P_O = 20 mW,	20 – 20 kHz		2%		
B_{OM}	Maximum output power BW	G = 20 dB,	THD < 2%		>20		kHz
	Phase margin	Open loop			97°		
	Supply ripple rejection	f = 1 kHz,	$C_{(BYP)}$ = 0.47 μF		61		dB
	Channel/channel output separation	f = 1 kHz,	P_O = 65 mW		98		dB
SNR	Signal-to-noise ratio	P_O = 90 mW,	A_V = 1		104		dB
V_n	Noise output voltage	A_V = 1			11.7		μV(rms)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 3, 5, 6, 7, 9, 11, 13,
		vs Output power	2, 4, 8, 10, 12, 14
	Supply ripple rejection ratio	vs Frequency	15, 16
V_n	Output noise voltage	vs Frequency	17, 18
	Crosstalk	vs Frequency	19 – 24
	Shutdown attenuation	vs Frequency	25, 26
	Open-loop gain and phase margin	vs Frequency	27, 28
	Output power	vs Load resistance	29, 30,
I_{DD}	Supply current	vs Supply voltage	31
SNR	Signal-to-noise ratio	vs Voltage gain	32
	Power dissipation/amplifier	vs Load power	33, 34

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

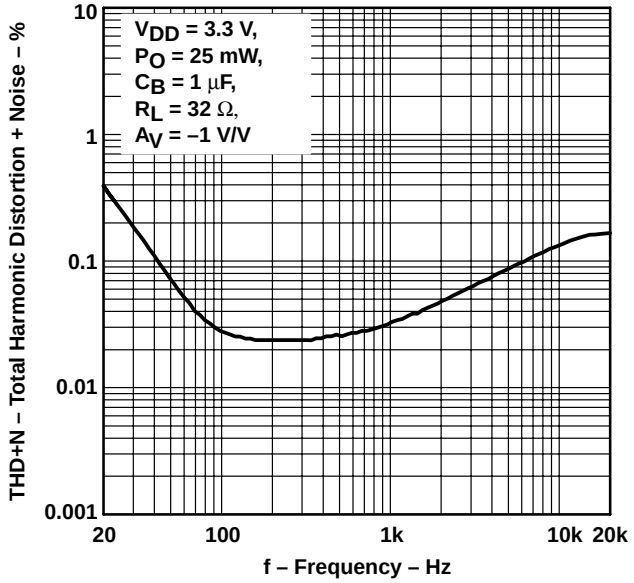


Figure 1

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

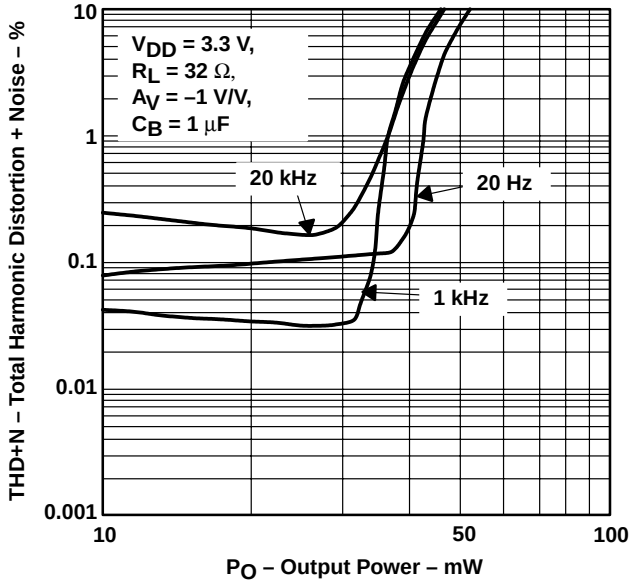


Figure 2

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

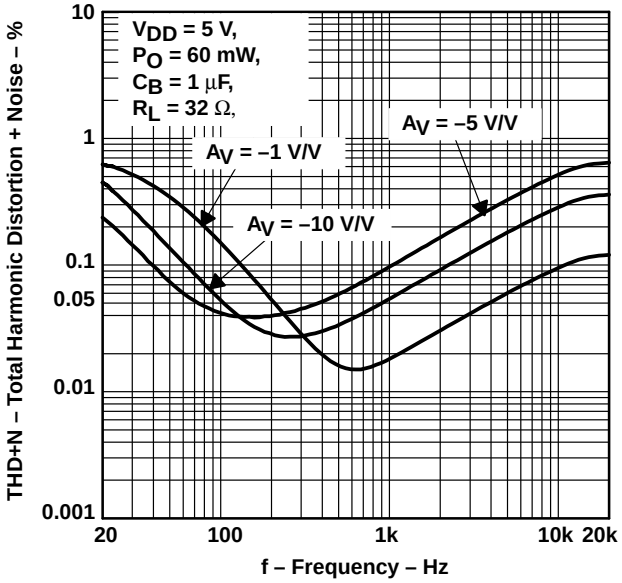


Figure 3

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

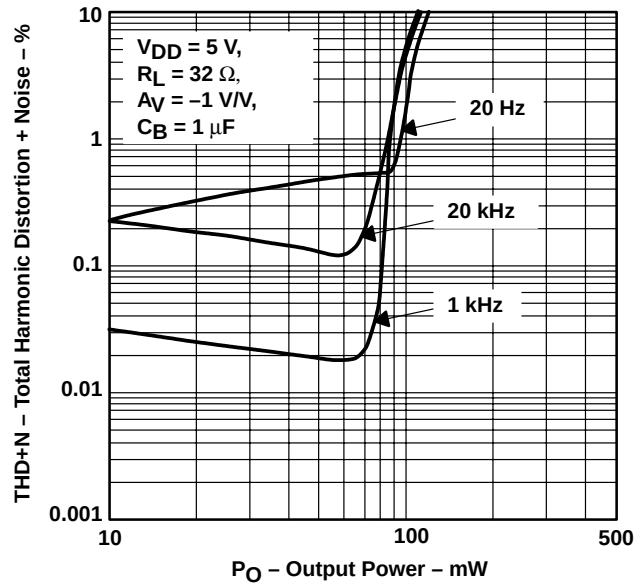


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

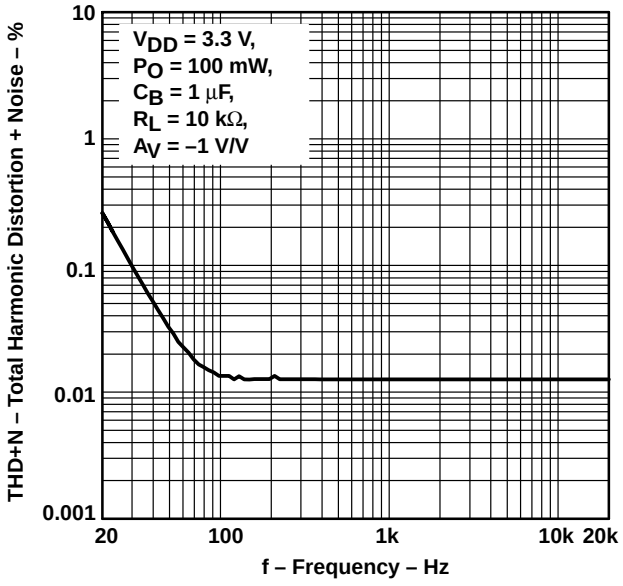


Figure 5

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

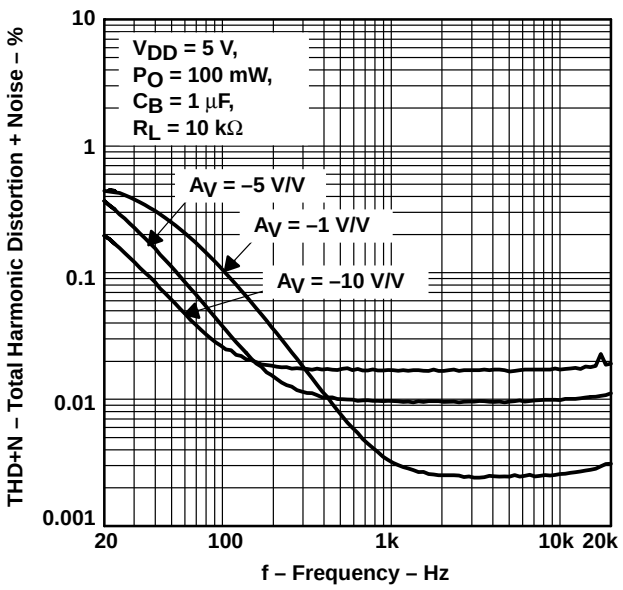


Figure 6

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

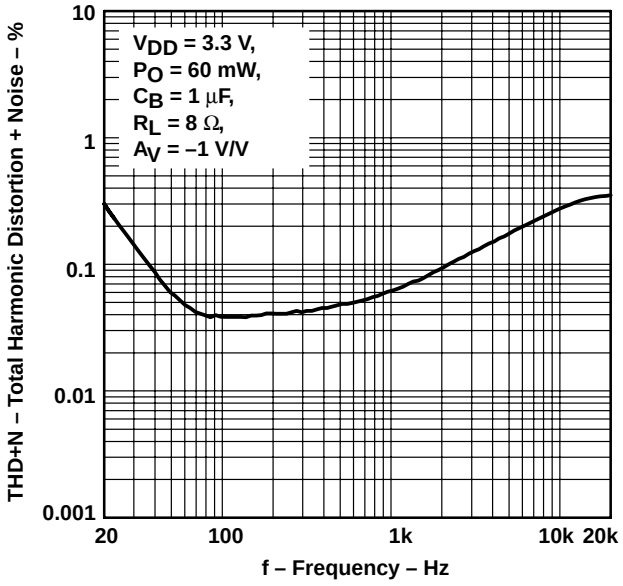


Figure 7

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

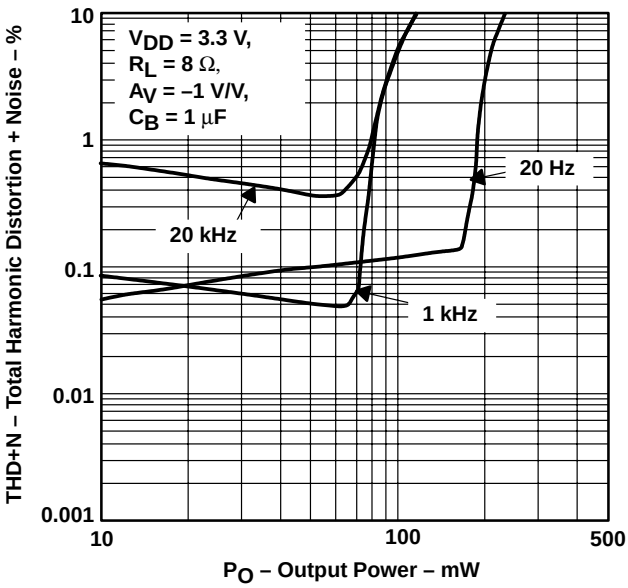


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

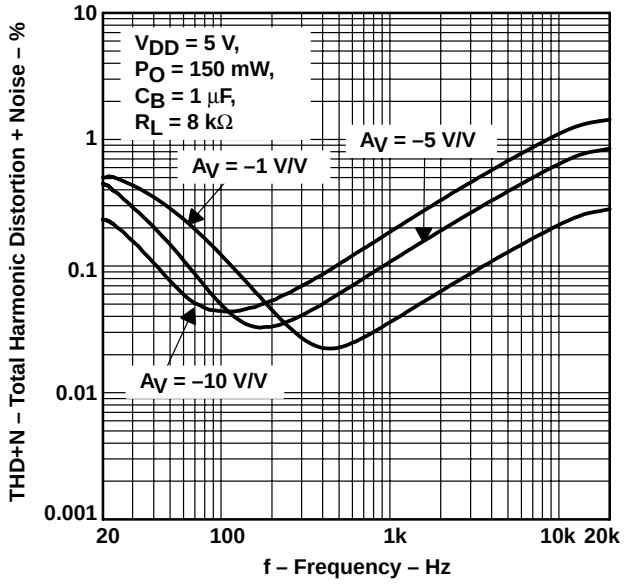


Figure 9

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

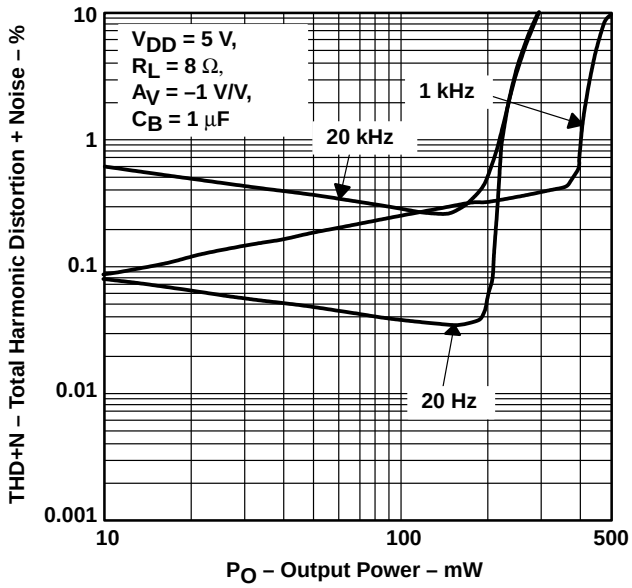


Figure 10

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

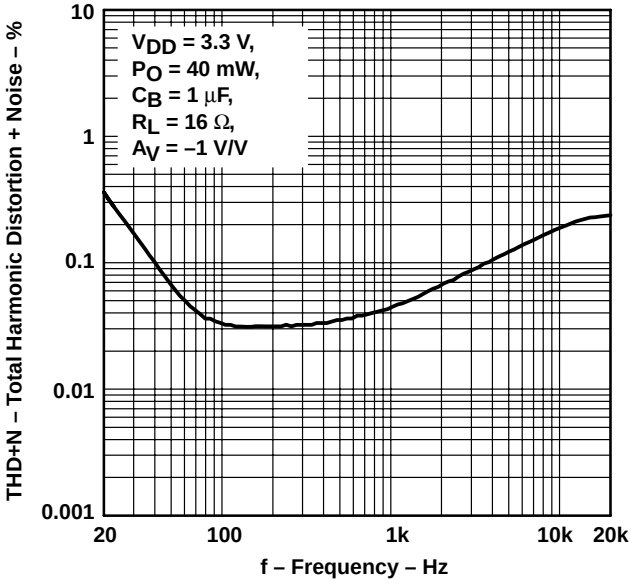


Figure 11

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

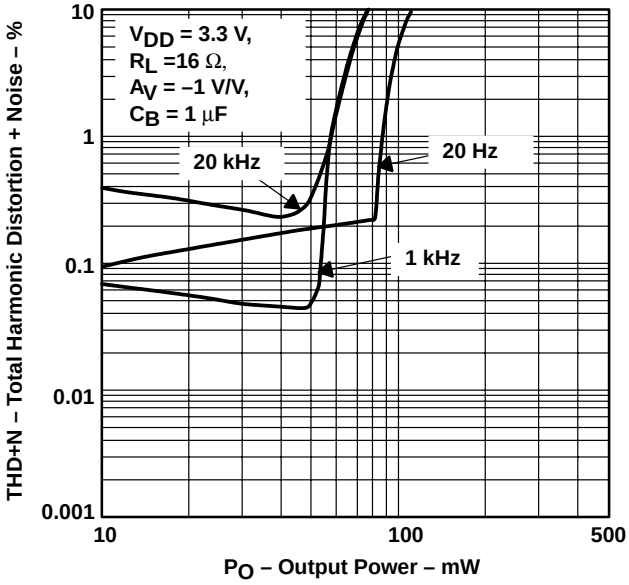


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

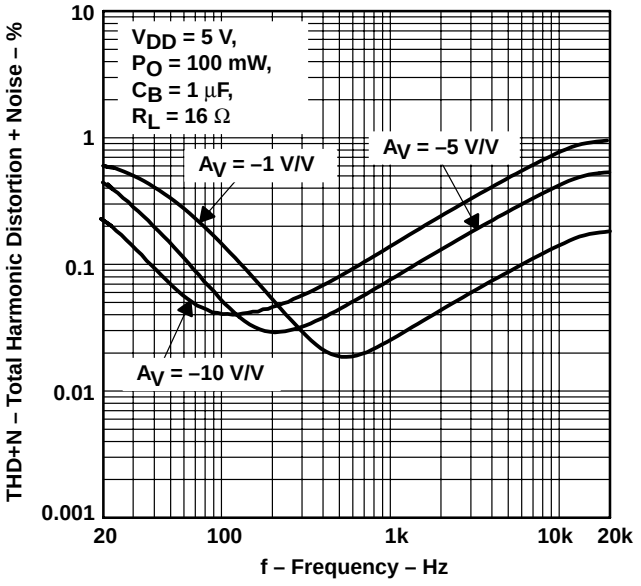


Figure 13

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

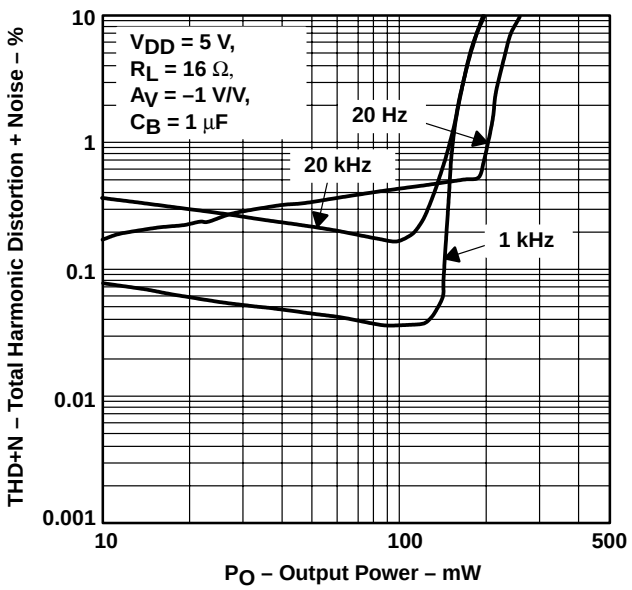


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

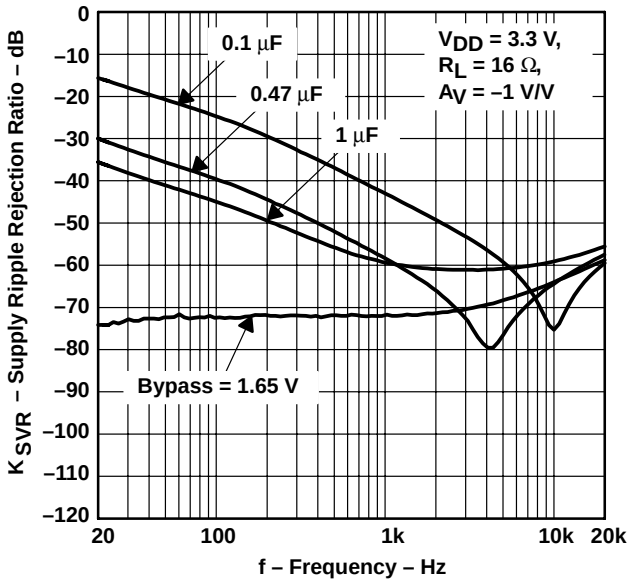


Figure 15

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

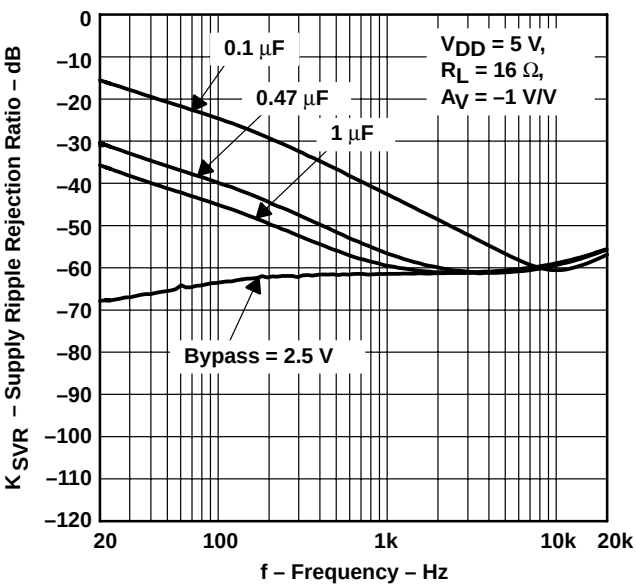


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

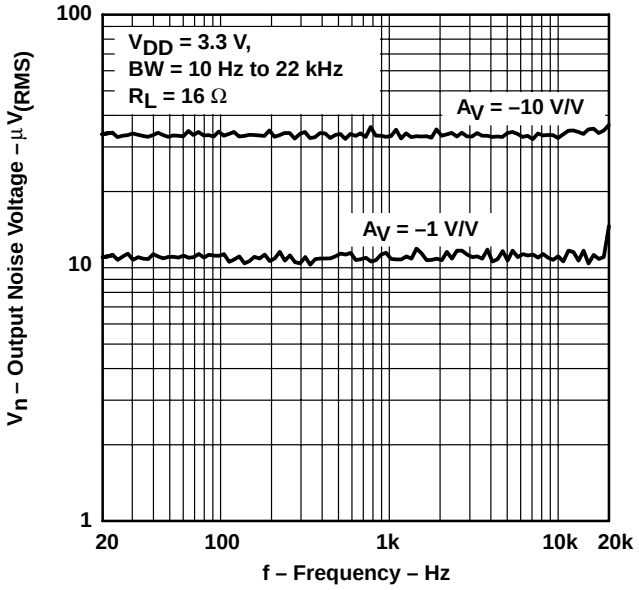


Figure 17

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

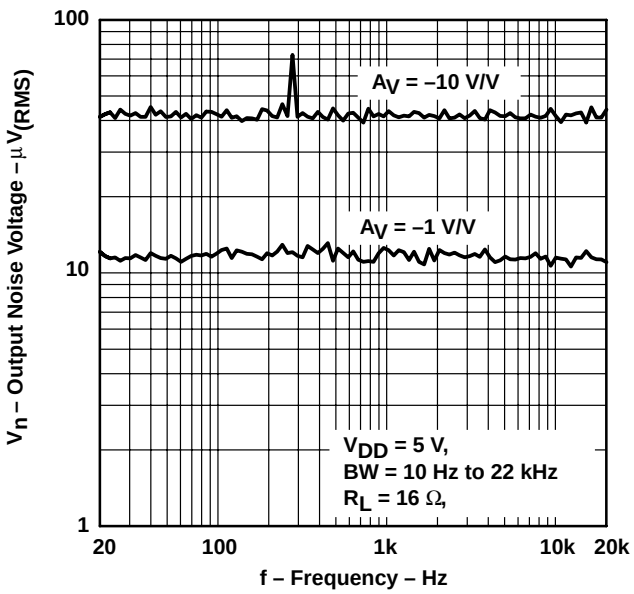


Figure 18

CROSSTALK
vs
FREQUENCY

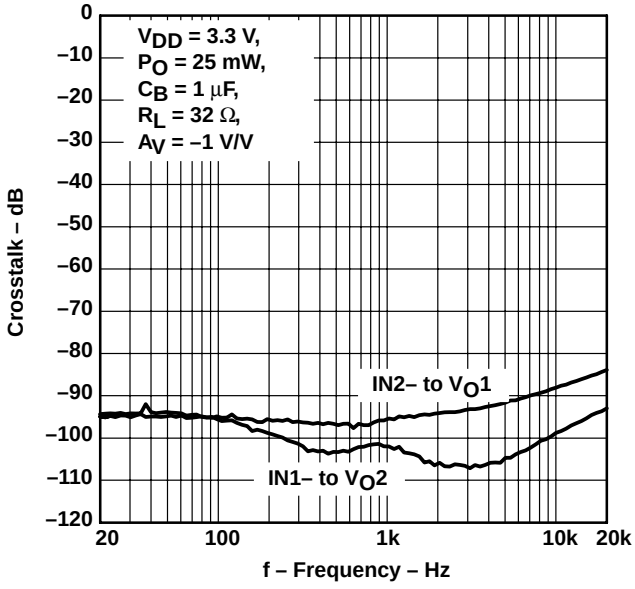


Figure 19

CROSSTALK
vs
FREQUENCY

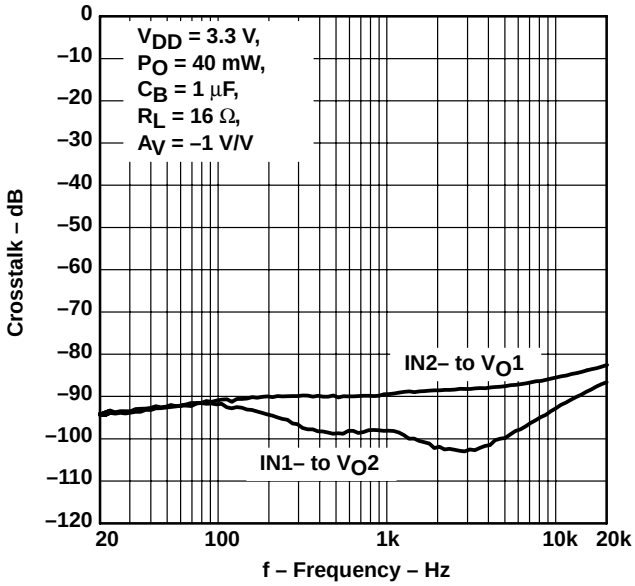


Figure 20

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

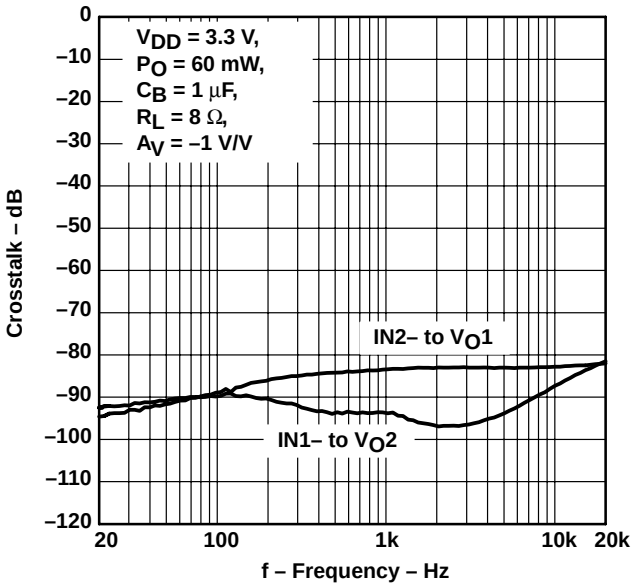


Figure 21

CROSSTALK vs FREQUENCY

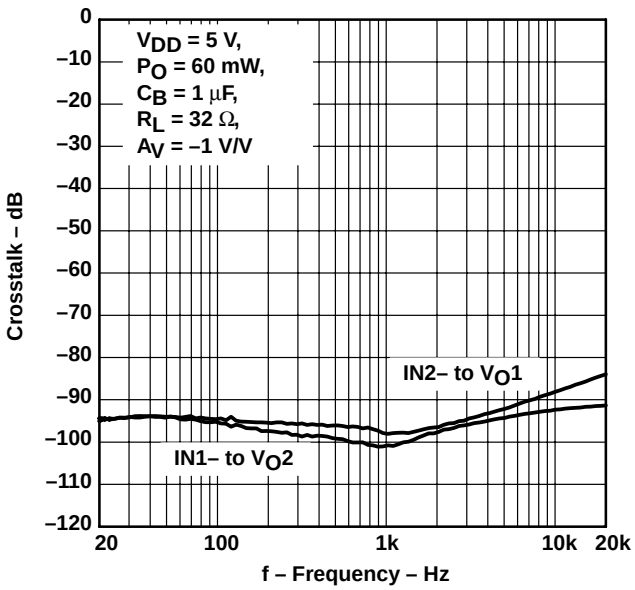


Figure 22

CROSSTALK vs FREQUENCY

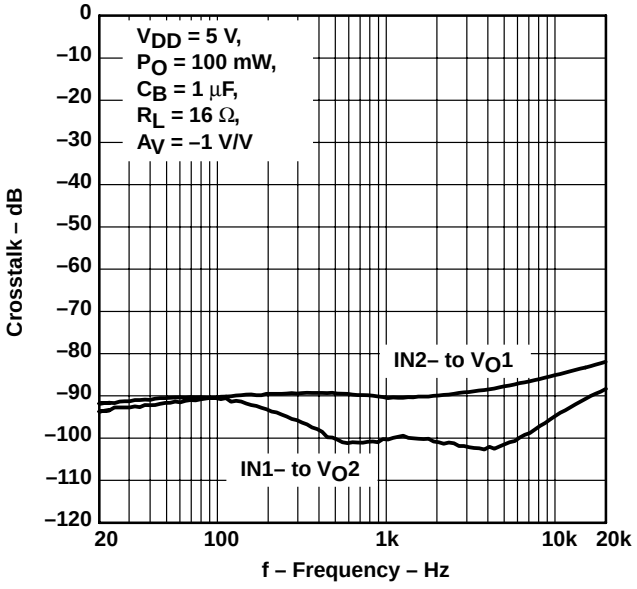


Figure 23

CROSSTALK vs FREQUENCY

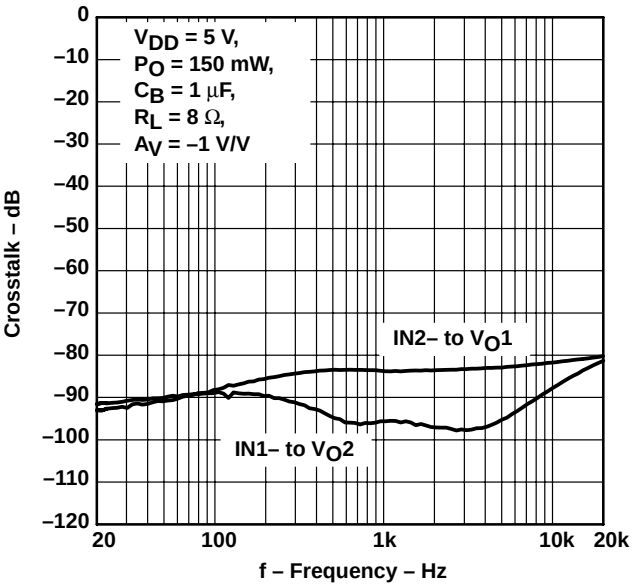


Figure 24

TYPICAL CHARACTERISTICS

SHUTDOWN ATTENUATION vs FREQUENCY

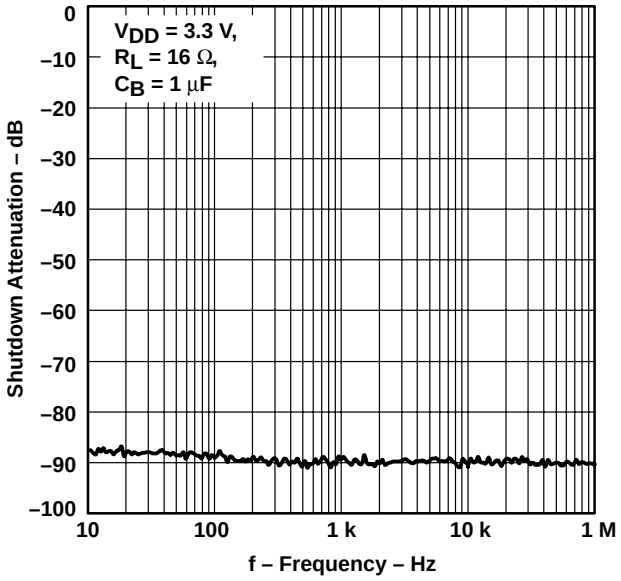


Figure 25

SHUTDOWN ATTENUATION vs FREQUENCY

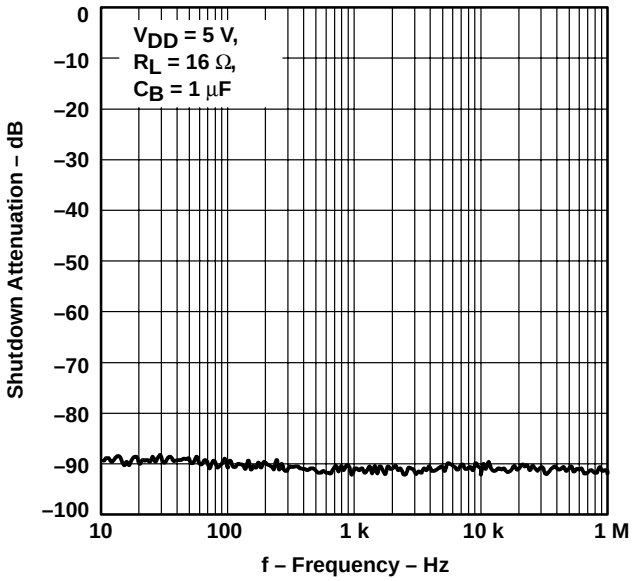


Figure 26

OPEN-LOOP GAIN AND PHASE MARGIN vs FREQUENCY

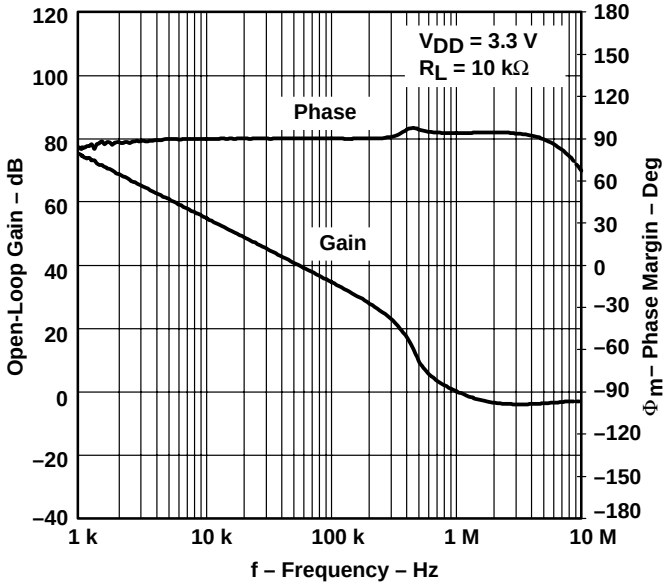


Figure 27

OPEN-LOOP GAIN AND PHASE MARGIN vs FREQUENCY

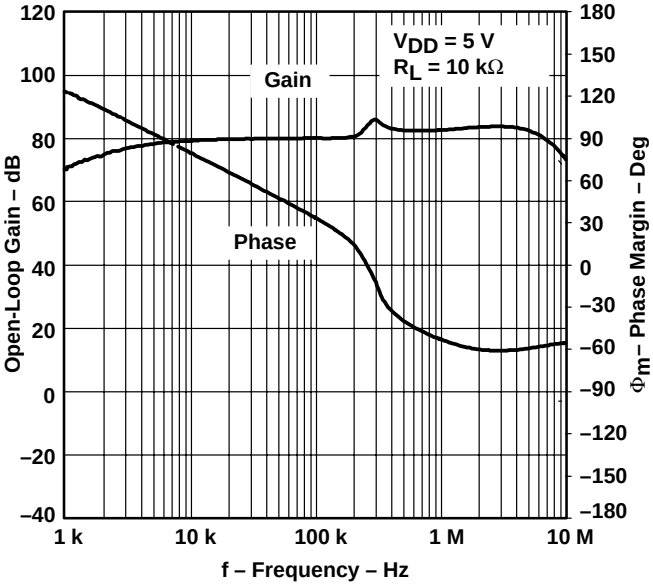


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

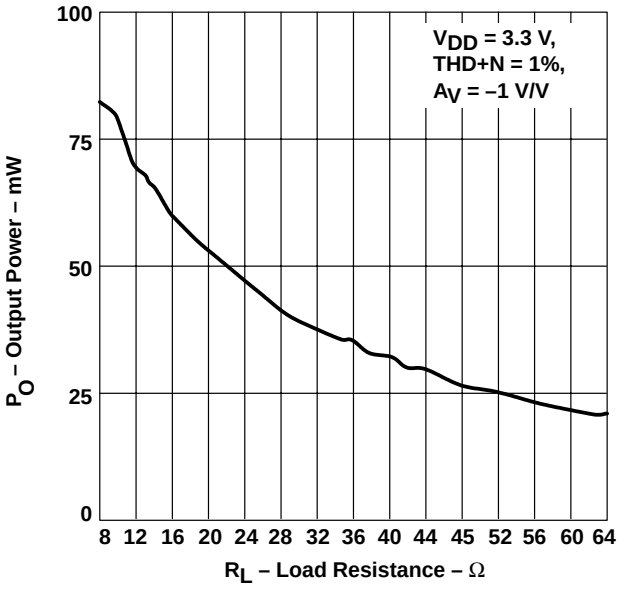


Figure 29

OUTPUT POWER vs LOAD RESISTANCE

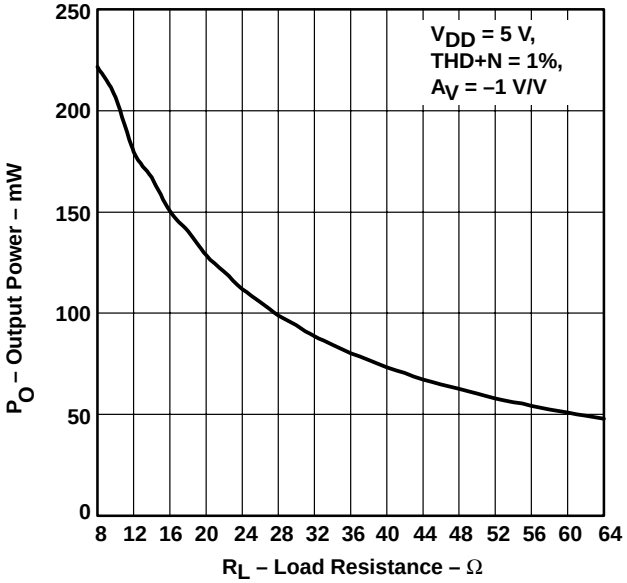


Figure 30

SUPPLY CURRENT vs SUPPLY VOLTAGE

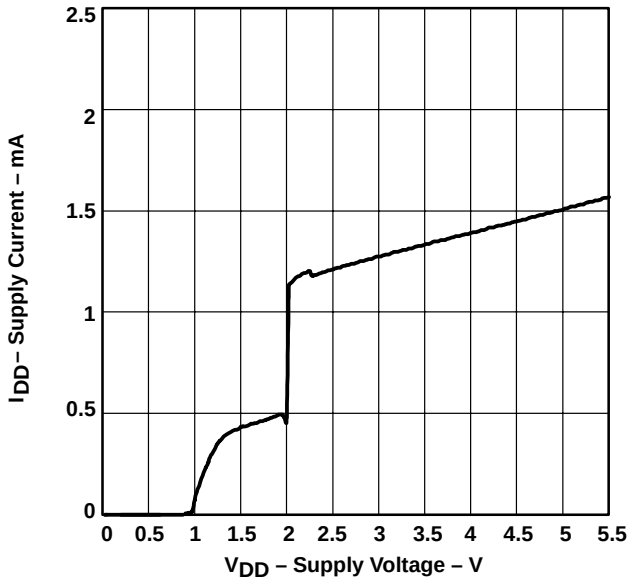


Figure 31

SIGNAL-TO-NOISE RATIO vs VOLTAGE GAIN

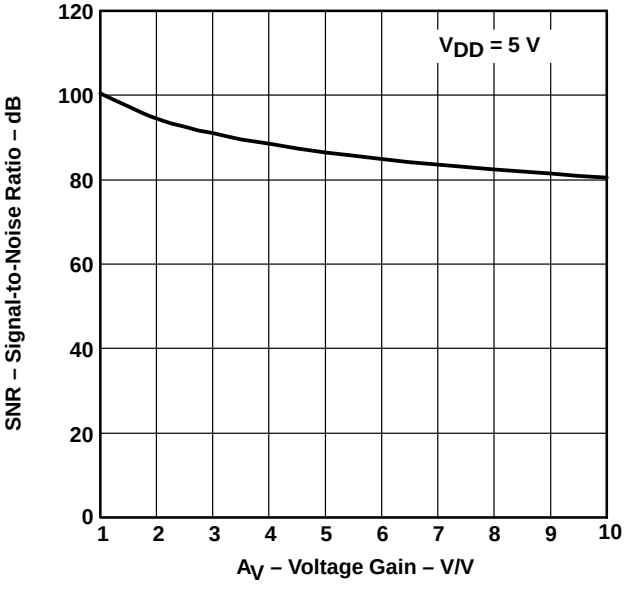


Figure 32

TYPICAL CHARACTERISTICS

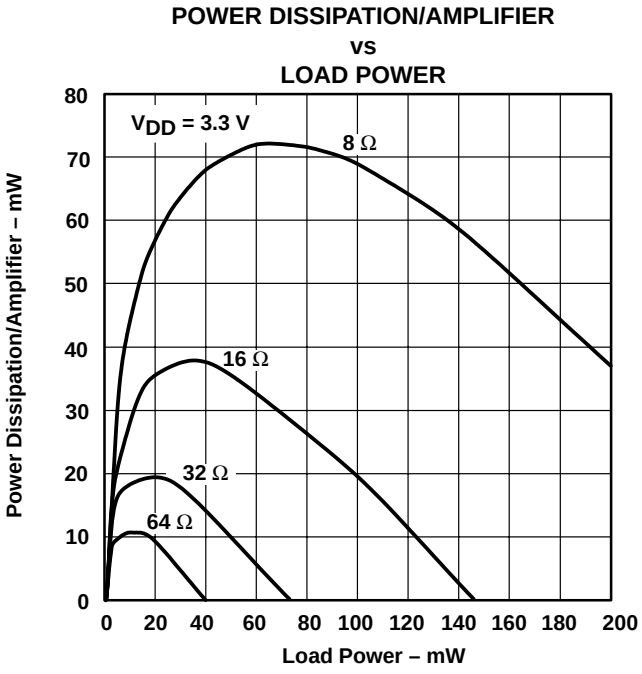


Figure 33

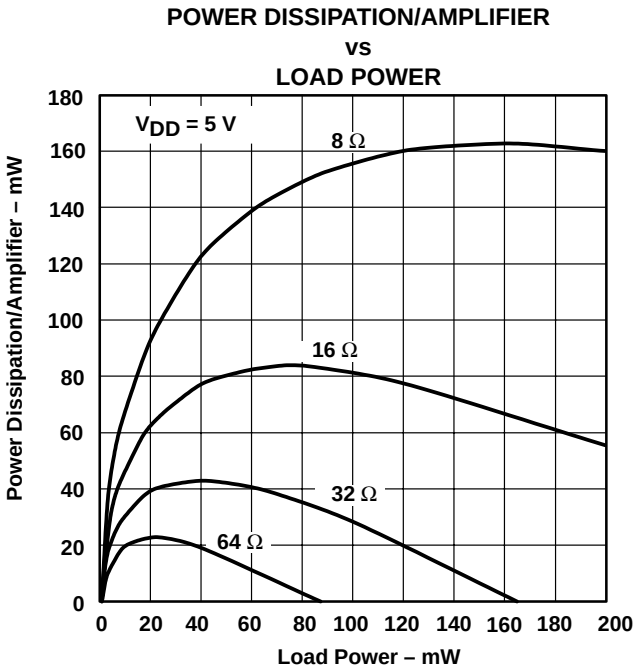


Figure 34

APPLICATION INFORMATION

gain setting resistors, R_f and R_i

The gain for the TPA6111A2 is set by resistors R_f and R_i according to equation 1.

$$\text{Gain} = -\left(\frac{R_f}{R_i}\right) \tag{1}$$

Given that the TPA6111A2 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_f increases. In addition, a certain range of R_f values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_f R_i}{R_f + R_i} \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_f above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_f and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_f. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_f C_F} \tag{3}$$

For example, if R_f is 100 kΩ and C_F is 5 pF then $f_{c(\text{lowpass})}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and R_i form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_i C_i} \tag{4}$$

The value of C_i is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_i = \frac{1}{2\pi R_i f_{c(\text{highpass})}} \tag{5}$$

APPLICATION INFORMATION

input capacitor, C_i (continued)

In this example, C_i is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i, C_i) and the feedback resistor (R_f) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, $C_{(S)}$

The TPA6111A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, $C_{(BYP)}$

The midrail bypass capacitor, $C_{(BYP)}$, serves several important functions. During start-up, $C_{(BYP)}$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{\left(C_{(BYP)} \times 230\ k\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \tag{6}$$

As an example, consider a circuit where $C_{(BYP)}$ is 1 μF, C_i is 1 μF, and R_i is 20 kΩ. Inserting these values into the equation 9 results in: $6.25 \leq 50$ which satisfies the rule. Bypass capacitor, $C_{(BYP)}$, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, $C_{(C)}$

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_c = \frac{1}{2\pi R_L C_{(C)}} \tag{7}$$

APPLICATION INFORMATION

output coupling capacitor, $C_{(C)}$ (continued)

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 68 μF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 μF	73 Hz
10,000 Ω	68 μF	0.23 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_{(BYP)} \times 230\ k\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \ll \frac{1}{R_L C_{(C)}} \quad (8)$$

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

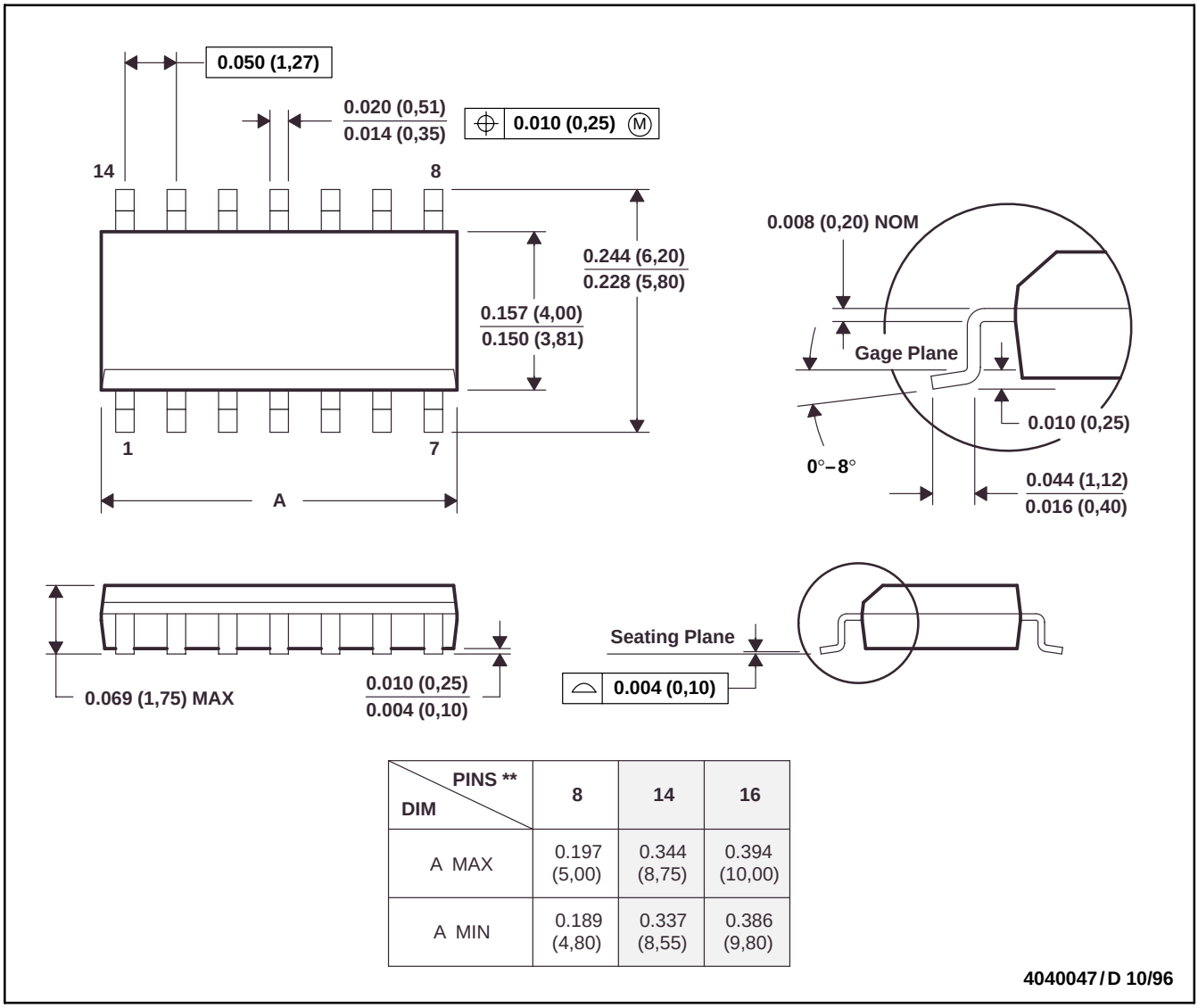
5-V versus 3.3-V operation

The TPA6111A2 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA6111A2 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



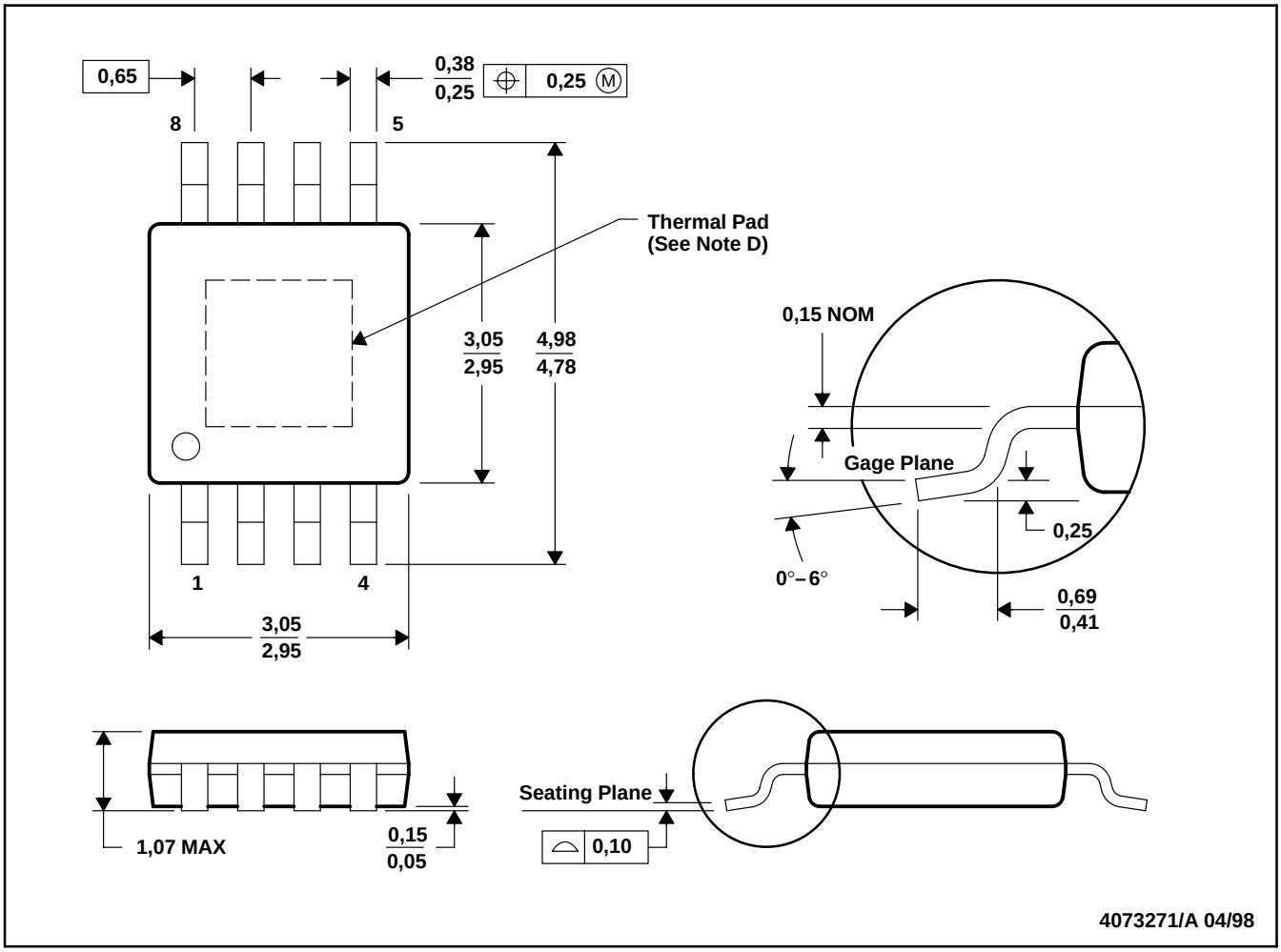
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

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