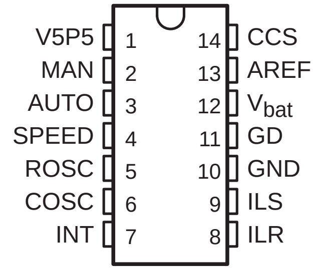
- **0 V to 16 V, 50 mA Max PWM Gate Drive Output**
- **Dual Speed Command Input Capability**
- **Effective Motor Voltage Adjustment**
- **100% Duty Cycle Capability**
- **Low Current (<200 µA) Sleep State**
- **Built-in Soft Start**
- **Over/Under Voltage Protection**
- **Over Current Protection of External FET/IGBT**

D or N PACKAGE
(TOP VIEW)



description

The TPIC2101 is a monolithic integrated control circuit designed for direct current (dc) brush motor control that generates a user-adjustable, fixed-frequency, variable duty cycle, pulse width modulated (PWM) signal primarily to control rotor speed of a permanent magnet dc motor. The TPIC2101 can also be used to control power to other loads such as solenoids and incandescent bulbs. This device drives the gate of an external, low side NMOS power transistor to provide PWM controlled power to a motor or other loads. Inductive current from motor or solenoid loads during PWM off-time is recirculated through an external diode.

The TPIC2101 accepts a 0% to 100% PWM signal (auto mode) or a 0 V to 2.2 V differential voltage (manual mode), and internally engages the correct operating mode to accept the input type.

The device operates in a sleep state, a run state, or a fault state. In the sleep state the gate-drive (GD) terminal is held low and the overall current draw is less than 200 µA. The normal operating mode of the device is in the run state and is initiated by any speed command. When the device detects an overvoltage or current fault, it enters the fault state.

The TPIC2101 is offered in a 14-terminal plastic DIP (N) package, and a SOIC (D) package, and is characterized for operation over the operating free-air temperature range of –40°C to 105°C.

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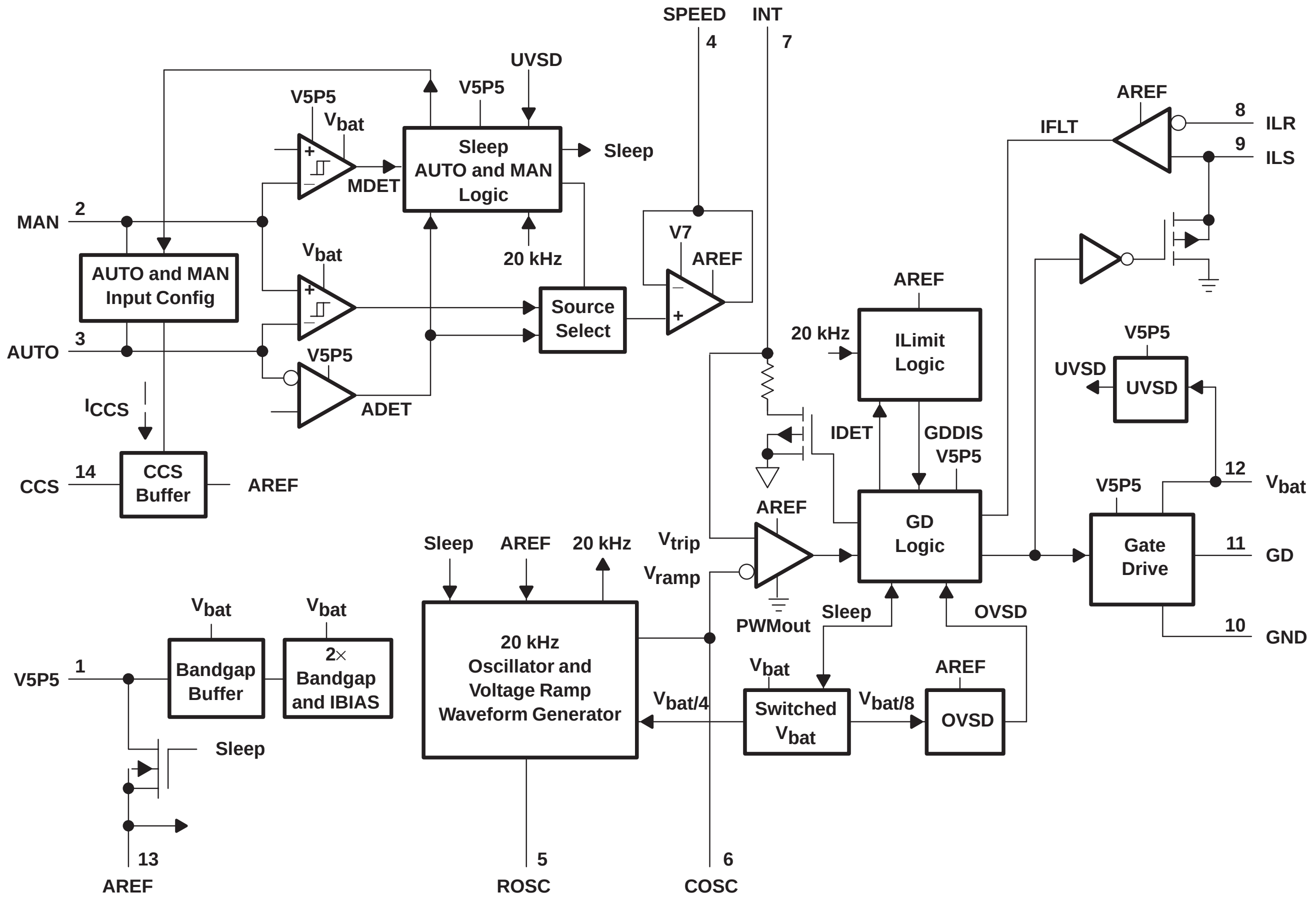
functional block diagram



NOTE A: For correct operation, no terminal may be taken below GND.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
V5P5	1	O	5.5 V supply voltage. V5P5 is a regulated voltage supply from V_{bat}, internally switched to AREF during the run state. This requires a 4.7 µF tantalum capacitor from V5P5 to GND for stability.
MAN	2	I	Manual control input. MAN is an active high (greater than 5.5 V asserts the manual mode) input that serves as a positive differential input (0-2.3 V full range) for the manual mode. In man mode, I_{man} is approx. 20×I_{CCS}.
AUTO	3	I	PWM control input. AUTO is an active low input that remains active if pulsed every 2048 counts of the oscillator frequency. It also serves as a negative differential input for the manual mode. In auto mode, I_{auto} is approx. 13×Iccs pullup, I_{auto} is approx. 20×I_{CCS} pulldown in man mode.
SPEED	4	O	Integrator output. SPEED is an integrator output with a required minimum resistance between SPEED and INT terminals of 20 kΩ (typically 1 second RC time constant, or as required for soft start).
ROSC	5	O	Oscillator resistor output. ROSC has an external resistor connected to ground which determines the constant charging current of COSC. The IC forces a voltage of V_{bat}/4 in run state.
COSC	6	O	Oscillator capacitor output. COSC has an external capacitor connected to ground which determines (with ROSC) switching frequency. f(osc) = 2/(ROSC×COSC)
INT	7	I	Integrator input. INT is an input from an integrator that requires a 4.7 µF capacitor and a 20 k minimum resistance between the SPEED and INT terminals.
ILR	8	I	Current limit reference. ILR is an input from a resistor divider off AREF.
ILS	9	I	Current limit sense. ILS senses drain voltage of external FET. ILS trips within ±10 mV of ILR.
GND	10		Ground terminal
GD	11	O	Gate drive output. GD, PWM output, 0-V_{bat} voltage, provides a 0-V_{bat} PWM output pre-drive for an external FET.
V_{bat}	12	I	Positive power input.
AREF	13	O	5.5 V reference voltage. AREF is a 5.5 V reference voltage switched from V5P5 during the run state. AREF is used as a reference for ILR in current limit detection and is capable of sourcing 2 mA of current.
CCS	14		Constant current sink. I_{CCS} equals AREF/(2×R_{ccs}). Requires an external resistor.

recommended external components for auto and manual modes (see Figures 2 and 4)

TERMINAL NAME	NO.	DESCRIPTION
V5P5	1	Capacitor – 4.7 µF tantalum
MAN	2	Capacitor – 0.1 µF
MAN	2	Resistor – 499 Ω, 1%, 100 ppm
AUTO	3	Capacitor – 0.47 µF
AUTO	3	Resistor – 499 Ω, 1%, 100 ppm
SPEED	4	Resistor – 100 kΩ, 1%, 100 ppm to INT terminal, (minimum 20 kΩ)
ROSC	5	Resistor – 45.3 kΩ
COSC	6	Capacitor – 2200 pF
INT	7	Capacitor – 4.7 µF
CCS	14	Resistor – 27.4 kΩ, 1%, 100 ppm

detailed description

The TPIC2101 is an integrated circuit that generates a fixed frequency, variable duty cycle PWM signal to control the rotor speed of a permanent-magnet dc motor. This section provides a functional description of the device.

dual command speed input capability

The TPIC2101 is user configurable to either auto or manual mode, and can sense either configuration internal to the IC. In automatic mode, the speed-command-signal is an open-collector PWM signal on the AUTO terminal, and the MAN terminal is floating. In manual mode, the speed-command-signal is a variable resistance across the AUTO and MAN terminals with the MAN terminal connected to V_{bat}.

sleep, run, and fault states

The TPIC2101 operates in a sleep state, a run state, or a fault state. In the auto mode, a zero-speed input initiates the sleep state. In the manual mode, an open-circuit at the AUTO and MAN terminals initiates the sleep state. The device will also be in the sleep state during fault conditions. In the sleep state, the gate drive terminal (GD) is held low and the overall current draw is less than 200 µA. Any speed command initiates the run state, which is the normal operating state of the device. The fault state is entered only when the device detects an overvoltage or current fault. Fault state is exited either by removal of the overvoltage condition (exiting to run state) or by resetting a current fault by entering the sleep state.

speed command adjustment

The device adjusts the GD terminal PWM signal with changes in V_{bat} to keep the effective motor voltage constant. The effective motor voltage is defined to be the product of the GD terminal PWM rate and the voltage of V_{bat}. Figure 1 shows motor voltage as a function of input speed command in the automatic mode for various battery voltages. PWM_{in} is described as the duty cycle of the PWM signal at the AUTO terminal.

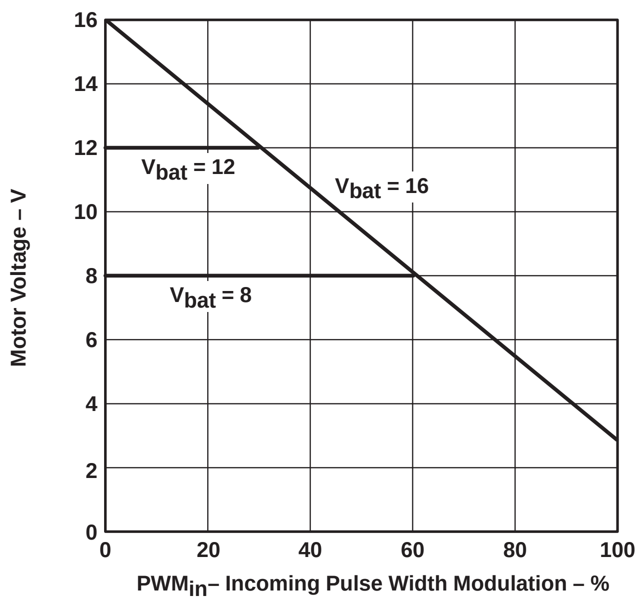


Figure 1. Motor Voltage vs. Incoming PWM for Various Battery Voltages

over/under voltage protection

The IC enters the fault state if V_{bat} rises above over-voltage shutdown (V_{OV} typically equals 18.5 V). If V_{bat} falls below the under-voltage shutdown (V_{UV} typically equals 7.5 volts) the IC enters sleep state. Hysteresis assures that the device will not toggle into and out of sleep state or fault condition.

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current limit protection

Current through the motor is limited by lowering the GD terminal PWM when a high current situation occurs. If the condition persists, the device shuts off the gate drive (GD terminal) until the circuit is reset externally by entering the sleep state.

theory of operation

This section explains the normal circuit operation for the automatic and manual states.

power supply and oscillator

Positive voltage is supplied to the integrated circuit on the V_{bat} terminal, ground is the GND terminal. The IC steps down the V_{bat} supply to the regulated 5.5 V supply at the V5P5 terminal. AREF is shorted to V5P5 in run state and disconnected when the IC is in sleep state. Two terminal connections (COSC and ROSC) are provided to control an internal oscillator. The oscillator freq, $f_{(osc)}$, is defined by the following equation:

$$f_{(osc)} = \frac{2}{ROSC \times COSC}$$

Nominal oscillator frequency is 20-kHz based on the recommended components.

automatic mode signal decoding

In automatic state, a high-to-low signal transition on the AUTO terminal (open collector) will wake the device from the sleep state into the run state. The speed command information is contained in the duty cycle of a 100 Hz PWM signal on the same terminal. The speed information is inverted, i.e. a signal that is 10% high commands a faster speed than a 20% high signal. In automatic mode the MAN terminal is floating. The device is capable of rejecting ± 2 V of ground offset V_{IO} between the open-collector switching transistor and the GND terminal without affecting the output duty cycle. Two terminals are provided for an RC integrator (SPEED and INT) to average the incoming PWM signal for use as a PWM comparator input. Figure 2 illustrates the automatic state connections.

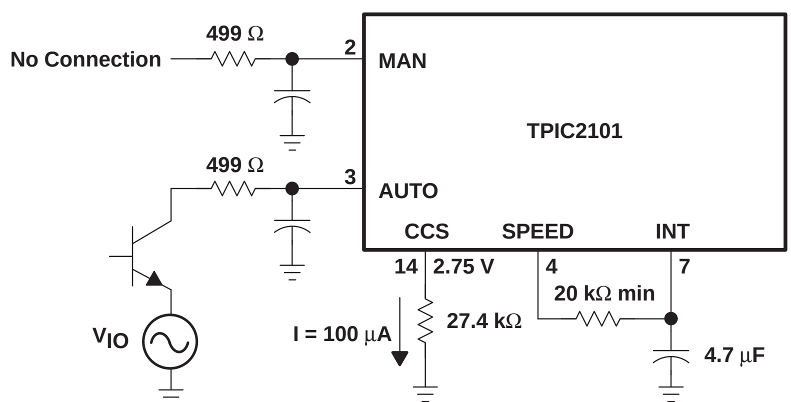


Figure 2. Automatic Mode Connections

automatic mode signal decoding (continued)

The device enters the sleep state if the PWM signal on the AUTO terminal is absent (the AUTO terminal remains high or low) for 2048 clock cycles of the 20 KHz oscillator. An internal 1 mA pull-up resistor is provided for the AUTO terminal when in the auto mode. This pull-up resistor is not present in the manual mode or during sleep state.

The device adjusts the output PWM duty cycle to keep the effective motor voltage constant with changing battery voltages (V_{bat}) as per the equation:

$$PWM_{out} = \frac{(2.88 + 13.12(1 - \text{Input Duty Cycle}))}{V_{bat}} \times 100\%$$

Figure 3 illustrates this transfer curve with various battery voltages.

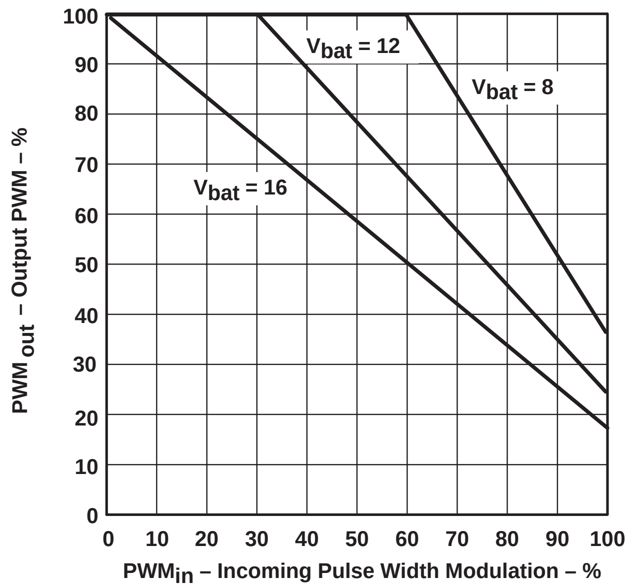


Figure 3. Output PWM vs. Incoming PWM for Various Battery Voltages

The allowable automatic mode PWM_{out} variation is ± 7% over all operating conditions as indicated in the AC characteristics Table.

manual mode speed signal decoding

In manual mode, a high input (>5.5V) on the MAN terminal changes the state of the device from sleep to run. While in the run state the device senses the resistance between the MAN and AUTO terminals by turning on a 2 mA current sink to each terminal. The MAN and AUTO current sinks are multiplied 20 X from the CCS current. This 2 mA current sink creates a 1 V drop across each 0.5 kΩ resistor and a 0 to 2.2 V differential across the 0 to 1 kΩ potentiometer (and thus across the 2 terminals). The SPEED and INT terminals should be utilized as in the proceeding section as a low-pass filter. When the connection to the MAN terminal is opened, the device enters the sleep state. In addition, the device is capable of rejecting up to 2.2 V of source voltage offset (V_{IO}), as indicated in Figure 4.

manual mode speed signal decoding (continued)

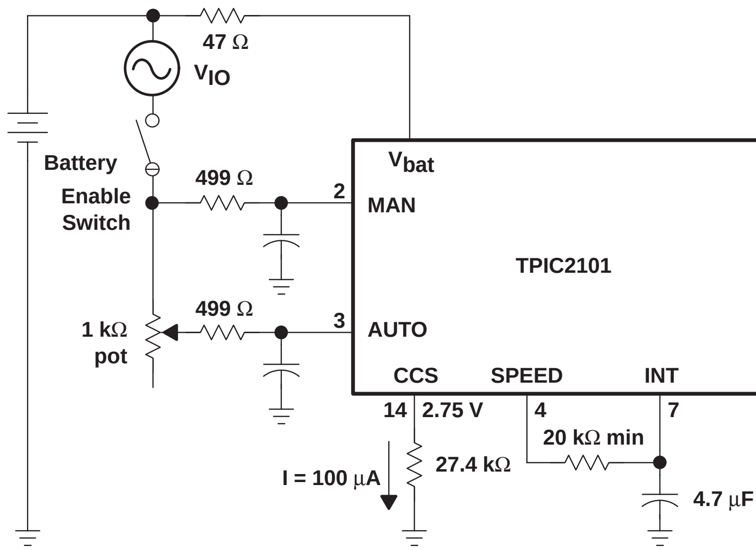


Figure 4. Manual Mode Connections

As in the automatic mode, the device will adjust the GD terminal PWM duty cycle to keep the effective motor voltage constant with changing battery voltages (V_{bat}). The transfer equation for the manual mode is:

$$PWM_{out} = \frac{(2.88 + 6.56(V_{MAN} - V_{AUTO}))}{V_{bat}} \times 100\%$$

Figure 5 shows the output characteristic for various source voltages.

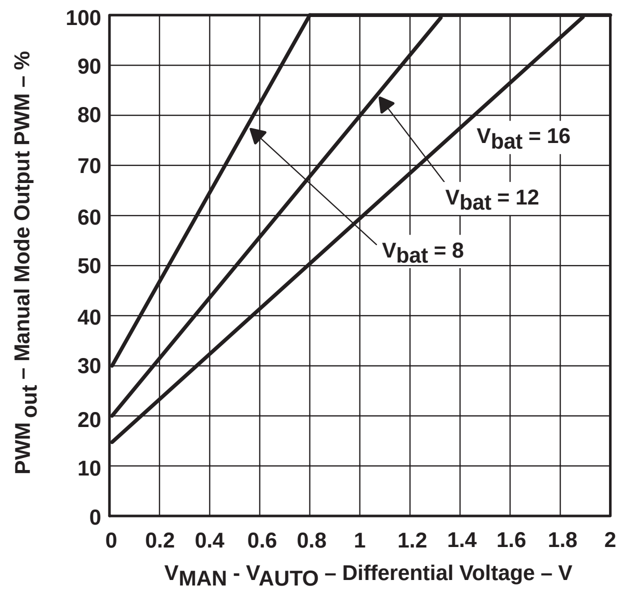


Figure 5. Manual Mode Input Signal vs. Output PWM

The allowable manual mode PWM_{out} variation is ±7% over all operating conditions as indicated in the AC characteristics table.

over/under voltage operating

The TPIC2101 detects an over or under voltage condition (on the V_{bat} terminal) and turns off the gate drive circuit. The device remains in this condition until the supply voltage returns to normal operating voltage. Hysteresis assures that the over/under voltage condition does not toggle off and on near the threshold. The INT terminal pulls toward GND through an internal impedance of less than 500 Ω during the over-voltage condition or during sleep state. This ensures a slow ramp up of the GD terminal PWM when the V_{bat} voltage returns to the operating range.

current limit operation

An over-current condition is detected if the ILS terminal is higher than the ILR terminal while the gate drive (GD terminal) is high. This condition activates a closed-loop control, causing the INT terminal to be pulled low (through an internal resistance less than 500 Ω) lowering the commanded duty cycle to close the loop.

current fault operation

During a window of 8192 clock cycles, a latch is set if at least once during the window, a current limit condition is detected. If a current limit condition is set for eight consecutive 8192 clock cycle windows, the gate drive (GD terminal) will be shut off for a disable period of 65536 clock cycles. During the disable period, the INT terminal is pulled to GND through an internal resistance of less than 500 Ω. After the disable period is completed, an internal restart is attempted. If the current limit is present again, as described above, for 8 consecutive windows, the GD and INT terminals are again pulled to GND and the device remains in this current fault state until the device is cycled through a sleep state to run state. However, if the current limit condition is not present during any of the eight 8192 clock cycle windows, the latches for the 8 count window timer and the two cycle shutdown/restart are reset. See timing diagrams, Figures 6, 7, and 8.

absolute maximum ratings over the operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{bat}‡	–0.3 V to 40 V
Input voltage range, MAN, AUTO	–0.3 V to 40 V
Input voltage range, INT CCS, ILR	–0.3 V to 7 V
Continuous gate drive output current, I_{GD}	±50 mA
Continuous speed output current, $I_{O(SPEED)}$	±1 mA
Continuous output current, $I_{O(V5P5)}$, $I_{O(AREF)}$	20 mA
Continuous ROSC output Current, $I_{O(ROSC)}$	1 mA
Continuous output current, $I_{O(CCS)}$	500 µA
Thermal Resistance, junction to ambient, $R_{\Theta JA}$: D package	131°C/W
N package	78°C/W
Operating free-air termperature range, T_A	–40°C to 105°C
Maximum junction temperature, T_{JM}	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Under load dump conditions, the voltage on V_{bat} can reach 40 V within 1 ms.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{bat}	8	12	16	V
AREF Input current $I_{(AREF)}$	0		2	mA
Input voltage, $V_{I(MAN)}$, $V_{I(AUTO)}$ (manual mode)	6		16	V
Differential voltage, $V_{I(MAN)} - V_{I(AUTO)}$	0		2.2	V
Input voltage, $V_{I(AUTO)}$ (auto mode)	0		5.5	V
V_I, ILR, ILS	0.5		2.75	V
Output resistance, input resistance, $R_{(CCS)}$	27.2	27.5	27.8	kΩ
Output Resistance, ROSC, r_o	20		100	kΩ
Output Capacitance, COSC, C_O	1		5	nF
Gate drive frequency f = 2/(ROSC × COSC), $f_{(GD)}$		20		kHz
Gate drive output capacitance, $C_{O(GD)}$			3300	pF
Operating free-air temperature, T_A	–40		105	°C

electrical characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{bat}	Supply current (average), V_{bat}	V_{bat} = 16 V, GD open, f(osc) = 20 kHz, MAN = AUTO = V_{bat}		4	10	mA
		V_{bat} = 16 V, GD open, f(osc) = 20 kHz, MAN open, Auto mode, AUTO – 99% PWM_{in}		2	10	mA
$I_{bat(Q)}$	Quiescent current (sleep state), V_{bat}	V_{bat} = 13 V, AUTO and MAN open		150	200	µA
		V_{bat} = 13 V, AUTO shorted to MAN, floating		165	200	µA
$V_{(AREF)}$	Voltage supply regulation, AREF	$I_{(AREF)}$ = 0 – 2 mA, MAN = AUTO = V_{bat}	5.225	5.5	5.775	V
V_{IO}	Input offset voltage, current limit comparator, ILS, ILR	AUTO or MAN mode, ILS, ILR common mode, Voltage range 0.5 – 2.75 V, V_{int} = 4.5 V, Detect $I_{(int)}$ > 100 µA			10	mV
I_{IB}	Input bias current, current limit comparator, ILS, ILR†,	ILS, ILR common mode, Voltage range 0.5 – 2.75 V			250	nA
I_{IO}	Input offset current, current limit comparator, ILS, ILR†	ILS, ILR common mode, Voltage range 0.5 – 2.75 V			100	nA
$I_{OL(CLS)}$	Pulldown current, ILS terminal blanking, ILS	ILS = 100 mV, GD commanded low	250	360		µA
$V_{IL(AUTO)}$	Automatic mode low level input voltage, AUTO	MAN open, AUTO mode, Lower $V_{I(AUTO)}$ until $V_{I(SPEED)}$ >2.4V	2.7	3	3.3	V
$V_{IH(AUTO)}$	Automatic mode high level input voltage, AUTO	MAN open, AUTO mode, Raise $V_{I(AUTO)}$ until $V_{I(SPEED)}$ < 2.4 V	3.6	4	4.4	V
$I_{I(AUTO)}$	Input current, automatic mode, AUTO	MAN open, Auto mode, $V_{I(AUTO)}$ = 0 V	–1		–10	mA
$I_{I(AUTOQ)}$	Input current, auto sleep mode, AUTO	MAN open, Sleep state, $V_{I(AUTO)}$ = 0 V	–40	–80		µA
$V_{IH(MAN)}$	High level input voltage, manual mode, MAN	V_{bat} = 9 V to 16 V, $V_{IH(MAN)}$ = $V_{IH(AUTO)}$, Raise $V_{(MAN)}$ until $V_{I(AREF)}$ > 2.5 V	5	5.5	6	V
$V_{IL(MAN)}$	Low level input voltage, manual mode, MAN	$V_{I(MAN)}$ = $V_{I(\ AUTO)}$, Lower $V_{I(MAN)}$ until $V_{I(AREF)}$ < 2.5 V	2.3	2.5	2.7	V
$V_{ID(MAN)}$	Input voltage, manual mode high differential (high speed command), MAN-AUTO	V_{bat} = 16 V, V_{bat} – 3.5 V < MAN < V_{bat}	1.7		2.3	V

† Indicates electrical parameter not tested in production.

electrical characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C (continued)

	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
$V_{ID(low)}$	Input voltage, manual mode low differential (low speed command), MAN–AUTO	V_{bat} –3.5 V < MAN < V_{bat}+ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, PWM_{out} @ $V_{(diff)}$ = 0.2 V ≥ PWM_{out} @ $V_{I(DIFF)}$= 0 V				0.2	V
$I_{I(MAN)}$ $I_{I(AUTO)}$	Input currents, auto and manual mode, MAN, AUTO	V_{bat} –3.5 V < MAN < V_{bat} +ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, MAN – AUTO = 0 V to 2 V, $R_{(css)}$ = 27.5 kΩ to GND		1.70	2	2.30	mA
$I_{I(MANRATIO)}$	Input current, manual mode matching ratio, MAN, AUTO	V_{bat} –3.5 V < MAN < V_{bat} +ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, MAN – AUTO = 0 V to 2 V, R_{css} = 27.5 kΩ to GND		–7		7	%
$I_{I(MAN(a))}$	Input current, man terminal auto mode, MAN	Auto mode,	MAN = 2.2 V	5	10	15	µA
$I_{I(MANQ)}$	Input current, man terminal sleep mode, MAN	Sleep state,	MAN = 2.2 V	5	10	15	µA
$V_{(CCS)}$	Constant current sink voltage regulation, CCS	Auto or Man mode,	$I_{(CCS)}$ = –100 µA	2.58	2.78	2.92	V
$V_{(OV)}$	Over voltage shutdown, V_{bat}	V_{bat} rising from 16 V, Detect $I_{(INT)}$ > 100 µA	INT = 1 V,	17	18.5	20	V
$V_{hys(OV)}$	Hysteresis, over voltage, V_{bat}	V_{bat} rising from 20.1 V, Detect $I_{(INT)}$ < 100 µA	INT = 1 V,	0.5	0.8	0.99	V
$V_{IT-(UVLO)}$	Under voltage shutdown negative going threshold voltage, V_{bat}	MAN = V_{bat}, Detect AREF < 2.5 V	V_{bat} falling from 9 V,	7	7.5	8	V
$V_{IT+(UVHI)}$	Under voltage shutdown positive going threshold voltage, V_{bat}	MAN = V_{bat}, Detect AREF > 2.5 V	V_{bat} rising from 6.9 V,	8	8.5	9	V
$V_{hys(UV)}$	Hysteresis, under voltage, V_{bat}	$V_{(UVHI)}$ – $V_{(UVLO)}$		0.5	1		V
$V_{OH(GD)}$	High level output voltage, gate drive, GD	I_{GD} = –50 mA, Run state	INT = 4.5 V,	V_{bat} –3		V_{bat}	V
		I_{GD} = –2 mA, Run state	INT = 4.5 V,	V_{bat} –0.2		V_{bat}	V
$V_{OL(GD)}$	Low level output voltage, gate drive, GD	Run state, $V_{I(INT)}$ = 0 V,	I_{GR} = 50 mA, V_{COSC} = 1 V			3.5	V
		Run state, INT = 0 V,	I_{GD} = 2 mA, V_{COSC} = 1 V			0.75	V
$V_{GD(SL)}$	Gate voltage, sleep-state, GD	Sleep state,	I_{GD} = 2 mA		0.03	0.75	V
$I_{(GDP)}$	Pulldown current, gate drive passive, GD	V_{bat} open,	V_{GD} = 0.75 V	7.5	20		µA
$I_{(INT)}$	Pulldown current, INT	Run state, $V_{I(INT)}$ = 1 V	V_{ILS} > V_{ILR},	2	3		mA

switching characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{bat} = 16 V, Load = 3300 pF, ROSC = 45.3 kΩ, COSC = 2200 pF			1	µs
t_f	Fall time	V_{bat} = 16 V, Load = 3300 pF, ROSC = 45.3 kΩ, COSC = 2200 pF			0.8	µs
	Output PWM absolute accuracy to spec equation	16 > V_{bat} > 9 Manual and automatic modes GD open, Measure at GD = 0.5 × V_{bat} @ 20 kHz	–7%		7%	
$f_{(osc)}$	Oscillator frequency	ROSC = 45.3 kΩ, COSC = 2200 pF	19	20	21	kHz
	Minimum speed pedestal	MAN = AUTO=V_{bat} = 16	15		21	%DC
		V_{bat} = 16, MAN floating, AUTO @ 99% duty cycle	15		21	%DC

PARAMETER MEASUREMENT INFORMATION

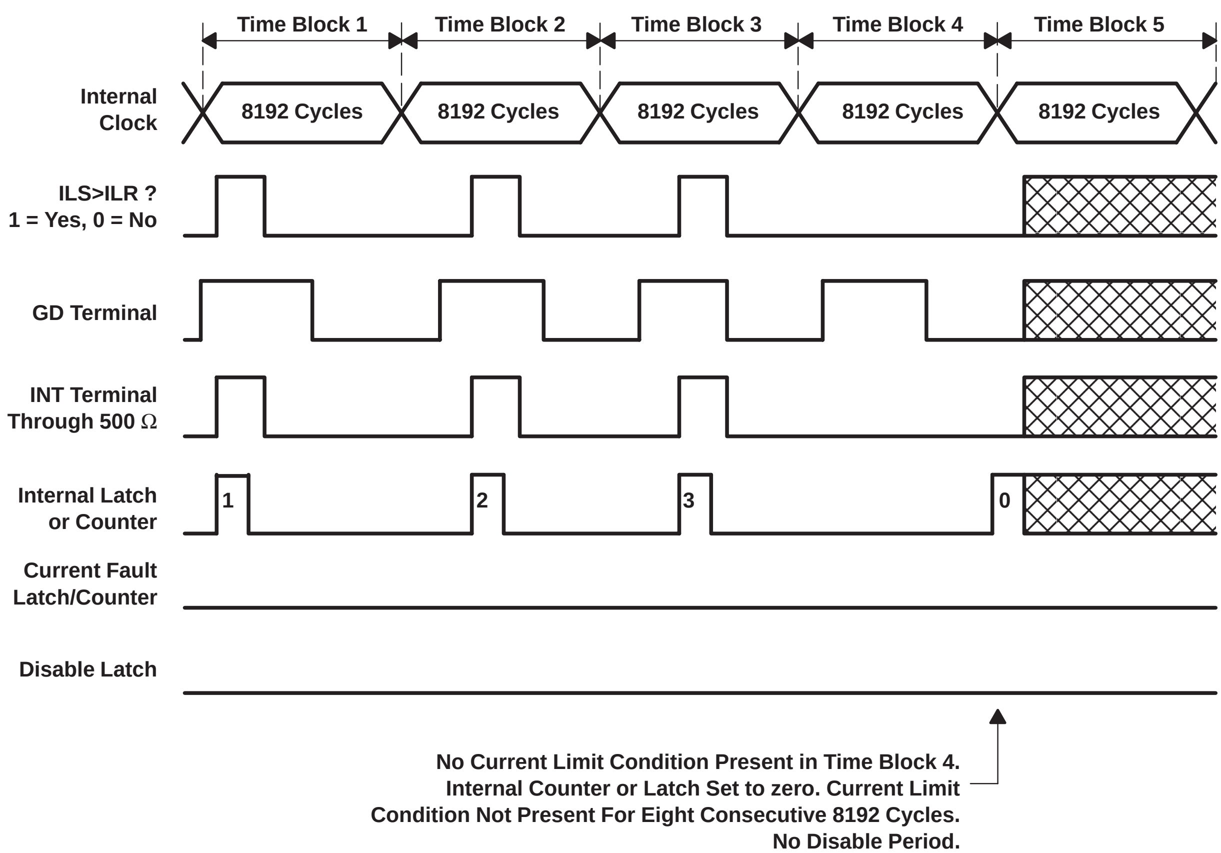


Figure 6. Current Fault Timing Diagram, Normal State

PARAMETER MEASUREMENT INFORMATION

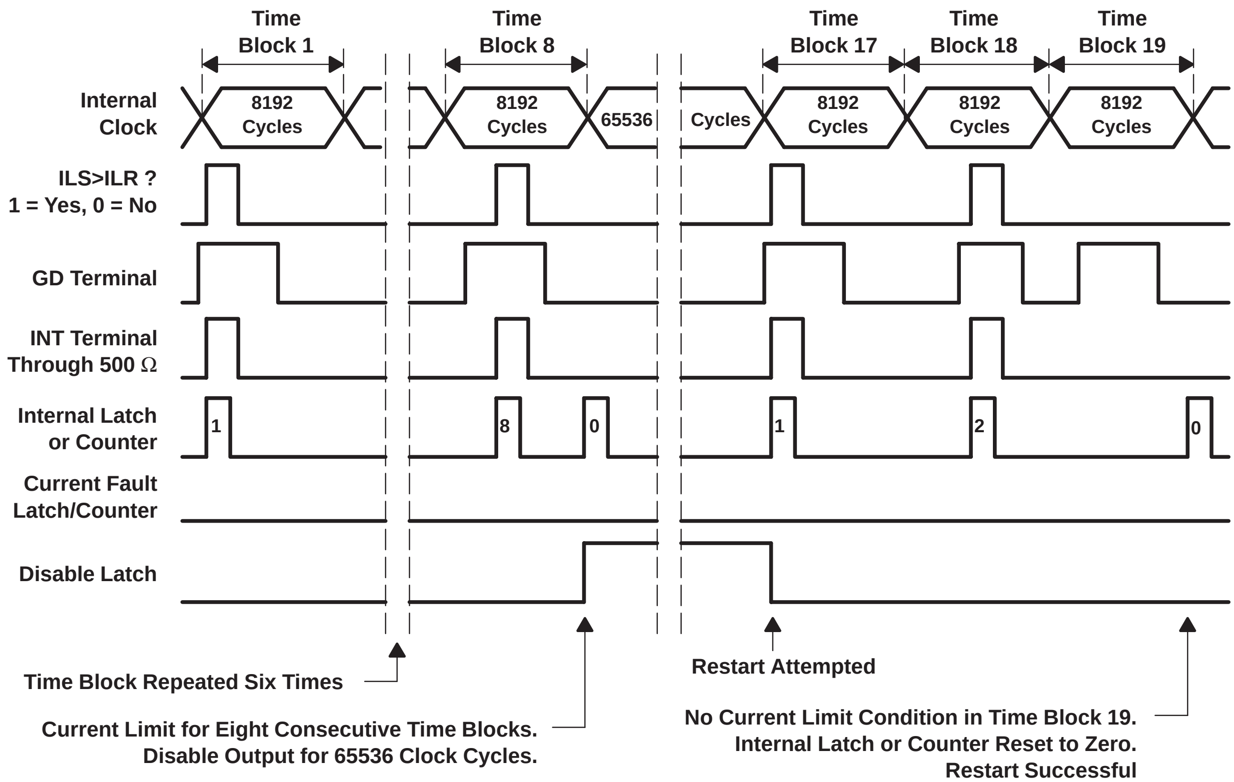
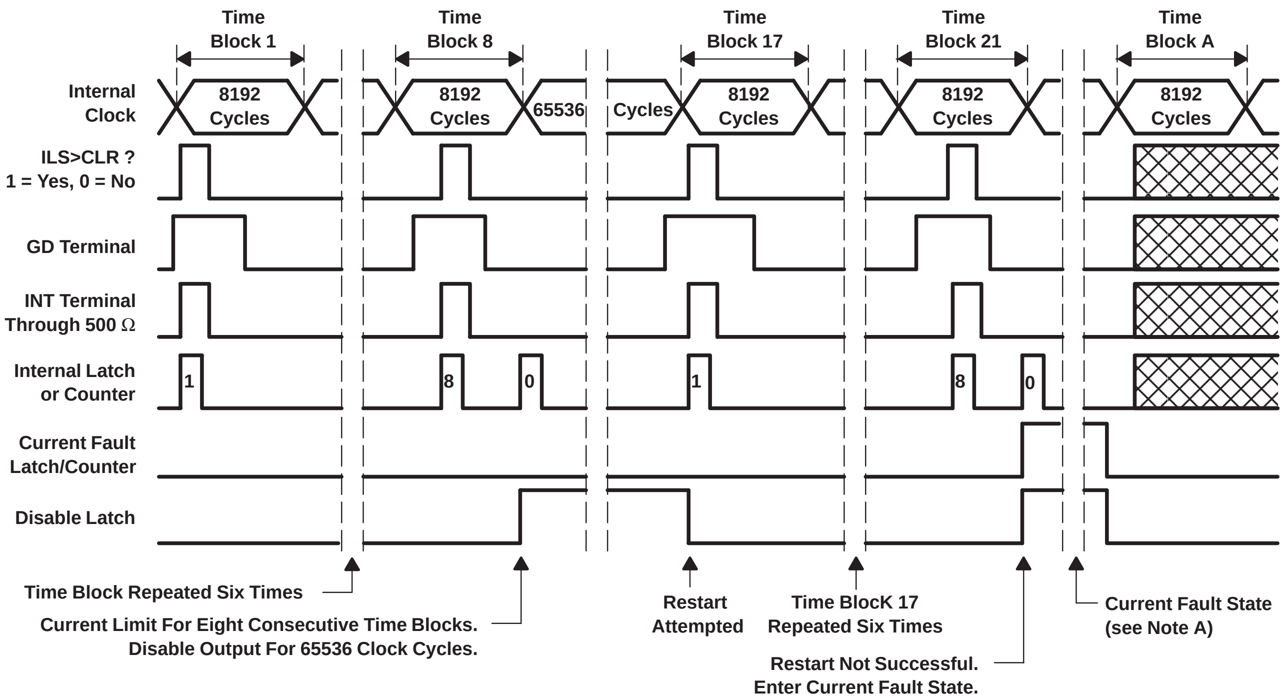


Figure 7. Current Fault Timing Diagram, Over-Current Limit Condition

PARAMETER MEASUREMENT INFORMATION



NOTE A: The integrated circuit remains in this state until cycled through the sleep state into the run state. Timing resumes as shown in time block A at right.

Figure 8. Over-Current Fault State Timing Diagram 3

TYPICAL CHARACTERISTICS

MANUAL/AUTO CURRENT
vs
CCS CURRENT (MANUAL MODE)

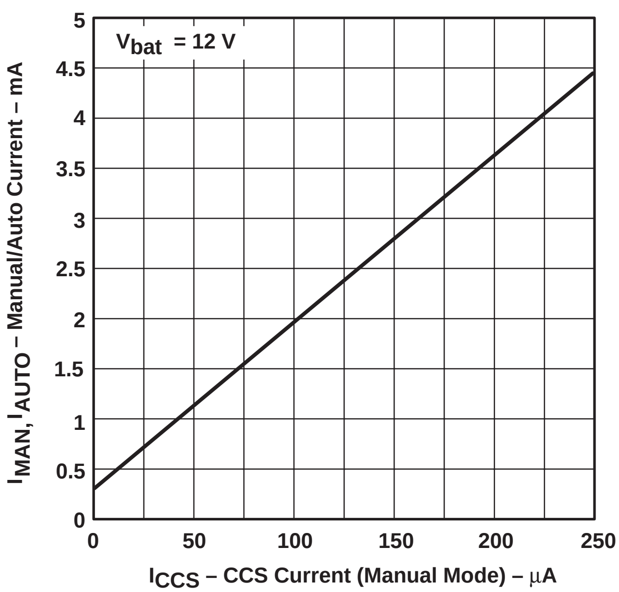


Figure 9

AUTO CURRENT
vs
CCS CURRENT (AUTO MODE)

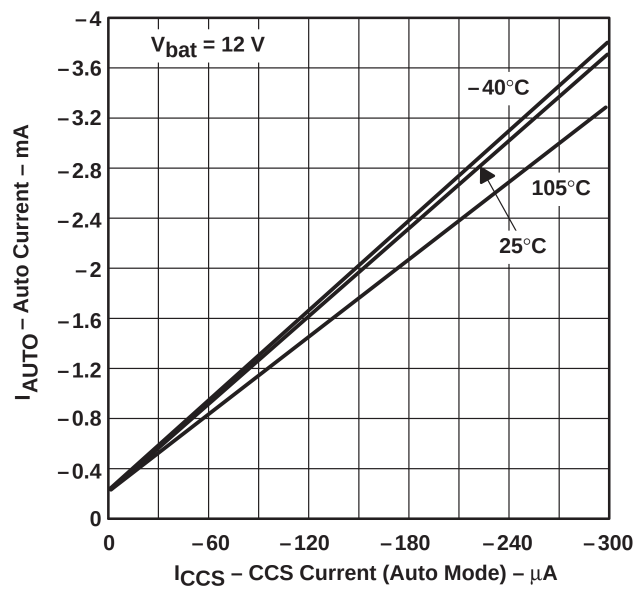


Figure 10

INTEGRATOR PULLDOWN CURRENT
vs
INTEGRATOR INPUT VOLTAGE

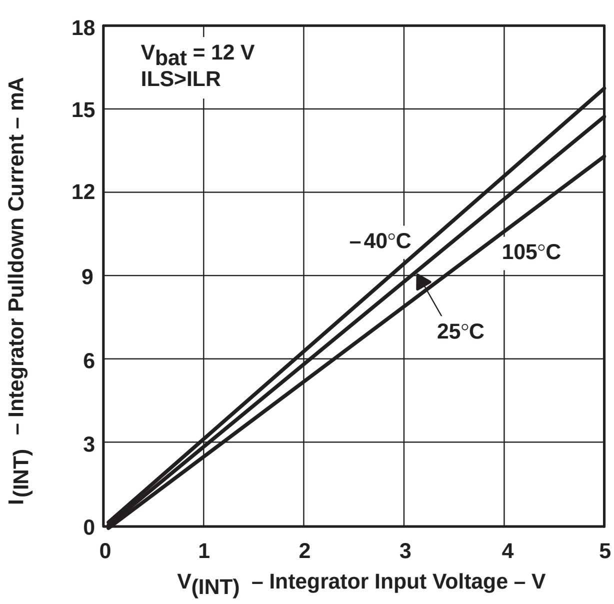


Figure 11

OSCILLATOR CAPACITOR CURRENT
vs
OSCILLATOR RESISTOR CURRENT

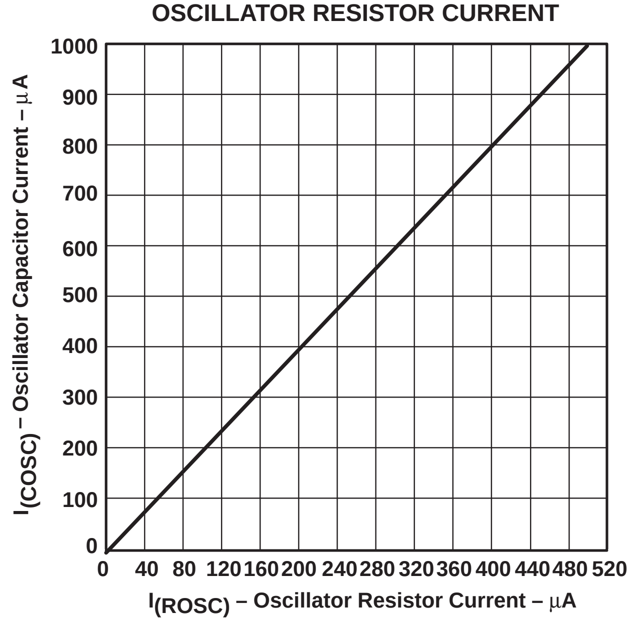


Figure 12

TYPICAL CHARACTERISTICS

GATE DRIVE LOW SIDE
vs
GATE DRIVE CURRENT

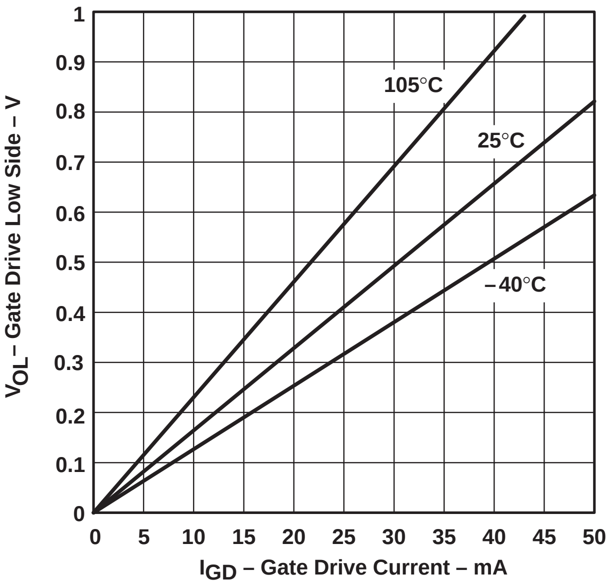


Figure 13

GATE DRIVE HIGH SIDE
vs
GATE DRIVE CURRENT

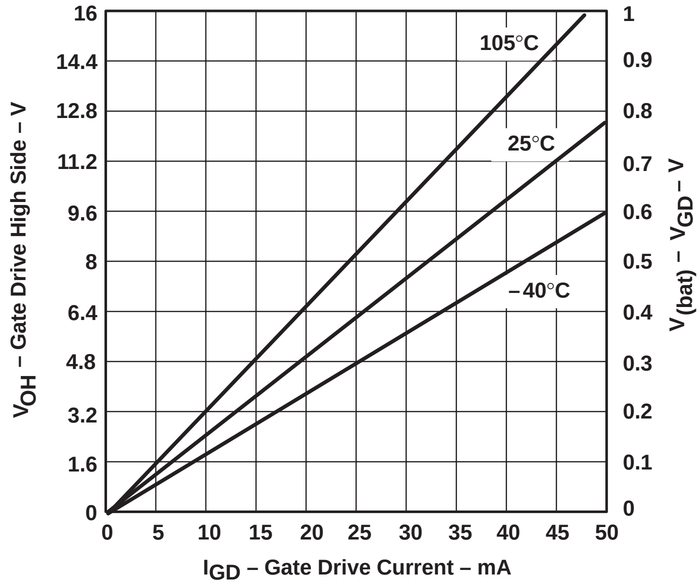


Figure 14

EFFECTIVE MOTOR VOLTAGE
vs
INCOMING PULSE WIDTH MODULATION

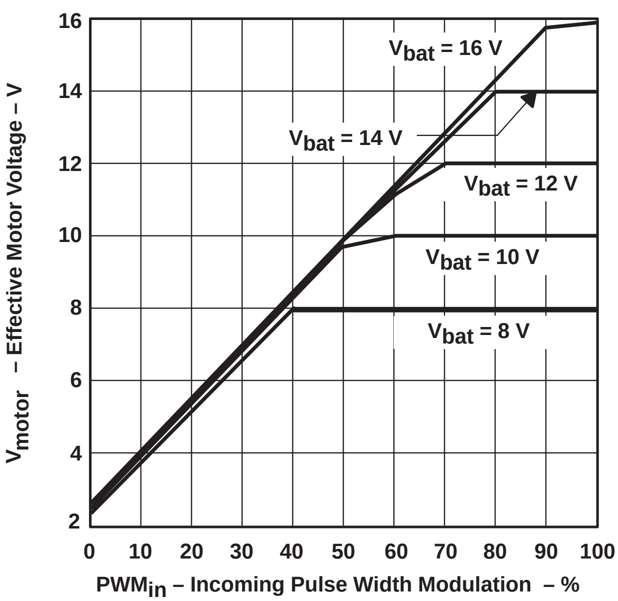


Figure 15

MOTOR RPM
vs
INCOMING PULSE WIDTH MODULATION

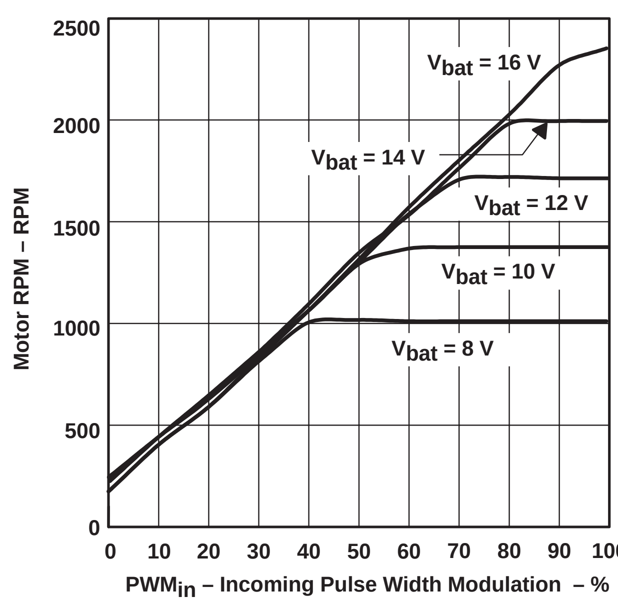


Figure 16

TYPICAL CHARACTERISTICS

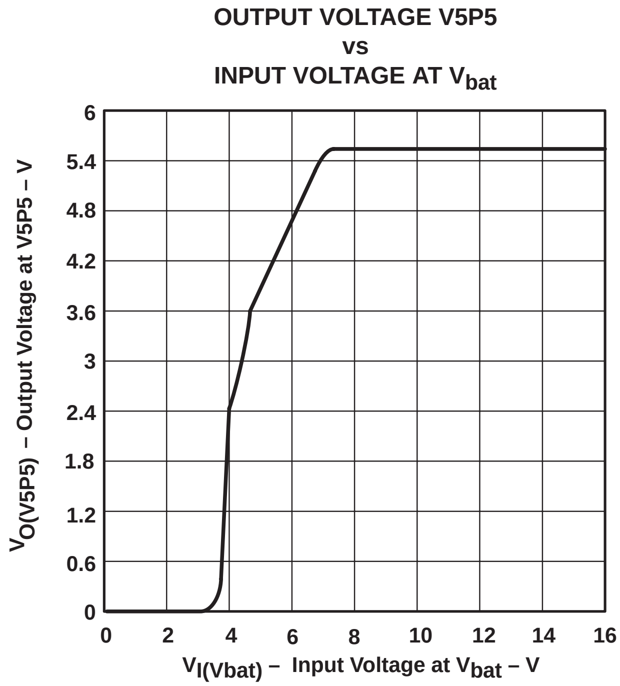


Figure 17

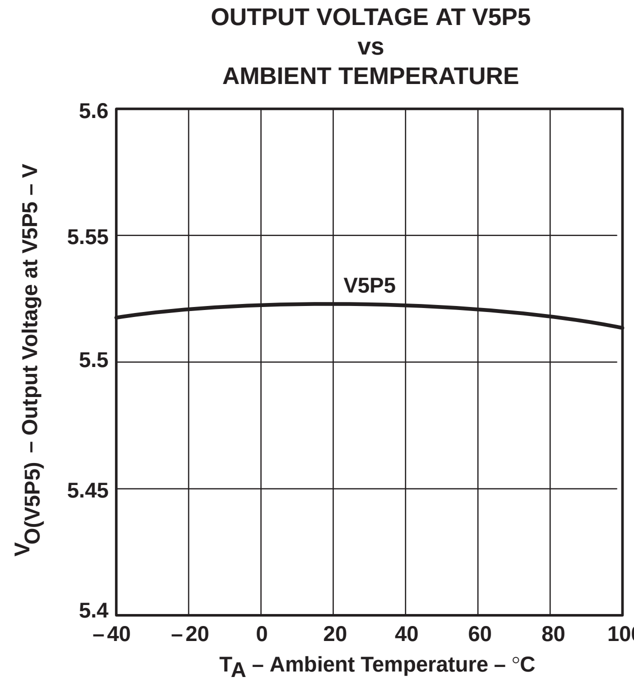


Figure 18

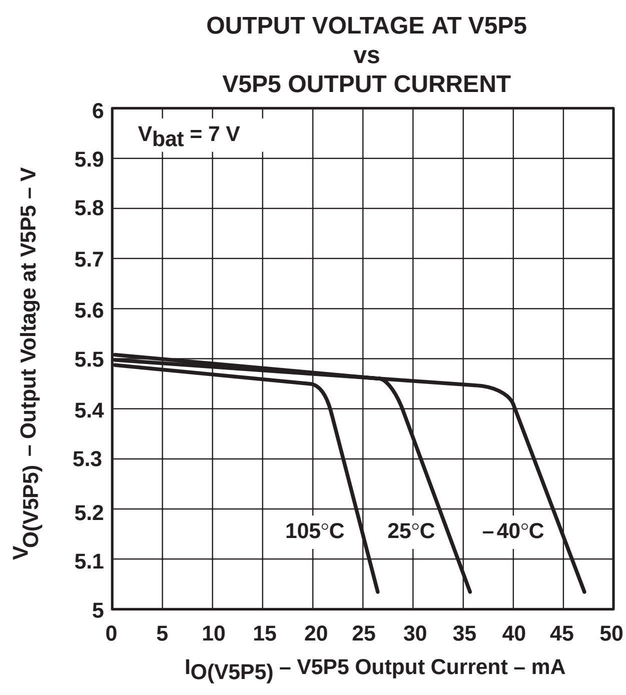


Figure 19

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